International Journal of Applied Science & Environmental Engineering – IJASET 2018

Volume 1 : Issue 1 Publication Date : 28 December, 2018

53 to 56GHz MMIC Non-Foster Enhanced Class-J GaAs pHEMT Power Amplifier

Charles Nwakanma Akwuruoha[1], Zhirun Hu[2]

***Abstract*— Non-Foster circuits are widely used to enhance the bandwidth of microwave circuits owing to its ability to provide the negative impedance required to cancel transistor parasitic capacitance. In this paper, a 53 to 56 GHz MMIC (monolithic microwave integrated circuit) non-Foster enhanced class-J GaAs pHEMT (gallium arsenide pseudo high electron mobility transistor) power amplifier (PA) is proposed. The non-Foster circuit (NFC) is used to enhance the PA output power and gain. The NFC and PA were designed with WIN semiconductor's P10-10 process GaAs pHEMT with periphery of 150 µm. The transistor was biased with drain supply voltage of 2V for the NFC and 3V for the PA with respective quiescent drain-to-source current (I_{DSQ}) of 2mA and 3mA respectively. The PA operates from 53GHz to 56GHz with center frequency of 54.5GHz. The NFC effective negative capacitance stood at -0.15pF at 54.5GHz. Small and large signal simulations result of the PA with and without NFC were obtained and compared at the center frequency The NFC MMIC PA measures 0.9 x 1.0 mm^2 (0.9 mm^2). Simulation results indicate that the PA with NFC demonstrates higher output power of 17dBm, gain of 8dB and 43% PAE than the one without NFC with 15.5dBm output power, 41.5% PAE and 6.5 dB power gain.**

Keywords— Non-Foster circuit, power amplifier, effective negative capacitance, P10-10 GaAs pHEMT process, output power, gain

I. Introduction

Class-J PA was first proposed by Cripps [1] to mitigate the bandlimited of class-AB/B PAs resulting from the effects of the transistor output parasitic capacitance on the fundamental load. This involves the use of reactive terminations to convert the fundamental load from resistive to reactive mode [2]. Class-J GaN HEMT PAs using packaged transistor have been reported in [2]-[6]. MMIC GaAs pHEMT with chip dimensions of 1.57 x 1.29 mm^{2}was reported in [7] while MMIC GaN HEMT (gallium nitride high electron mobility transistor) with 2 x 2 mm^2 dimension was reported in [8]. However the reported PAs in [2]-[8] have operational frequency below 8GHz and do not have an NFC. This implies that the problem of transistor input parasitic capacitance which limits output power and gain was not resolved. In this paper, a compact MMIC NFC class-J PA with smaller chip dimension of 1 x 0.9 mm^2 with operation frequency from 53 to 56GHz is proposed.

The NFC provides the negative capacitance required to cancel the power transistor input parasitic capacitance in order to enhance the PA output power and gain while maintaining the power added efficiency (PAE). The NFC forms part of the input matching network. Although NFCs have the tendency to introduce instability and noise into the circuit [19], it is proven to have significant advantage in improving the output power and gain of PAs when properly stabilized as reported by the workers in [18]-[20] and proposed in this paper.

R. M. Foster in his theorem in [9], which followed the earlier works in [10] and [11], stated that the reactance of a lossless one-port network increases with frequency. The components which obey Foster theorem such as positive capacitance or inductance are referred to as Foster elements while the components which disobeys Foster theorem such negative capacitance or inductance are referred to as Non-Foster elements.

The use of active circuit to generate negative impedance was first proposed by J, G. Linvill in one of his early papers wherein he referred to it as transistor negative-impedance converters [12]. The negative impedance converters (NICs) were used to reduce the losses on telephone lines. The NIC was described as a four-pole network in which the input current is equal to the output current and the input voltage equal to the negative of the output voltage while having the property of an ideal transformer such that the input impedance is equal to the negative of the load impedance. The NIC was classified as open circuit stable (OCS) and short circuit stable (SCS) [12]. The NIC was also described as an active network having a property such that the driving point immittance connected to one terminal pair equals the negative of the load immittance connected to the other terminal pair [13]. In this paper, a balanced Linvill OCS NIC is proposed and will hereafter be called NFC.

Although NFCs were mainly used for the enhancement of antenna bandwidths [15]-[17], it has also been used to increase the gain of CMOS distributed power amplifier [18]. NFC has also been used as an inter-stage matching network of a two-stage GaN HEMT which resulted in increased performance [19].

[1,2]*School of Electrical and Electronic Engineering, The University of Manchester, Manchester United Kingdom*

International Journal of Applied Science & Environmental Engineering – IJASET 2018

Volume 1 : Issue 1 Publication Date : 28 December, 2018

The bandwidth of an HBT Doherty power amplifier (DPA) was reportedly enhanced by an NFC in [20]. To the best of the Authors' knowledge, a 53 to 56GHz MMIC Non-Foster class-J GaAs pHEMT PA, has yet to be reported. This paper is structured as follows. In section II, class-J theory is discussed. Section III contains the Non-Foster circuit theory and design. Section IV, discusses the PA circuit design and performance results and compares it with the reported NFC PA modes. Section V concludes the paper.

II. Class-J Theory

The class-J PA mode which utilizes the application of reactive terminations to the fundamental and second harmonic, aims to change the fundamental load from resistive to reactive regime while counteracting the effects of transistor output capacitance [1]. In class-J PA higher order even harmonic than the second harmonic does not exist while the third harmonic is assumed short. Class-J mode results in 45^o phase shift between the drain current and voltage of the PA which in turn enhances the performance of the PA in the scale of classes AB and B PAs [7]. The class-J drain current and voltage waveforms on the transistor intrinsic nodes are sine waves consisting of even harmonics. The drain current waveform of a class-J PA with phase angle denoted by θ has a half-cosine waveform given by [8]

$$I_D(\theta) = I_{D,\,max}/\pi + I_{D,\,max}/2\cos\pi + 2I_{D,\,max}/3\pi\cos 2\theta \quad (1)$$

where $I_{D,\,max}$ is the peak drain current of the transistor.

The drain voltage is given by [8]

$$V_D(\theta) = (V_{D,\,dc} - V_{Knee})[\cos(\theta) - \sin(\theta) + \sin(2\theta)/2] \quad (2)$$

where $V_{D,\,dc}$ is the dc drain supply voltage and V_{Knee} is the transistor knee voltage.

The fundamental and second harmonic loading impedances Z_{fo} and Z_{2fo} are functions of optimum load resistance R_{opt} given by [1]-[2]

$$R_{opt} = (V_{D,\,dc}) / [(I_{D,\,max}/2)] \quad (3)$$

$$Z_{fo} = R_{opt} + j * R_{opt} \quad (4)$$

$$Z_{2fo} = 0 - j*3\pi / 8*R_{opt} \quad (5)$$

The third harmonic loading impedance Z_{3fo} is given by

$$Z_{3fo} = 0 \quad (6)$$

III. NFC Circuit Theory and Design

A. *NFC theory*

Foster circuits have positive reactance slope with respect to the frequency as well as reflection coefficient with moves in a clockwise direction with respect to frequency on a Smith chart [9]. The derivative of the reactance and susceptance of a Foster circuit (X_{FC}) and (B_{FC}) respectively, with angular frequency (ω) is greater than zero [16]. Foster elements obey Foster theorem and include positive capacitance and inductance. The non-Foster circuits disobey Foster theorem. The NFCs have a negative reactance slope with respect to frequency as well as reflection coefficient which moves in a counter-clockwise direction with respect to frequency on a Smith chart. The derivative of the reactance and susceptance of an NFC (X_{NFC}) and (B_{NFC}) respectively, with respect to angular frequency ω is less than zero. Non-Foster elements include negative capacitance and inductance [16]. Mathematically,

$$dX_{FC}/d\omega > 0 \quad \text{and} \quad dB_{FC}/d\omega > 0 \quad (7)$$

$$dX_{NFC}/d\omega < 0 \quad \text{and} \quad dB_{NFC}/d\omega < 0 \quad (8)$$

B. *NFC design*

The NFC was designed based on WIN semiconductor's P10-10 GaAs pHEMT process. The two transistors (Q_1 and Q_2) have periphery of 150µm each and biased with drain supply voltage of 2V at quiescent drain-to-source current of 2mA as shown in DC biased points I_{DS} versus V_{DS} characteristics in Fig. 1. The NFC schematic circuit consists of lumped components which include inductors, capacitors and resistors as shown in Fig. 2. The NFC design was aimed at enhancing stability using stability resistors as well as achieving negative reactance slope across the entire operational bandwidth of the proposed PA as shown in the graph of magnitude and imaginary part of input impedance (Z_{in}) in Fig. 3. The effective capacitance of the NFC across the 3GHz operational bandwidth is shown in Fig. 4. The NFC effective negative capacitance at 54.5GHz center frequency stood at -0.15 pF.

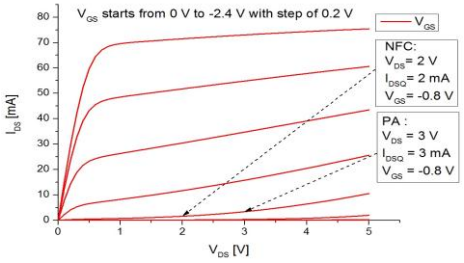

Fig. 1 NFC and PA bias points

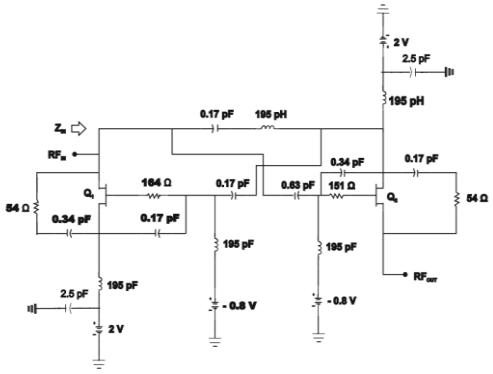

Fig. 2 NFC schematic circuit

International Journal of Applied Science & Environmental Engineering – IJASET 2018
Copyright © Institute of Research Engineers and Doctors, SEEK Digital Library
Volume 1 : Issue 1 Publication Date : 28 December, 2018

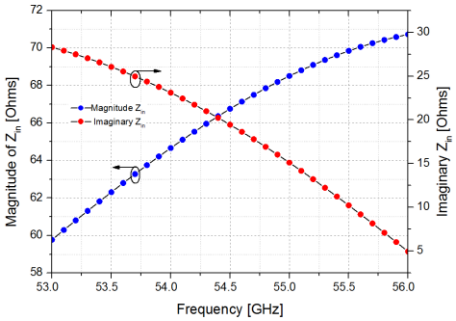

Fig. 3 Magnitude and Imaginary part of input impedance

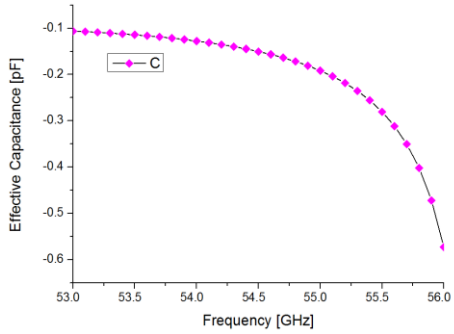

Fig. 4 Effective Capacitance

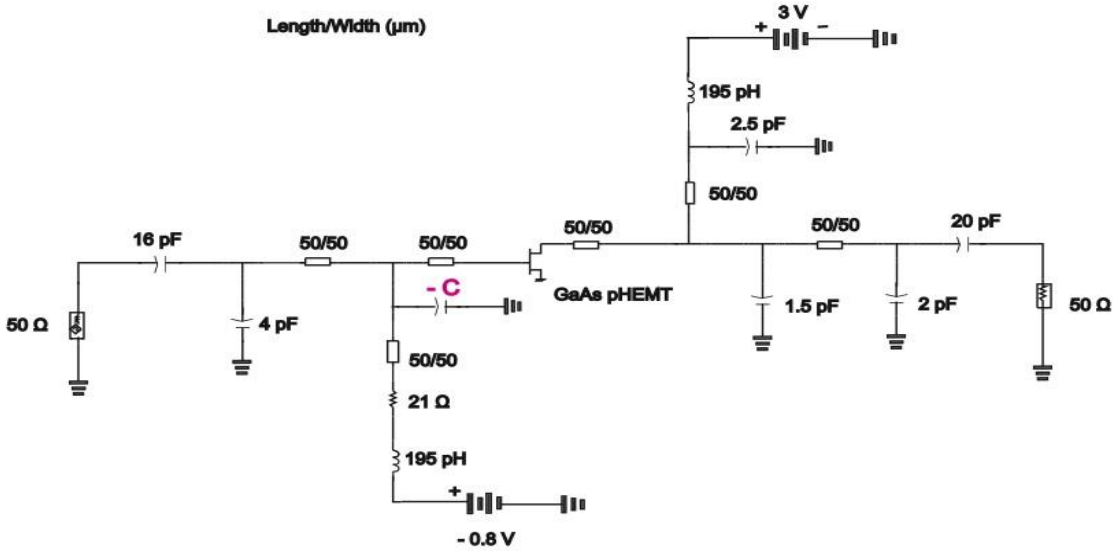

Fig. 5 PA Schematic circuit

IV. PA circuit design and Simulation Result

A. *PA design*

The PA circuit was designed based on WIN Semiconductor's P10-10 process GaAs pHEMT with device periphery of 150µm biased with drain supply voltage of 3V at quiescent drain-to-source current of 3mA. Harmonic Load pull and Source pull simulations where respectively used to

equired to achieve maximum power at the PA center frequency of 54.5GHz. The NFC forms part of the input network in consideration with PA stability and efficiency. The components consist of distributed microstrip transmission lines (with dimensions in µm) as well as capacitors, inductors and resistors. One of the main considerations in this design is to ensure that the NFC is placed in the position on the PA circuit where it provides optimum non-Foster reactance devoid of oscillations or instability. The second consideration is to ensure that the PA circuit size remains compact in-line with the proposed MMIC PA design objective. A compact PA was achieved as shown in the schematic and layout in Figs. 5 and 6 respectively. The NFC PA is unconditionally stable as shown in Fig. 7.

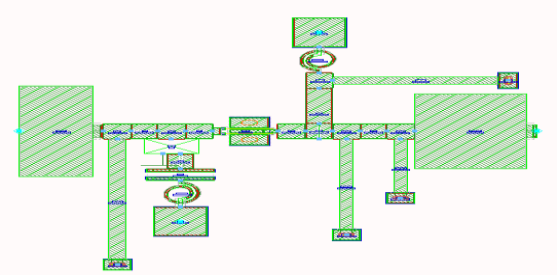

Fig. 6 PA Layout

B. *PA simulation result*

The simulation result in this paper will be considered in accordance with the small and large signal simulations. In the small signal s-parameter simulation result shown in Fig. 8 regarding the gain (S_{21}) and reverse isolation (S_{12}) of the PA with NFC (denoted as PA_w_NFC) and the PA without NFC (denoted as PA_wo_NFC), the PA with NFC has a higher S_{21} of 8dB while the PA without NFC has an S_{21} of 5dB. This indicates a 3dB increase in small signal gain for the PA with NFC. The large signal simulation result shown in Figs. 9 and 10 indicates the PA with NFC has higher power added efficiency (PAE) 43% and a higher power gain of 8dB than the PA without NFC with a PAE of 41.5% and power gain of 6.5dB. The output power of the PA with NFC stood at 17dBm while the output power of the PA without NFC stood at 15.5dBm. The proposed PA compares with other reported NFC PA modes as shown in Table. I.

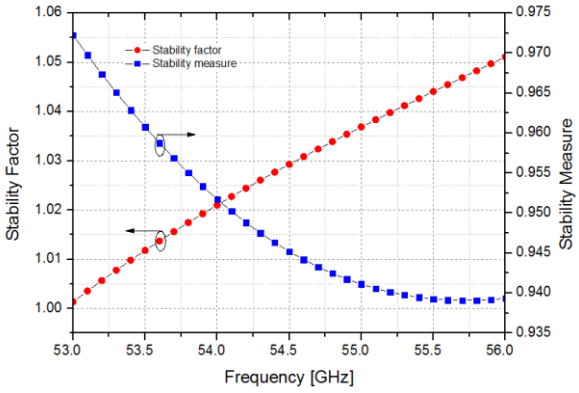

Fig. 7 PA Stability

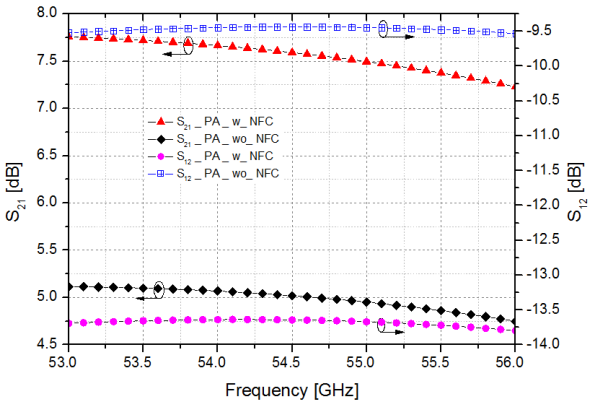

Fig. 8 S_{21} and S_{12}

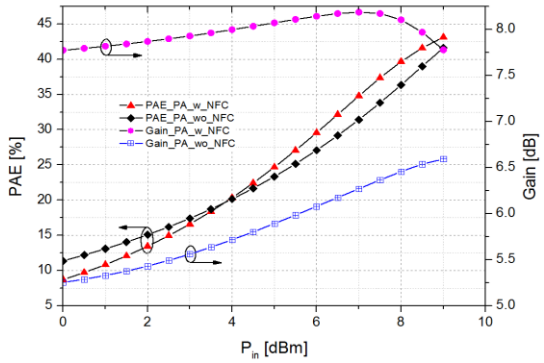

Fig. 9 PAE and Power gain

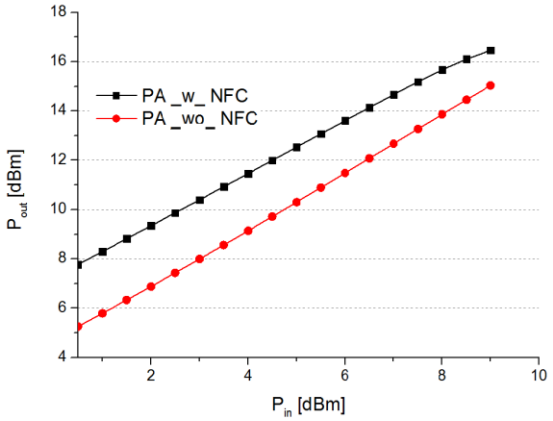

Fig. 10 Output Power

TABLE. I
COMPARISON OF PROPOSED PA WITH OTHER REPORTED NFC PA

Ref.	PA Performance				
	Topology	**Device**	**Frequency Range (GHz)**	**Output power (dBm)**	**Gain (dB)**
[18]	DA	CMOS	1 - 30	21	13.2
[19]	DA	GaN pHEMT	6 - 18	35.7	13.5
[20]	DPA	GaN HEMT	1.9 - 2.2	30	-
This work	Class-J	GaAs pHEMT	53 - 56	17	8

v. Conclusions

A 53 to 56GHz MMIC non-Foster class-J GaAs pHEMT power amplifier has been proposed, designed and simulated. The simulation results indicate that the performance of a class-J PA regarding output power, gain and power added efficiency can be enhanced by the addition of an NFC in the input network.

Acknowledgment

The Authors are grateful to the tertiary education trust fund of Nigeria (TETFund Nigeria) for sponsoring this research work. We also wish to thank WIN Semiconductors for providing the model used in this work.

References

[1] S. C. Cripps, "RF Power Amplifiers for Wireless Communications," 2nd ed., Boston, Artech House, Inc. 2006. Ch.4, sec. 2, pp. 68-76.
[2] P. Wright, J. Lees , J. Benedikt, P. J. Tasker and S. C. Cripps, "A Methodology for Realizing High Efficiency Class-J in a Linear and Broadband PA", IEEE Trans. Microw. Theory Tech. , vol. 57, no. 12, pp. 3196-3204, Dec. 2009.
[3] N.Tuffy, A. Zhu and T. J. Brazil, "Class-J RF power amplifier with wideband harmonic suppression", in IEEE MTT-S Int. Microw. Symp. Dig. , 2011, pp. 1-4.
[4] R. Ma, S. Goswami, K. Yamanaka and Y. Komatsuzuki, "A 40-dBm high voltage broadband GaN Class-J power amplifier for PoE micro-basestations", in IEEE MTT-S Int. Microw. Sym. Dig. , 2011, pp. 1-4.
[5] X. Fu, D. T. Bespalko, and S. Boumazia, "Novel dual-band matching network topology and its application for the design of dual-band Class-J power amplifiers", in IEEE MTT-S Int. Synp. Dig. , 2012, pp. 889-1827.
[6] Y. Guan, W. Chen and Z. Feng, "High efficiency and wideband CLASS-J power amplifier using 2nd harmonic microstrip stub matching", in Proc. ICMMIT, 2012, pp. 1-4.
[7] A. Alizadeh, and A. Medi, "A Broadband Integrated Class-J Power amplifier in GaAs pHEMT Technology", IEEE Trans. Microw. Theory Tech. , vol. 64, no. 6, pp. 1822-1830, Jun. 2016.
[8] S.Rezaei, L. Belostotski, F. M. Ghannouchi, and P. Aflaki, "Integrated Design of a Class-J Power amplifier", IEEE Trans. Microw. Theory. Tech. , vol. 61, no. 4, pp. 1639-1648, Dec. 2013.
[9] R. M. Foster, " A reactance theorem", Bell System technical Journal, vol. 3, no. 2, pp. 259-267, Nov. 1924.
[10] G. A Campbell, "Physical Theory of Electric wave Filters", Bell System Technical Journal, vol. 1, no. 2, pp. 1-32, Jan. 1922.
[11] O. J. Zobel, "Theory and Design of Uniform and Composite Electric wave Filters, Bell System Technical Journal, vol. 2, no. 1, pp. 1-46, Jan. 1923.
[12] J. G. Linvill, "Transistor Negative-Impedance Converters", IRE Trans. Circuit Theory, June 1953, pp. 725-729.
[13] I. A. Larky, "Negative Impedance Converters", IRE Trans. Circuit Theory, Sep. 1957, pp. 124-131.
[14] W. R. Lundry, "Negative Impedance Circuits-Some Basic Relations and Limitations", IRE Trans. Circuit Theory, Sep. 1957, pp. 132-139.
[15] S. E. Sussman-Fort, "Matching Network Design using Non-foster impedances", Int. Journal of RF and Microwave Computer-Aided Engineering", Wiley periodicals, 2006, pp. 135-142.
[16] A. A. Muller and S. Lucyszyn, "Properties of purely reactive Foster and Non-Foster passive networks", Electronic letters, vol. 52, no. 23, pp. 1882-1884, Nov. 2015.
[17] A. M. Elfrgani and R. G. Rojas, "Successful Realization of Non-Foster circuits for wideband antenna applications", in IEEE MTTS-S Int. Microw.Symp. Dig. 2015, pp. 1-4.
[18] A. Ghadiri, and K. Moez, "gain-Enhanced Distributed Amplifier Using Negative Capacitance", IEEE Trans. Circuits and Sys, vol. 57, no. 11, pp. 2834-2843, June 2010.
[19] S. Lee, H. Park, J. Kim, and Y. Kwon, "A 6-18 GHz GaN pHEMT Power Amplifier Using Non-Foster Matching", in IEEE MTT-S Int. Microw. Sym. Dig. 2015, pp. 1-4.
[20] L. M. Ledezma, "Doherty power amplifier with Lumped non-foster impedance inverter", in IEEE WMCS Symp. , 2015, pp. 1-4.