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1.5 Bit/Stage, 12-Bit Pipeline ADC Design with Foreground Calibration

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***Abstract*—In this paper, 12-Bit pipeline ADC is to be designed together with caring non-idealities. Pipeline issue in modern computers is quite advantageous for performance. Such structure can be constructed in analog-to-digital converters to make the performance faster. By considering the non-ideal cases for the design, more realistic outputs are expected. There are several non-ideal effects that lower the ADC performance such as gain error and capacitor mismatches. By using calibration techniques like background or foreground calibration, non-ideal effects can be reduced. In this paper, foreground calibration technique is applied and tabloid results are presented at the end. Modelling of the pipeline ADC is constructed on Matlab Simulink environment.**

Keywords—ADC, data converter, foreground, non-idealities, pipeline, sample and hold

I. Introduction

This paper aims to design a pipeline ADC where will be several design issues and Matlab Simulink details together with test results. Moreover, this paper considers a calibration technique to have more like an ideal model. Even, Matlab Simulink design presents an ideal model, the added non-idealities in the scope of the study will be handled. In the literature, there are several examples related to pipeline ADC design. This study contains Matlab related modelling, therefore, first of all, the higher level modeling research papers were reviewed. For the top-level design, Fig. 1 shows how the stage based architecture is constructed as happens in the previous works.

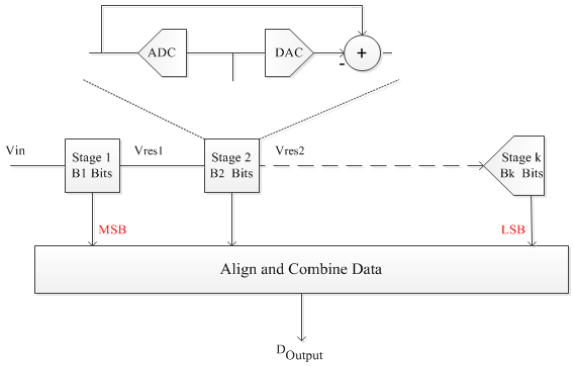

Fig. 1. Pipeline ADC Block Diagram.

Furthermore, in Fig. 1, whereabouts the data out alignment & combination, calibration should be treated. In foreground calibration technique, the normal operation has to be interrupted when a test signal is injected at input point. All the foreground calibration methods need this interruption of normal converter operation to start a calibration process. Generally, the error corrections are obtained just after power is turned on. Then, if the ADC works continuously, some errors that vary with environment change cannot be overcome. Therefore, background calibration technique should be introduced to solve this problem [1]. In a 13-bit 10 MHz BiCMOS ADC design as an example, the first background calibration technique is introduced. This calibration does not affect the normal operation of the converter. Furthermore, it does improve the linearity during normal operation. The basis of this calibration technique is an oversampling sigma-delta ratio calibrator working synchronously with the converter in background. In the design of background calibration technique, Li and Moon propose to improve background digital calibration techniques to correct ADC's errors. These errors can be listed as capacitor mismatch, opamp dc gain, offset, and switch feedthrough [2]. Foreground calibration lacks tracking capability; therefore, it is sensitive to drift in temperature, voltage supply, and device aging. Background calibration, no matter digital or analog, calibrates ADCs continuously in the background during normal operation thus, it has the advantages of tracking temperature change, voltage supply variations, and device aging [3-5]. Nevertheless, background calibration yields extra analog circuit complexity and area trade-off, on the other hand, foreground calibration can be applied in some special systems easily that allow intermittent operation even is recently in use. This paper considers the foreground calibration as presented in the following Fig. 2 [6].

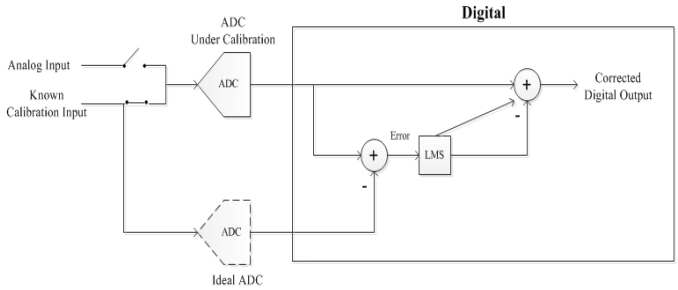

Fig. 2. Foreground calibration (LMS: Least Mean Square) [6].

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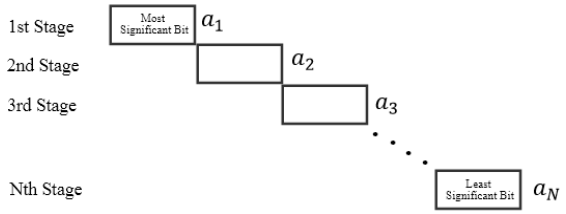
II. Pipeline ADCs and Calibration

Pipeline ADC has wide range of usage in the systems of communications. It has several specialties related to resolution, speed, low power dissipation and dynamic performance. Pipeline ADCs have stage based structure in where each stage has sample and hold (S&H), DAC and ADC in the feed forward path, a differentiator and an operational amplifier. Pipeline ADCs suit applications that require high sampling rate and precision. In digital communications, ADCs work well because the dynamic performance is an important issue [7].

A. *Pipelined ADCs*

Pipeline converters are the ones use a cascade of individual stages that every stage processes basic functions needed for sequential algorithm. Some like in computer architecture fetch-decode-execute operations, pipeline issues for ADC has the same philosophy. In Fig. 3. consecutive pipeline operations are presented.



$$2^{N-1}a_1 + 2^{N-2}a_2 + \cdots + 2^1 a_{N-1} + 2^0 a_N$$

Fig. 3. An N-bit, ideal ADC with 1-bit per stage architecture.

In this scheme the two important phenomena is called: *throughput* and *latency*. In every stage, there are its indices amount of $D_{outputs}$ relatedly the throughput concept. The implementation of the pipeline ADC bases on bit per stage. In this project 1.5 bit/stage is to be used (9 stages), therefore, Fig. 3 gives the details about the motivation of this circuit design.

B. *Foreground Calibration*

Low opamp gain and capacitor mismatches are responsible for the missing codes that causes linearity breakdown of the pipeline ADC. Calibration of these unwanted conditions can be obtained by opamp gain and matching capacitor treatment. As new deep sub-micron technologies support digital circuits with low power consumption and area relatedly previous technologies, digital calibration has become an important issue for low powered and much linear ADCs [6]. In the choice of calibration technique, several papers in the literature were searched to decide for this paper. First of all, the calibration techniques are inspected. There are analog and digital calibration techniques. Recently, the digital calibration techniques are used mostly as either foreground calibration or background calibration methods. In digital calibration technique, code errors are calculated in the digital domain and it gives information about the precision requirements of analog circuits. There are several types of enhancement techniques as;

i.) Trimming of elements
ii.) Foreground calibration
iii.) Background calibration
iv.) Dynamic matching

In this paper, foreground calibration technique is to be utilized. Foreground calibration assesses the unknown error sources by interfering with ordinary ADC operation and applying a known input to the ADC. By contrasting the output of the ADC with the normal ADC output under ideal conditions, the effect of error sources can be regulated. The upside of a foreground calibration is to have calibration in a few clock cycles, the reason why error signal correlation with error sources is high that cause missing code. The downside of foreground calibration is to have ADC been offline for each calibration attempt. This makes the calibration impossible for some special applications [6].

III. Design Issues of the Pipeline ADC with Calibration

In SoC applications, usage of pipeline analog-to-digital converters increases. Thanks to its resolution at high-speed operation, many of the CMOS related SoCs include embedded pipeline ADCs. In the following parts, the designed pipeline stages are given which is the first part of SoC design modelling.

A. *1.5 Bit/Stage in Pipeline ADCs*

In this paper, 1.5 bit per stage is used. In pipeline converters, there are several lower-resolution stages which are connected series in cascade. Following, Fig. 4 illustrates the higher level design for 9 stages in Simulink.

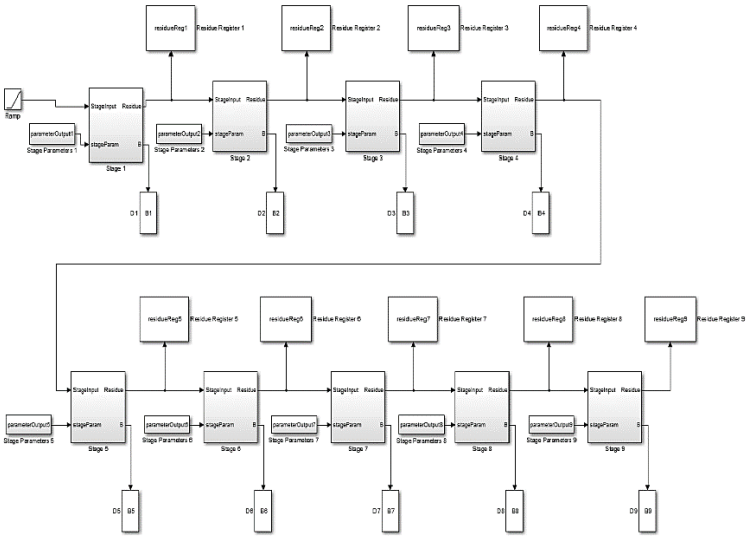


Fig. 4. Higher level design of pipeline ADC – 9 stages, 1.5 bits per stage.

In Fig. 5, the individual pipeline higher level stage is presented. Input should be sourced with a ramp function.

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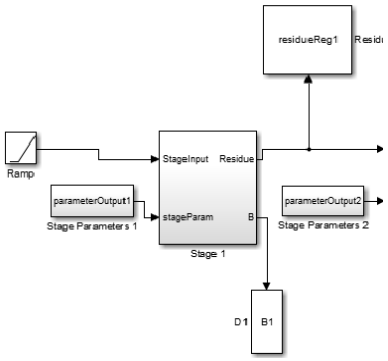

Fig. 5. Higher level of first pipeline stage.

Moreover, in the Fig. 6 and Fig. 7, summary of all proposed top-down design in this paper is illustrated without calibration and non-ideal effects. In Fig. 6, first stage is shown.

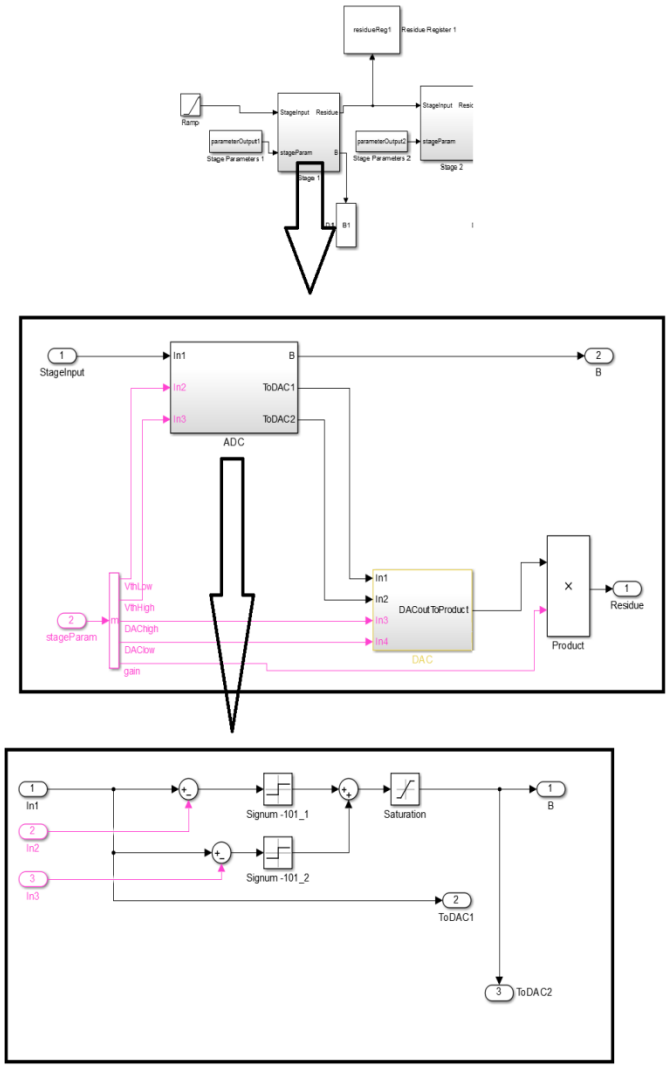

Fig. 6. Higher details of the each stage – ADC [8].

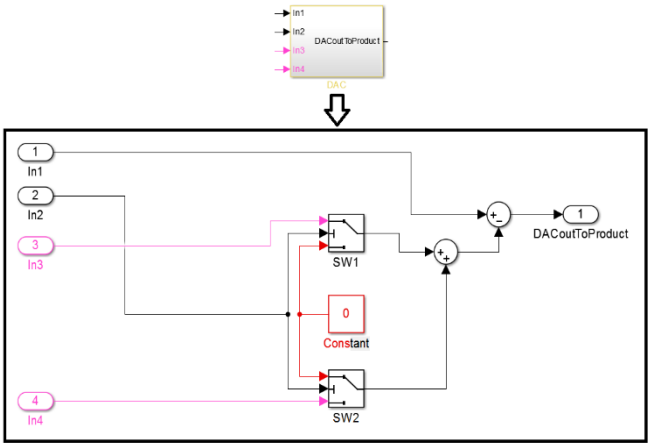

Fig. 7. Higher details of the each stage – DAC [8].

B. *Calibration*

In the Fig. 8, the foreground calibration is to be illustrated. The main procedure on the foreground as shown previously is to find the difference between ideal and non-ideal sub-ADC output signal and calibrate DAC. The resultant is compared how much it deviates from the ideal and the compensation via subtraction from non-ideal is applied. Moreover, in some papers, the ideal MDAC (reference MDAC) is used to calibrate some errors like mismatches and gain. Output analog resultant is digitized to find out how much it has been affected in the digital to analog conversion phase in the sense of DAC calibration.

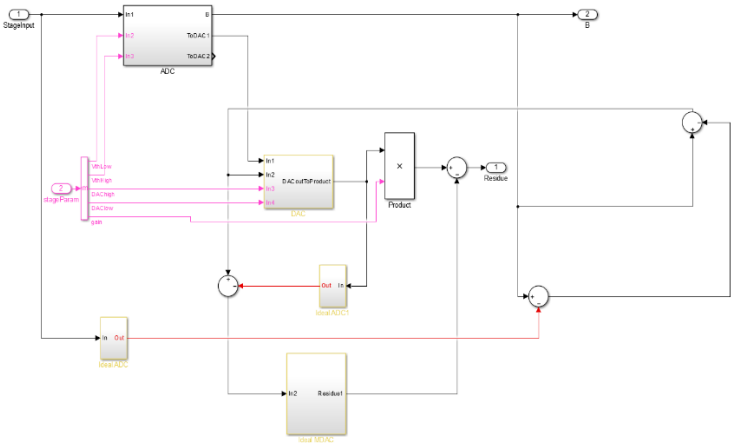

Fig. 8. Simulink conceptual foreground scheme on the exemplary stage.

C. *Non-idealities*

In pipeline ADC, non-idealities associated with sub-ADCs, sub-DACs and gain stages result in error for overall pipeline ADC performance. There are some important sources of error as sub-ADC errors, gain stage error, sub-DAC errors etc. The aim of the design with calibration is to obtain a converter as close as to the ideal conditions. Basic non-ideal cases are shown as follows [9].

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1) *Offset in Sub-ADC:*

Comparator outputs a signal that shows if the input signal is larger than the reference or not. In the case of a difference between two input signals, the offset is to be added on. On the other hand, if two input signals are too close to each other, it may result in incorrect outputs, then incorrect reference is subtracted from the input. In Fig. 9, the effect of offset in a pipeline stage is measured and shown.

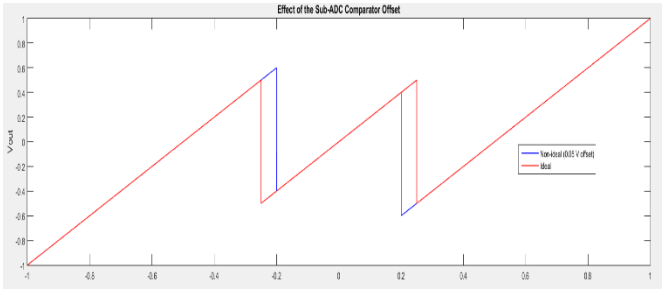


Fig. 9. The effect of the offset.

2) *Capacitor Mismatch:*

Capacitor ratio C_S/C_F gives the gain of multiplying-DAC. In the case of capacitors C_S and C_F are different, then this mismatch causes a proportional error relatedly in the residue output. Therefore, precise capacitor matching is expected in the design of a high-resolution pipeline ADC. In Fig. 10, the effect of the capacitor mismatch shown.

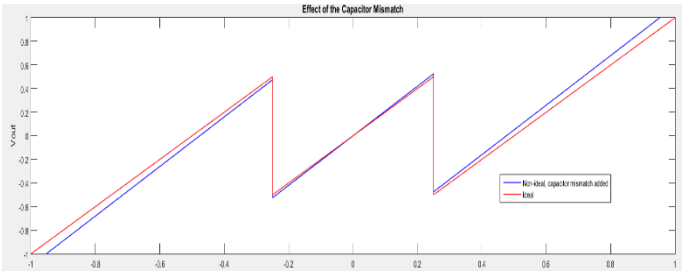


Fig. 10. The effect of the capacitor mismatch.

3) *Gain Error:*

As a vital analog structure, opamp has its importance for SC circuits. In the case of non-ideal measurement of ADCs, opamps are needed to be treated. Because in non-ideality, opamp has finite gain that causes such a case in the capacitor mismatch. Therefore, to obtain linearity, opamp gain should be large. In Fig. 11, effect of the gain error accordingly the ideal case is illustrated which is animated in Matlab.

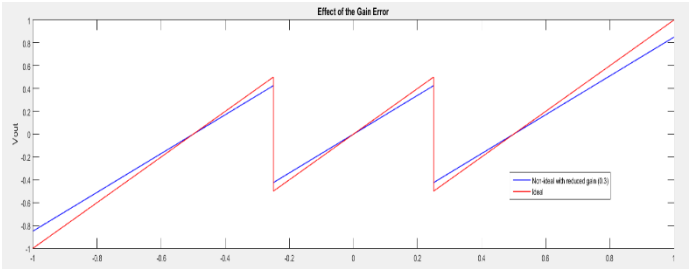


Fig. 11. Effect of the gain error accordingly the ideal case.

Moreover, there are some other non-ideal effects like thermal noise and clock jitter as He and Meng model them [10]. The thermal noise is usually modeled as an additive white noise source with Gaussian distribution. Fig. 12 presents the thermal noise model. It can be modeled as a random variable generator with zero-order block, and the gain block is used to adjust the value of the total thermal noise [11]. The clock jitter can be added into model as on the figure, too.

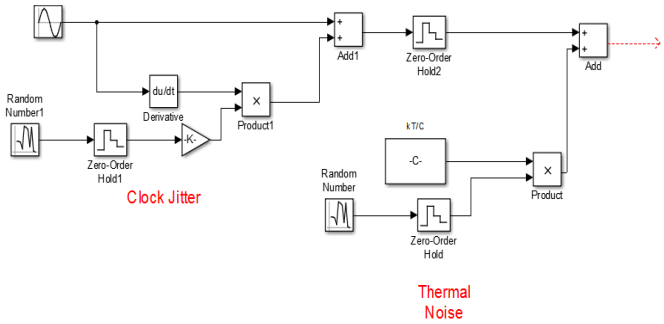


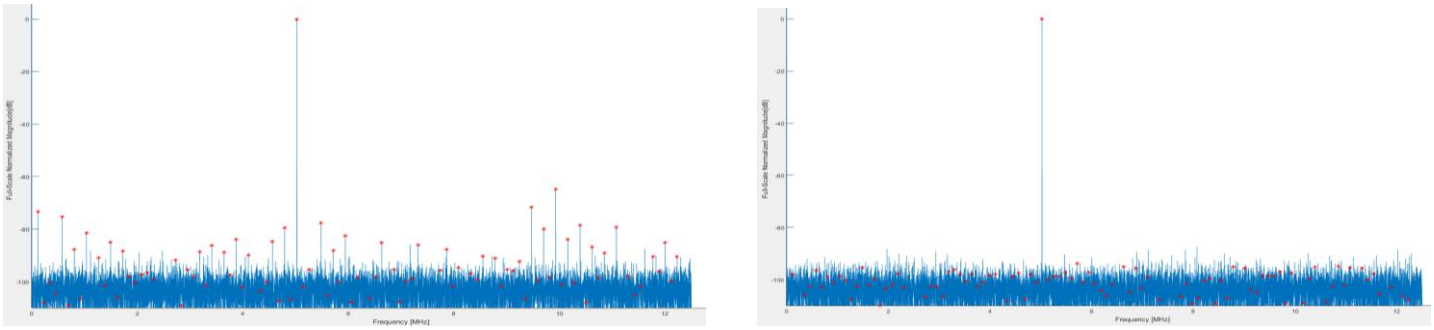
Fig. 12. Matlab implementation of clock jitter and thermal noise [10-11].

IV. Performance Aspects, Results And Conclusion

This paper is to construct an ADC, 12-bit, 1.5 bit per stage with a calibration. The design is in ideal and non-ideal conditions combining all together. Foreground calibration and the model on Matlab – Simulink related to pipeline ADC are constructed and analyzed in Matlab using Simulink block design. The results are presented with calibrated version and without any calibration. The behavioral modelling of the ADC is obtained but for the calibration check, the non-ideal sources must be entered. Therefore, previously non-idealities has been presented. After all, proposed calibration is applied to obtain several outputs. The difference between calibrated and non-calibrated cases differs first on the FFT related distortions and INL-DNL calculations which are shown in Fig. 13, 14 and 15 respectively. For the first, distortions, i.e. spikes are reduced and there become higher SNDR. Moreover, Effective Number of Bits (ENOB) is closer to 12 bits which is the main aim of this paper. Also, indicative enhancement is obtained on the INL, as shown in the following Table I.

TABLE I. RESULTS RELATED TO *WITH* AND *WITHOUT* CALIBRATION

Parameters	**Test Results**	
	Without Calibration	***With Calibration***
Fs	100 MS/s	100 MS/s
Fin	5.0 MHz	5.0 MHz
DNL	-0.53/+0.29 LSB	-0.31/+0.36 LSB
INL	- 1/+0.98 LSB	-0.2/+0.24 LSB
ENOB	9.3 Bits	11.2 Bits
SNR	60.5033 dB	69.8385 dB
SDR	62.1164 dB	79.9698 dB
SFDR	64.6948 dB	87.467 dB
SNDR	58.2251 dB	69.7858 dB



(a) (b)

Fig. 13. FFT analysis plots without calibration (a) and with calibration (b).

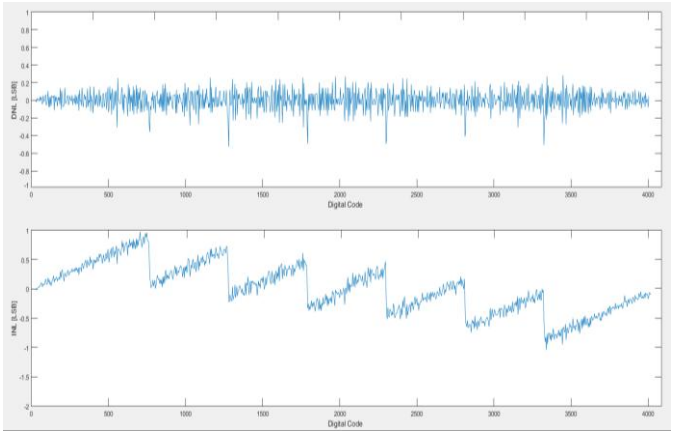


Fig. 14. DNL – INL plots without calibration.

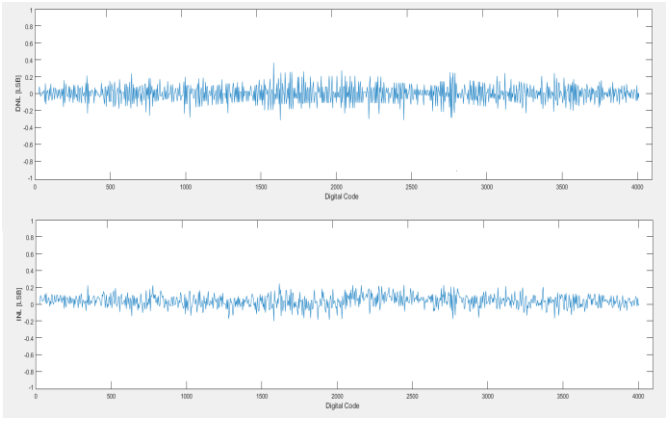


Fig. 15. DNL – INL plots with calibration.

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References

[1] L. Zhang, "The calibration technique for pipelined ADC," Intl. Conf. on Multimedia and Information Technology, China, 2008.

[2] J. Li and U. Moon, "Background calibration techniques for multistage pipelined ADCs with digital redundancy," *IEEE Transactions on Circuits snd Systems*, Vol. 50, No. 9, September 2003.

[3] Y. Chiu, C.W. Tsang, B. Nikolic, and P.R. Gray , "Least mean square adaptive digital background calibration of pipelined analog-to-digital converters," *IEEE Transactions on Circuits And Systems—I: Regular Papers*, vol. 51, no. 1, pp. 38-46, January, 2014.

[4] C. Tsang, "Digitally calibrated analog-to-digital converters in deep sub-micron CMOS," EECS Dept., Uni. of California, Berkeley PhD. thesis, 2008.

[5] M.H. Zarifi, A. Rostami, Z.D. KuzeKanani, and J. Sobhi, "A 12 bit, 80 Msamples/s, pipelined analog to digital converter," 5th Intl. Conf. on Electrical and Electronics Engineering, Bursa, 2007.

[6] I. Ahmed, "Pipelined ADC design and enhancement techniques", Springer Science & Business Media, Chapter 5, 2010.

[7] K. Javeed, "Digital gain error correction technique for 8-bit pipeline ADC", thesis, Dept. of Electrical Eng., Linköpings University, 2010.

[8] F. Maloberti, "Data converters", Springer US, 2007.

[9] V. Kledrowetz and J. Haze "Analysis of non-ideal effects of pipelined ADC by using MATLAB – Simulink", 3rd WSEAS Intl. Conf. on Advances in Sensors, Signals and Materials, pp.85-88, 2010.

[10] W.W. He and Q. Meng, "Behavioral modeling of a 12-bit 500-MS/s multi-stage ADC," PIERS Proceedings, Taipei, March, 2013.

[11] S. Hanfoug, N.E. Bouguechal, and S. Barra, "Behavioral non-ideal model of 8-bit current-mode successive approximation registers ADC by using Simulink," *Intl. J. of u- and e- Service, Science and Technology*, vol.7, no.3, pp.85-102, 2014.

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