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A New Generalized Asymmetrical Cascade Multilevel Inverter Topology with Reduced Power Electronic Switches and Dc Sources

G. Sridhar **P. Satishkumar** **M. Sushama**

Abstract-- ***In the past few years the demand for the achievements in development of multilevel inverter topologies has been increasing a lot. Recently presented topologies accomplish higher number output voltage levels with few number of switches, DC voltage sources, and reduced voltage stress across switches, with fewer losses as compared with conventional topologies. Minimization of switches and dc voltage sources reduces complexity, cost size and improves the overall performance. These benefits are proposed in this paper with a new topology of asymmetrical cascaded multilevel inverter. This developed structure provides reduced number of controlled switches, DC sources, as compared with conventional and presented topologies in the literature so far.***

The proposed asymmetrical topology generates seven voltage levels with eight switches only. Furthermore reduction in voltage stress across the switches can be attained. Phase Opposition Disposition (POD) is adopted for generating switching pulses. The proposed topology is simulated using MATLAB/SIMULINK and results have been validated experimentally.

Keywords: ***Asymmetrical multilevel inverter, reduction of Switches, dc voltage sources, POD.***

I. Introduction:

Introduction of multilevel inverter was done in 1975, since its introduction the demand in the field of DC/AC power conversion and associated applications has been increasing [1]. In the recent day MLI is gaining much fame in the field of Dc/AC conversion due to less THD, better power quality and good electromagnetic compatibility.

Even after having many merits MLI has few demerits that is to maximize output voltage levels semiconductor switch requirements with peripheral devices like protection circuits, gate driver circuits used extensively .Due to more device count the overall system becomes expensive ,stupendous and complicated and minimizes the quality and competency of the converter[2-11].

MLI are grouped into Cascaded H Bridge, Flying capacitor and Neutral point Clamped traditionally. In the recent past most of the published articles showed the study on NPC, FC and CHB topologies regarding their merits and demerits [12]. Among MLI topologies CHB is popular due its coherence and easy operation but the limitation of the topology is requirement of isolated dc power supplies [13]. CHB is arranged as asymmetric and symmetric configuration based on magnitude of the dc voltage sources. If V1=V2=V3… is symmetric vice versa. For the same number of power switches the symmetric configuration of CHB generates lesser number of voltage levels as compared with asymmetric configuration.

A combination of unidirectional and bidirectional switches of different ratings have been utilized with reduced device count have been offered by the large number of topologies and control schemes in the recent past [12-22]. The requirement of large number of bidirectional switches is a major issue in asymmetrical topologies. An effort has been attempted to reduce bidirectional switches in asymmetrical topology by proposing a new topology in this paper. The cost of the symmetrical topology MLI is less due to less different dc voltage sources but the major problem is its modularity [22].The topologies presented in [21-22], has the limitation that all the voltage levels (series/parallel) cannot be ascertained with the suggested algorithms.

In [21] topology of MLI constituted many bidirectional switches is presented. Owing to bidirectional switches, voltage stress over the switches and number of devices is more.

In this paper new topology of asymmetrical MLI is proposed. The proposed topology is capable of producing 7 output voltage levels by utilizing 8 controlled switches.. Experimental results as well as Simulation results are described for 7-level multi level inverter to verify the proposed topology.

II. Proposed Multilevel Inverter Topologies:

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The proposed topology shown in Figure1. The topology is composed with two dc voltage sources V1 and V2 along with polarity generation circuit ,it consist high frequency switches and should withstand to high switching frequency to produce required voltage levels and polarity conversion circuit ,is responsible for the conversion of the polarity of the output voltage, is the low frequency part operating at line frequency. In polarity generation four diodes D1-D4 are connected in anti parallel to avoid dead short circuit across the switches and dc voltage sources. When DC voltage sources unequal (V1≠V2) can be called as asymmetrical otherwise symmetrical. The presented topology can produce seven level output voltage with eight controlled switches only. Batteries, capacitors and isolated dc voltage supplies can be used as dc voltage sources in this topology. When ac voltage sources are available using rectifiers and isolated transformers multiple dc voltage sources can be produced. The problem of voltage balancing is eliminated by employing fixed dc voltage source. The proposed topology can be easily extended to three phase system .

When S3 switch is ON and S1, S2 are OFF dc voltage source V1 is connected in parallel to polarity generation circuit in the output, when S2 switch is ON dc voltage source V2 is connected to polarity generation circuit in the output. When switch S1 is ON the dc voltage sources are connected in series (V1+V2 voltage will appear across the output of polarity generation circuit) by flowing the current through S1. When switches S1, S2 and S3 are OFF and Sa is ON Zero voltage will appear across polarity generation circuit. Thus by using the above switching sequence four output voltage levels are achieved differently can be observes from Figure4.The arrangement of the basic cell for 16level output voltage shown in Figure2.The generalized structure of the proposed topology shown in figure3. To avoid the short circuit of the switches four diodes are connected in parallel to switch s2.The switching states of the proposed MLI with particular combination of the switches and corresponding voltage levels for 7level summarized in TableI

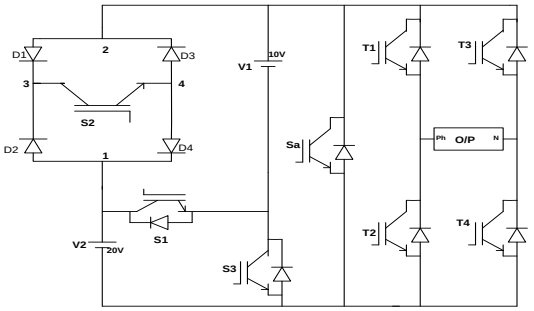

Figure2: Arrangement of Basic cell of the proposed Topology for 16Level Output voltage

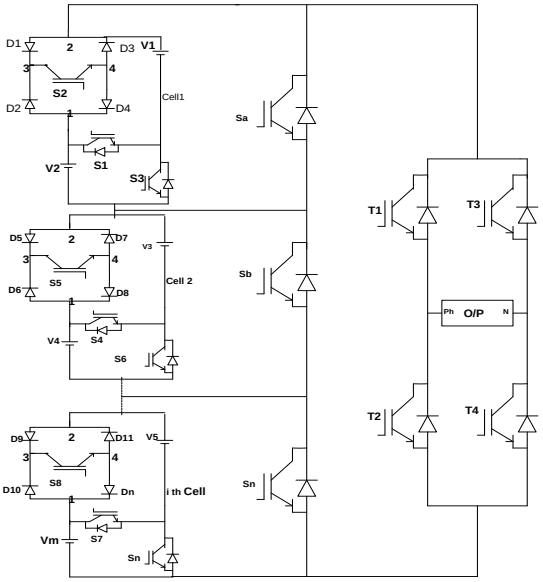

Figure3 .Generalized Structure of the proposed single Phase Topology

Figure1. Proposed Topology

Table I: Switching states of the Proposed Topology shown in Figure1

S.No	ON State Switches	Output Voltage
1	Sa	0
2	S3	V1
3	S2,D2,D3	V2
4	S1	V1+V2

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It is important to mention here that the power switches for the polarity generation part need to have a minimum voltage rating equal to the operating voltage of the MLI. Hence the H Bridge is used as polarity conversion circuit and switches of H Bridge must able to tolerate the voltage equal to rated output voltage of the MLI

These four switches of H Bridge turn ON and OFF once during a fundamental cycle, hence these four switches restrict for the application of high voltage. As the proposed topology facilitates cascade connection the basic cells that solve the above problem and reduce the voltage stress across the switches.

In the presented topology [16], while operating polarity generation circuit switches, the switches may undergo short circuit with connected dc voltage sources due to forward biased diodes, this makes huge circulating current will flow through the switches this leads to burning of the high frequency switches which increases the cost of the the inverter and reduces the reliability.

This problem can be overcome by the proposed topology .The anti parallel diodes connected across switch does not provide the closed path for the current to circulate through the high frequency switches. It is clearly observed from the Figure1 when switch S2 is OFF, either switch S1 or S3 is conducting D2,D3 or D1,D4are in reverse biased condition that will not allow the current through it.

The values of the dc voltage sources employed in the asymmetrical MLI are assumed differently in the different cells such that maximum output voltage levels can be produced using lesser switching devices.

In asymmetrical topology the dc voltage sources values are unequal. Based on above condition the below equations are obtained for 'm' basic units

$$\text{Nsource} = 2\text{m} \quad (1)$$

$$Nswitch = 2Nsource + 4 \quad (2)$$

$$Nlevel = 2^{Nsource} \quad (3)$$

Nsource, Nswitch, Nlevel are the number of dc voltage sources, number of switches and number of output voltage levels respectively

The magnitude of the dc voltage sources can be selected using following equation, For the m^{th} basic unit, The value of the n_{th} dc voltage source in m^{th} basic unit

$$Vdcm,n = 2^{(n-1)}Vdc \quad (4)$$

For basic unit 1 consisting of 2 voltage sources Vdc1&Vdc2 The maximum output voltage is obtained by the m^{th} Unit of the proposed topology can be determined as follows;

The Maxmum Output Voltage:

$$Vo\max = (2^{2m} - 1)Vdc \quad (5)$$

In designing the cascaded Multilevel Inverters, it is important to consider the standing voltage of the power electronic switches. It is defined as the maximum operating voltage that present across switches during each mode of operation.

The standing voltage of the switches in m^{th} cascaded multilevel inverter basic unit (Vsm) in asymmetrical condition can be written

$$Vsm = 4(V1,1 + V1,2 + V2,3 + V2,4 + ...Vnm) \quad (6)$$

From the equation (4) V1,1, V1,2…etc can be written as

V1,1=Vdc: V1,2=2Vdc: V2,3=4Vdc: 2,4=8Vdc…..

$$Vsm = 4(Vd + 2Vd + 4Vd + 8Vd + ...) \quad (7)$$

Therefore the sum of the standing voltage of the switches in m basic units consisting of n dc voltage sources equal to

$$Vsm = 4\sum_{m=1}^{n} Vmn \quad (8)$$

The asymmetrical topology consisting of n dc voltage sources the total standing voltage equal to

$$Vsn = 2* \sum_{n=1}^{j} 2^{n-1} Vdc \quad (9)$$

III. Modulation Schemes:

Carrier based multi carrier modulations methods namely phase disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD) have been employed widely for switching of multilevel inverters due to their less computational requirements, flexibility and simplicity . Alternative Phase Opposition Disposition (APOD) PWM technique is employed for generating switching pulses

Alternative Phase Opposition Disposition (APOD) PWM Method:

In this method each carrier is phase shifted by 180 degrees from its adjacent.

IV. Simulation Results:

The required switching pulses in proposed topology is generated using PD,POD and APOD pulse width modulation techniques for 7 level asymmetrical topology and simulated using MATLAB/Simulink and developed prototype hardware model .

The simulated results of output voltage and current of the proposed seven level asymmetrical MLI using Alternative phase opposition disposition (APOD) PWM shown in Figure4. Figure5. It can be observed that the output voltage and current is nearly sinusoidal. The FFT analysis of the voltage and current wave forms of the above PWM techniques shown in Figure6, Figure7.

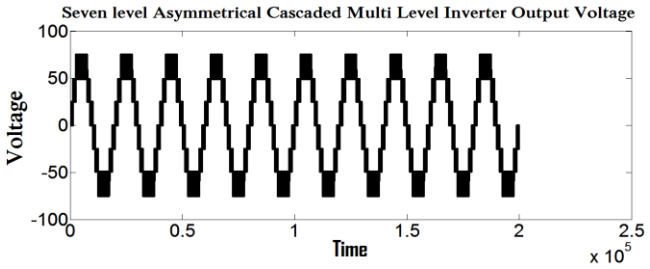


Figure4. Output Voltage of 7level Asymmetrical MLI of proposed topology using APODPWM

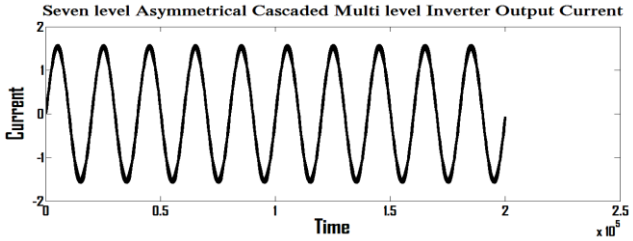


Figure5. Output Current of 7level Asymmetrical MLI of proposed topology using APODPWM

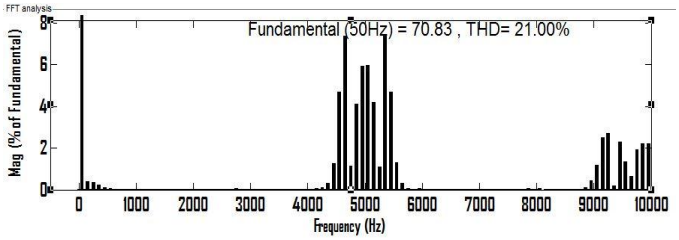


Figure6. Output Voltage THD of 7level Asymmetrical MLI of proposed topology using APOD PWM

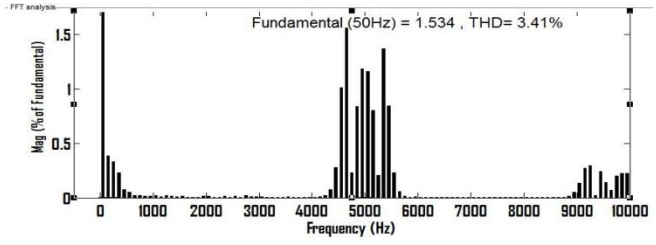
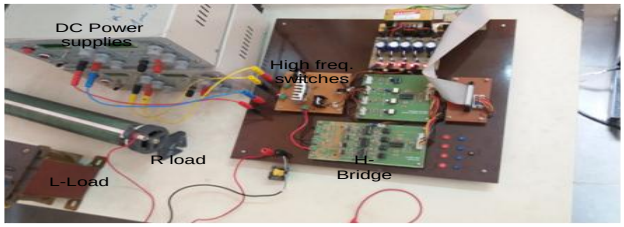


Figure7. Output Current THD of 7level Asymmetrical MLI of proposed topology using APOD PWM

V. Experimental Results:

To approve and ensure the concept and feasibility of the proposed asymmetrical topology experimental setup has been prepared for 7 levels of output voltage and validated experimentally with R-L load (R=50Ω and L=55mH) shown in Figure8. Switching pulses for H Bridge (T1 & T2) , for high frequency switches (S1, S2&S3) are generated using Alternative Phase Opposition Disposition (APOD) pulse width modulation technique.

The experimentally obtained voltage and current wave forms of the proposed 7level asymmetrical topology using APOD PWM technique are shown in Figure9, Figure10 .



Hardware implementation of proposed 7level asymmetric MLI

Figure8.Experimental circuit of Proposed 7level asymmetrical MLI with proposed topology

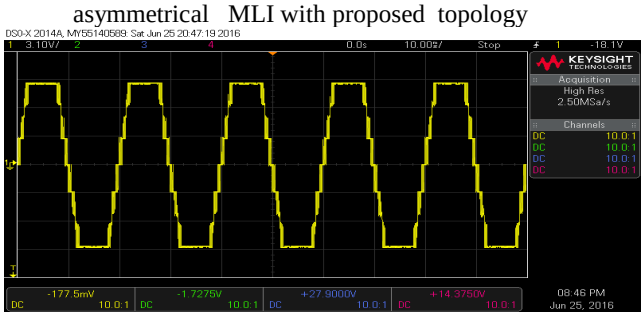


Figure9. Proposed 7level asymmetrical topology Voltage waveforms using APOD PWM

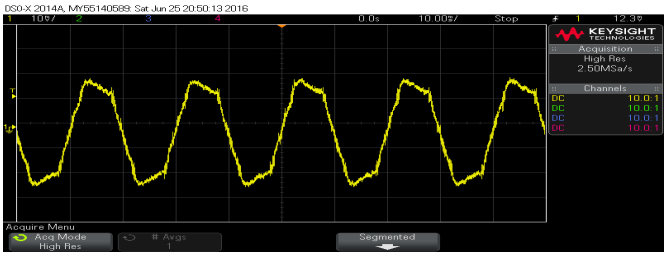


Figure10. Proposed 7level asymmetrical topology Current waveforms using APOD PWM

TableII. Comparison of Total Harmonic Distortion

Simulation	V_{THD}	I_{THD}
	21.07	3.42
Experimental	4.01	8.33

Conclusion:

In this paper a new generalized topology for asymmetrical multilevel inverter that works on the base of the series connection of the dc voltage sources was proposed. In the proposed topology the basic cell is connected in such way that the maximum number of voltage levels is attained. Algorithms were proposed for the magnitude of the dc voltage sources, number of voltage levels attained, number of switches required and maximum value of the output voltages. A 7level asymmetrical MLI prototype hard ware implemented to verify the ability of the proposed topology.

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