International Journal of Advancements in Electronics & Electrical Engineering– IJAEEE 2018
Copyright © Institute of Research Engineers and Doctors , SEEK Digital Library
Volume 6 : Issue 2 [ISSN : 2319-7498] - Publication Date: 25 June , 2018

Analysis of Level Shifted Modulation Strategies Applied to Cascaded H-Bridge Multi-Level Inverter Fed Induction Motor Drive

Ravi kumar Bhukya, P. Satish kumar, E. Sreenu

***Abstract*—This paper presents various level shifted multi carrier PWM techniques such as PD,POD and APOD for a cascaded H-Bridge multi level inverter fed induction motor drives. The performance analysis of these modulation strategies are analyzed by apply for five level, seven level, nine level and eleven level inverter. The performance analysis of cascaded H-Bridge interms of line voltage, stator current, speed, torque and total harmonic distortion. The results are depicting that PD-PWM is more effective among the three proposed PWM techniques. The proposed technique has been simulated using MATLAB/SIMULINK software. These Level shifted PWM techniques can be applied to N-level cascaded Inverter also.**

***Keywords*—Cascaded multi-level inverter, Level shifted multi carrier PWM, Variable speed control of induction motor, THD**

I. Introduction

The speed control of induction motors is done by the most common method called V/f control. A drive is required to do the task of speed control efficiently. Variable speed ac machine is equipped with an adjustable voltage or frequency drive called power electronic drive for speed control of electric machines (1) Cascade h-bridge Multi-level inverter is the most prominent topology when high number of output voltage levels are required compared to Diode clamped ML inverter (2). With the development in power electronic switches and low cost computational hardware ac induction motor drives now compare favorably to DC motors on considerations such as power to weight ratio, acceleration performance, maintenance, operating environment, and higher operating speed without the mechanical commutator, cost and robustness of the machine, and perhaps control flexibility are often reasons for choosing induction machine drivers in small to medium power range applications (3).

Ravi kumar Bhukya
line 1 Department of Electrical Engineering
line 2: University College of Engineering
line 3: Osmania University
line 4: Hyderabad, Telangana, INDIA
line 5: Rkpurnanaik2014@gmail.com

P.Satish kumar
line 1 Department of Electrical Engineering
line 2: University College of Engineering
line 3: Osmania University
line 4: Hyderabad, Telangana, INDIA
line 5: Satish_8020@yahoo.co.in

E.Sreenu
line 1 Department of Electrical Engineering
line 2: University College of Engineering
line 3: Osmania University
line 4: Hyderabad, Telangana, INDIA
line 5: Ssspawar@yahoo.com

Up to date, due to the improvement of fast-switching power semiconductor devices and machine control algorithm, more precise PWM (Pulse Width Modulation) method finds particularly growing interest (4).An induction motor being an asynchronous machine preferred in most of the industrial applications for its variable speed characteristics. In this aspect, compared with any other PWM method for the voltage source inverter, the PWM method based on voltage level shifted pulse width modulation results in excellent dc bus utilization(5).

In this paper Level shifted multi-carrier PWM modulation strategies most commonly used for CHB multi-level inverters are investigated on five-level, seven-level, nine-level and eleven-level cascade h-bridge multi-level inverter fed induction motor for variable speed control application using matlab simulation implementation so as to have comparative analysis in terms of output line voltages per phase.

II. Level Shifted Carrier Pulse Width Modulation Strategies

Maximum the modulation procedures developed for multilevel inverters are built on carrier arrangements. Carrier are organized with level shift (PDC-PWM, PODC-PWM,APODC-PWM), or phase shift(PSC-PWM).

A. *Phase disposition Carrier PWM*

Phase disposition carrier PWM, its called PDC-PWM, whose all carriers are in phase with each other as show in Fig. 1.This strategy gives the lowest total harmonic distortion (THD) for the line to line voltage.

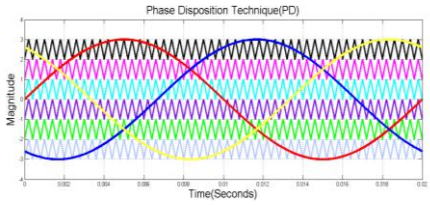

Figure 1. Reference sine and tringular carriers of seven level cascaded inverter (PDC-PWM).

B. *Alternative Phase Opposition disposition Carrier PWM*

Alternative Phase opposition disposition carrier PWM, it's called APODC-PWM, in which each carrier is phase shifted by 180^0 from its neighboring carrier as shown in Fig. 2.

International Journal of Advancements in Electronics & Electrical Engineering– IJAEEE 2018
Copyright © Institute of Research Engineers and Doctors , SEEK Digital Library
Volume 6 : Issue 2 [ISSN : 2319-7498] - Publication Date: 25 June , 2018

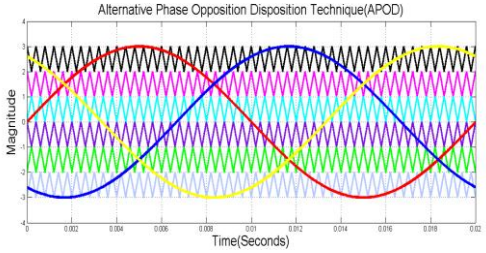

Figure 2. Reference sine and tringular carriers of seven level cascaded inverter (APODC-PWM).

C. *Phase Opposition disposition Carrier PWM*

Phase opposition disposition carrier PWM, its called PODC-PWM, bit similar to APODC-PWM but carriers above the sinusoidal reference zero point are 180^0 out of phase with those bellow the reference zero point as shown in Fig. 3.

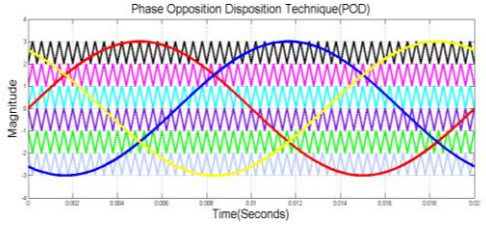

Figure 3. Reference sine and tringular carriers of seven level cascaded inverter (PODC-PWM).

III. The Proposed Closed Loop Cascaded Inverter Fed Induction Motor

A speed sensor or a shaft position encoder is used to obtain the actual speed of the motor. It is then compared to a reference speed. The difference between the two generates an error and the error so obtained is processed in a Proportional controller and its output sets the inverter frequency. Fig. 4.indicates V/F control of induction motor.

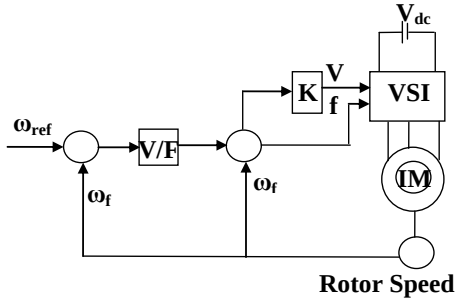

Figure 4. Block diagram for closed V/F control on three phase induction motor

. For a three-phase induction motor, stator voltage per phase is given by equation(1) that the ratio of supply voltage V_1 to supply frequency f_1 is kept consant, the air-gap flux ϕ remains constant. The starting torque given by equation (2) and The maximum torque is given by ω_1 (3).

$$T_{e,st} = \frac{3}{\omega_s} \times \frac{V1^2}{(r1+r2)^2 + (x1+x2)^2} \times r^2 \quad (1)$$

$$T_{e,st} = \frac{3p}{2\omega 1} \times \frac{V1^2}{\omega 1^2} \times \frac{r^2}{(l1+l2)^2} \quad (2)$$

$$T_{e,m} = \frac{3p}{4} \times \frac{V1^2}{\omega 1^2} \times \frac{1}{(l1+l2)} \quad (3)$$

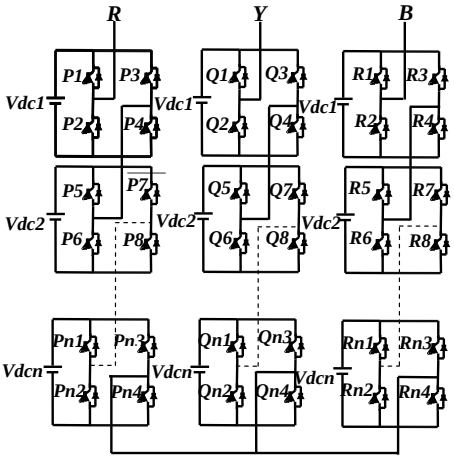

Figure 5. Three phase N-level cascaded inverter

Fig. 5. shows the power circuit for three phase N- level cascaded h-bridge multilevel inverter. the final phase voltage is the addition of voltages produced by the different cells in that phase. N-voltages is produced by each single H-bridge in a phase . the phase voltage consists of N-level inverter. the levels in phase voltage are 2N+1, here N is 1-ϕ inverter cells present in a phase and the number of levels in line voltage are 2M-1, where M is the number of level in phase voltage.the output voltage of the single h-bridge inverter in equation (4).

$$V_{O1} = V_{dc1} + V_{dc2} + \ldots\ldots\ldots + V_{dcn} \quad (4)$$

IV. Simulation Results

The system parameters of the induction motor show in Table. 1.

TABLE I. SYSTEM PARAMETER OF THE INDUCTION MOTOR

S.No	**System Parameters**	
	Parameters	***Readings***
1	Supply Voltage	410V RMS(Phase-Phase)
2	H-Bridge Inverter dc voltage	100V
3	Rotor speed	1440 RPM
4	Fundamental frequency	50Hz
5	Switching frequency	1kHz

A. *Five level cascaded inverter*

Fig. 6.indictes the output line voltages of the five level inverter and Fig. 7.,Fig. 8.and Fig. 9.show the harmonic spectrum for the PD, POD and APOD inverter output

voltages. Fig. 10. and Fig. 11.show the varation of stator current, torque and speed of the motor.

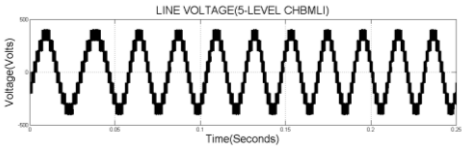

Figure 6. Five level cascaded inverter line voltage

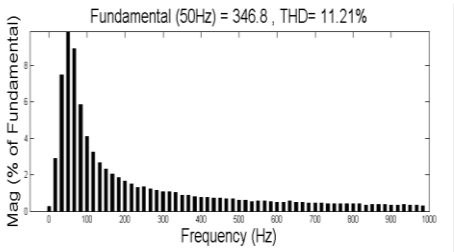

Figure 7. THD for five level inverter(PDC-PWM)

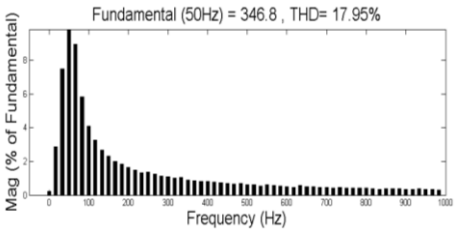

Figure 8. THD for five level inverter(PODC-PWM)

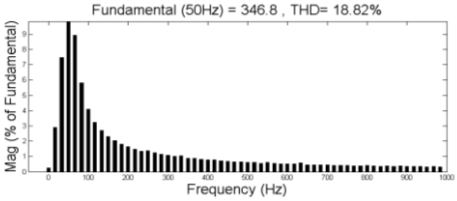

Figure 9. THD for five level inverter(APODC-PWM)

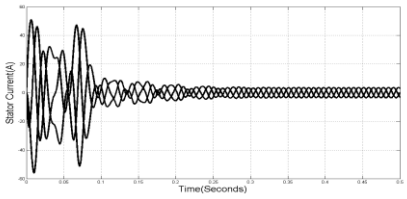

Figure 10. Three phase stator currents for five level inverter

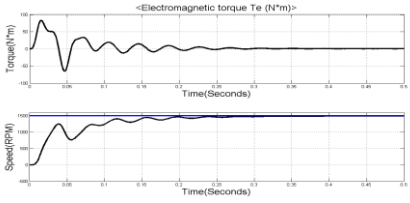

Figure 11. Torque and speed for five level inverter

B. *Seven level cascaded inverter*

Fig. 12.indictes the output line voltages of the seven level inverter and Fig. 13.,Fig. 14. and Fig. 15.show the harmonic spectrum for the PD, POD, and APOD inverter output voltages. Fig. 16. and Fig. 17.show the varation of stator current, torque and speed of the motor.

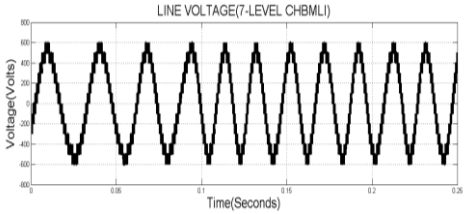

Figure 12. Seven level cascaded inverter line voltage

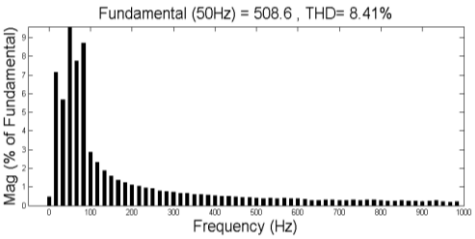

Figure 13. THD for Seven level inverter(PDC-PWM)

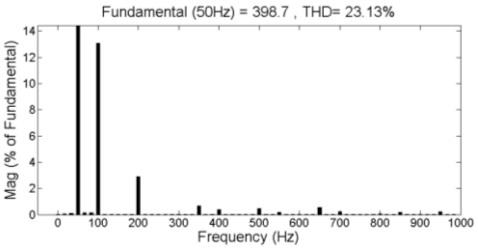

Figure 14. THD for Seven level inverter(PODC-PWM)

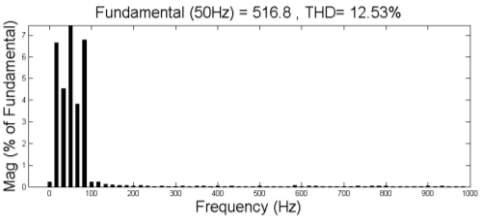

Figure 15. THD for Seven level inverter(APODC-PWM)

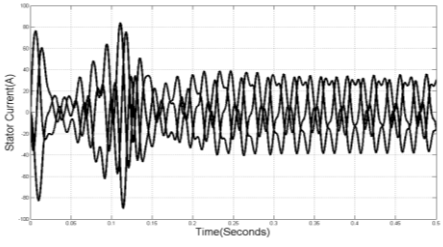

Figure 16. Three phase stator currents for Seven level inverter

International Journal of Advancements in Electronics & Electrical Engineering– IJAEEE 2018
Copyright © Institute of Research Engineers and Doctors , SEEK Digital Library
Volume 6 : Issue 2 [ISSN : 2319-7498] - Publication Date: 25 June , 2018

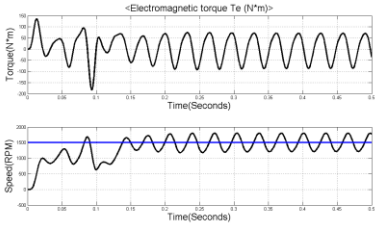

Figure 17. Torque and speed for Seven level inverter

C. *Nine level cascaded inverter*

Fig. 18.indictes the output line voltages of the seven level inverter and Fig. 19.,Fig. 20. and Fig. 21.show the harmonic spectrum for the PD, POD, and APOD inverter output voltages. Fig. 22. and Fig. 23.show the varation of stator current, torque and speed of the motor.

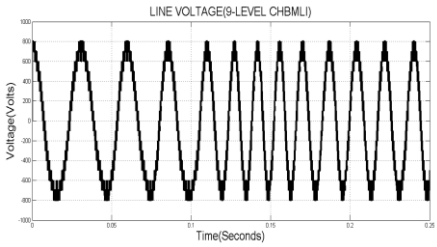

Figure 18. Nine level inverter line voltage

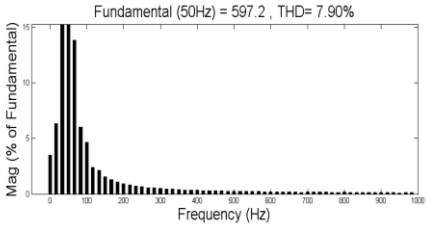

Figure 19. THD for nine level inverter(PDC-PWM)

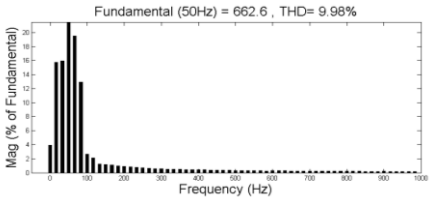

Figure 20. THD for nine level inverter(PODC-PWM)

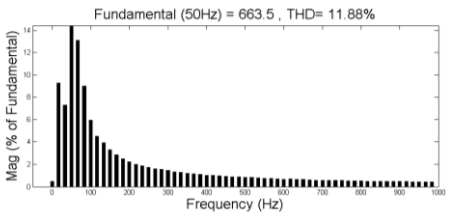

Figure 21. THD for nine level inverter(APODC-PWM)

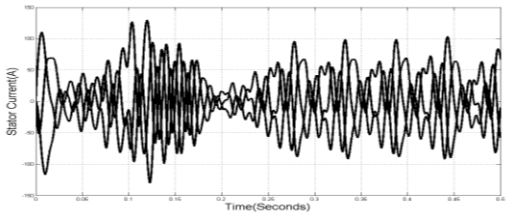

Figure 22. Three phase stator currents for nine level inverter

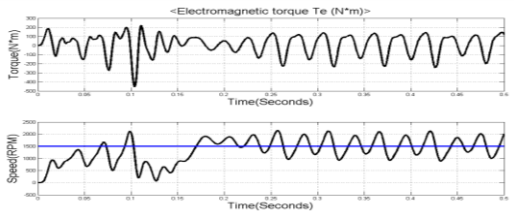

Figure 23. Torque and speed for nine level inverter

D. *Eleven level cascaded inverter*

Figure 24.indictes the output line voltages of the seven level inverter and Fig. 25.,Fig. 26. and Fig. 27.show the harmonic spectrum for the PD, POD, and APOD inverter output voltages. Fig. 28. and Fig. 29.show the varation of stator current, torque and speed of the motor.

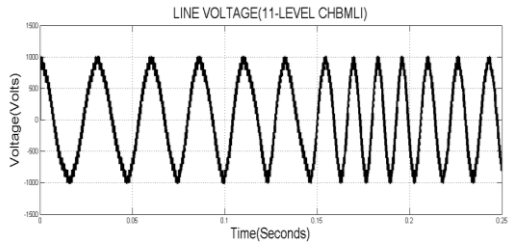

Figure 24. Eleven level inverter line voltage

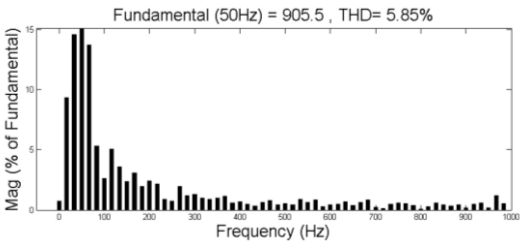

Figure 25. THD for eleven level inverter(PDC-PWM)

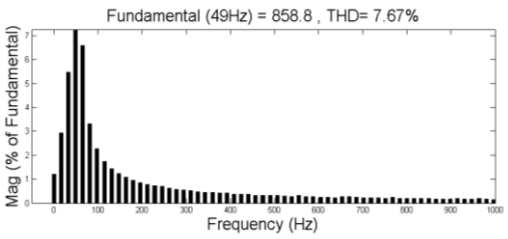

Figure 26. THD for eleven level inverter(PODC-PWM)

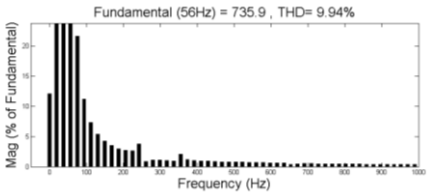

Figure 27. THD for eleven level inverter(APODC-PWM)

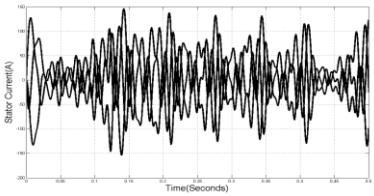

Figure 28. Three phase currents for eleven level inverter

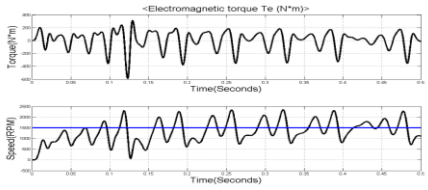

Figure 29. Torque and speed for eleven level inverter

The total harmonic distortion of the output voltage is 5.85%(Low) when using PD-PWM technique on Eleven-level cascaded multi-level inverter. And can observe the output stator current and torque, variations speed(actual speed and reference speed) of the load of five-level,seven-level,nine-level and eleven-level inverter.The Comparison of THD analysis of a three-phase five-Level, seven-level, nine-level and eleven-level CHBMLI shown in Table 2.

TABLE II. COMPARISION OF THD FOR INVERTER(FIVE,SEVEN,NINE AND ELEVEN)

Output voltage level	**PWM Techniques**		
	PD(%THD)	***POD(%THD)***	***APOD(%THD)***
Five-level	11.21	17.95	18.82
Seven-level	8.41	12.52	12.53
Nine-level	7.90	9.98	11.88
Eleven-level	5.85	7.67	9.94

v. Conclusion

In this paper various level shifted multi-carrier PWM techniques such as Phase disposition, Alternative Phase of disposition and Phase opposition disposition have used to control the switches of five-level, seven-level, nine-level and eleven-level cascaded multilevel inverter fed to induction motor for operating it in different speeds. The LSC-PWM techniques offers better harmonic reduction, fast switching frequency and better utilization of DC link compared to other modulation technique. The THD analysis, line voltages, stator currents and speed and torque of the machine are calibrated and compared confirming the good-quality waveforms.

Acknowledgment

We thank the University Grants Commission (UGC), Govt. of India, NewDelhi for providing Major Research Project to carry out the Research work on Multi-Level Inverters.

References

[1] M. Calais, L.J. Borle, V.G. Agelidis, “Analysis of multicarrier PWM methods for a single-phase five level inverter,” IEEE Power Electronics Specialists Conference (PESC), 2001, Vol. 3, pp. 1351-1356.

[2] E. Babaei, E. Ebrahimi, “Development of multi-carrier-PWM modulation for THD reduction and improvement of harmonics spectrum in multilevel inverters,” 24th International Power System Conference (PSC), Tehran, Iran, 2009, (in Persian).

[3] R.Linga Swamy,P.Satish Kumar,”Speed control of space vector modulated inverter driven induction motor”Proceedings of the International MultiConference of Engineers and Computer Scientists 2008 Vol II IMECS 2008, 19-21 March, 2008, Hong Kong.

[4] J.Rodriguez, S.Bernet, B.Wu, J.O.Pontt, and S.Kouro, “Multilevel voltage-source-converter topologies for industrial medium-voltage drives,” IEEE Trans.Ind.Electron., vol.54, no.6,pp.2930-2945, Dec.2007.

[5] P.W.Hammond, “ A new approach to enhance power quality for medium voltage AC drives,” IEEE Trans. Ind.Appl., vol.33, no.1, pp.202-208, Jan./Feb. 1997.

About Author (s):

Ravi Kumar Bhukya was born in Warangal, Telangana, India. He obtained B.Tech. in Electrical and Electronics Engineering from JNTU University, Hyderabad in 2010 and M.Tech. in Power and induristal drives Engineering in 2013 from Jawaharlal Nehru Technological University, Hyderabad. His research interests include Power Electronics Drives and Multilevel inverters. Presently he is pursuing Ph. D. in OU.

P. Satish Kumar was born in Karimnagar, Telangana, India. He obtained B.Tech. in Electrical and Electronics Engineering from JNTU College of Engineering, Kakinada, India in 1996. He obtained M.Tech. in Power Electronics in 2003 and Ph.D. in 2011 from Jawaharlal Nehru Technological University, Hyderabad. He has more than 21 years of teaching experience and at present he is an Assistant Professor in the Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad, India. His research interests include Power Electronics, Special machines and Drives and Multilevel inverters and guiding eight research scholars.

E.Sreenu was born in khammam, Telangana, India. He obtained B.Tech. in Electrical and Electronics Engineering from JNTU University, Hyderabad in 2003 and M.Tech. in Power electronics engnieering in 2006 from Jawaharlal Nehru Technological University, Hyderabad. His research interests include Power Electronics Drives and Multilevel inverters.