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2RC ADC for Massive Analog Signal Acquisition

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***Abstract*—There are applications that demand the simultaneous acquisition of a very large number of analog signals. This is the case when digital electronics circuits are connected to neural systems at very low level. In this paper, an ADC implemented with only two external resistors and one capacitor is presented. A description of this circuit is provided, including a detailed mathematical analysis of the behavior and its limitations. A circuit design procedure is applied to a real case using discrete components, and it is validated via simulation to demonstrate its performance.**

Keywords—ADC, biological interfaces, FPGA, programmable devices.

I. Introduction

The development of large programmable device such as FPGA has allowed the massive processing of digital data. These digital processors have hundreds of I/O digital pads for its external interconnection. However, these devices seldom include ADC in its core, and if so, the number of these converters is several order of magnitude lower than the number of gates that are integrated.

There are applications that demand the simultaneous acquisition of a very large number of analog signals. This is the case when digital electronics circuits are connected to natural systems at very low level, requiring a complex analog interface to massively translate biological signals into digital ones. A very clear example is the study of mammalian neural networks. In this case, a very large set of electrodes (MEA) have an intracellular or extracellular connection with the cells and capture their voltage potentials [1].

Although the use of fast and/or accurate ADCs is mandatory in many applications, when dealing with biological interfaces, it is often unnecessary. In this kind of applications, the number of captured signals is more important than the quality or speed of the A/D conversions, as they are relatively slow and only qualitative information is needed. For these reasons, a compact ADC is needed when massively connecting digital devices to such Biosystems.

In other application fields, such as in space, robustness is a must, and therefore minimal implementations are valuable.

Several already proposed schemes includes an external analog comparator or the use of stochastic logic for the implementation of an ADC [2].

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In this paper, an ADC implemented only two external resistors and one capacitor is presented. In next sections, a description of this circuit is provided, including a detailed mathematical analysis of the behavior and limitations. A circuit design procedure is applied to a case using discrete components, and it is validated via simulation and experimentation to demonstrate its performance.

II. 2RC ADC

A. *Circuit description*

The proposed 2RC ADC only uses two resistors and one capacitor as presented in Fig. 1. The principle of functioning is similar to a one-slope ADC [3].

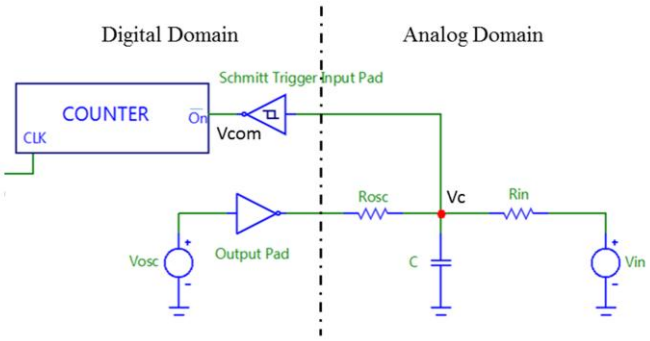


Figure 1. 2RC ADC Scheme.

A digital oscillator generates a square waveform with a fixed frequency f_{osc}. This digital signal is combined with the input voltage V_{in} to be converted, by using R_{osc} and R_{in}. The resulting voltage is integrated by capacitor C, whose voltage V_c is applied to a digital input pad. When the voltage V_c is above the threshold voltage of the input pad, V_{con} becomes a high level signal. Notice that the higher V_{in}, the longer the time that V_c will be above the gate threshold, and therefore the V_{com} pulse will be longer. This pulse will activate a counter, that will provide a digital representation of V_{in} when it stops.

If just an inverter gate is used as an input pad, it may oscillate due to the application of a continuous input voltage that is close to the unique threshold value for 0 to 1 and 1 to 0 transitions. This is why it is advisable to use a Schmitt Trigger inverter as an input pad. From now on, V_H and V_h will represent the low to high and high to low threshold voltages of the input pad that performs the comparison, respectively.

B. *Mathematical modelling*

The waveforms generated by the proposed circuit are depicted in Fig. 2. When V_{osc} is high or low, the capacitor is charged or discharged with a maximum or minimum

voltages given by the Thevenin voltages of the respective equivalent circuits connected to the capacitor.

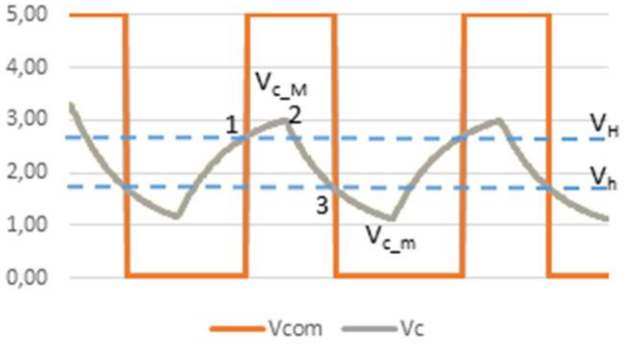


Figure 2. Waveforms generated in the 2RC ADC.

In what follows, it is assumed that R_{in}=R_{osc}=R and T_{osc} is the period of V_{osc}.

In general, the capacitor voltage V_c at time t, starting from an initial voltage (V_o), is given by:

$$V_c(t) = V_{th} + (V_o - V_{th})\, e^{-\frac{t}{R_{th}C}} \quad (1)$$

where R_{th} is the Thevenin equivalent resistance, which in our case is

$$R_{th} = \frac{R}{2} \quad (2)$$

and V_{th} depends on the digital output value V_{osc} according to (3).

$$V_{th} = \begin{cases} V_{th1} = \frac{V_{cc}+V_i}{2} & \text{when Vosc} = 1 \\ V_{th0} = \frac{V_i}{2} & \text{when Vosc} = 0 \end{cases} \quad (3)$$

But these limits are never reached because V_{osc} commutes before. V_c maximum and minimum voltages are called V_{c_M} and V_{c_m}. By analyzing these charge/discharge processes, it can be deduced that:

$$V_{c\_M} = \frac{1-E}{1-E^2}(V_{th1} + E\, V_{th0}) \quad (4)$$

$$V_{c\_m} = \frac{1-E}{1-E^2}(V_{th0} + E\, V_{th1}) \quad (5)$$

with

$$E = e^{-\frac{T_{osc}}{RC}} \quad (6)$$

Given R, C and T_{osc}, this waveform can be regarded as a pseudo-triangle signal, whose mean level depends on V_{th}, and subsequently on V_{in}.

The V_c signal is then processed by a Schmitt Trigger inverter input gate (74HC14), whose input impedance effect is neglected in this analysis. When V_c is above V_H, the input is considered to by high so the gate generates a low value, activating the counter that is initially reset. V_c is above V_H from 1 to 2, and from 2 to 3 in Fig. 2. By applying (1), the total time T_{on} when the counter is active can be deduced:

$$T_{on} = t_{1\to2} + t_{2\to3} \quad (7)$$

$$t_{1\to2} = \frac{RC}{2}\ln\left(\frac{V_H - V_{th1}}{V_{c\_M} - V_{th1}}\right) \quad (8)$$

$$t_{2\to3} = \frac{RC}{2}\ln\left(\frac{V_{c\_M} - V_{th0}}{V_h - V_{th0}}\right) \quad (9)$$

$$T_{on} = \frac{RC}{2}\ln\left[\frac{(2\,V_H - V_{cc} - V_i)}{(2\,V_h - V_i)}\frac{(2\,V_{cM} - V_i)}{(2\,V_{cM} - V_{cc} - V_i)}\right] \quad (10)$$

and the final count N, i.e. the ADC conversion value, is given by:

$$N(V_i) = \frac{T_{on}}{T_{clk}} \quad (11)$$

where T_{clk} is the period of the clock signal of the counter, which performs the analog to digital conversion.

The conversion time of this AD is

$$T_{conv} = 2 * T_{osc} \quad (12)$$

Unfortunately, as it can be seen in Fig. 3 as an example (R=10KΩ, C=20nF, T_{osc}=400us, T_{clk}=50ns, V_H=2.7V, and V_h=1.7V), this transfer function is clearly nonlinear, due to the inherent exponential behavior of the proposed circuit.

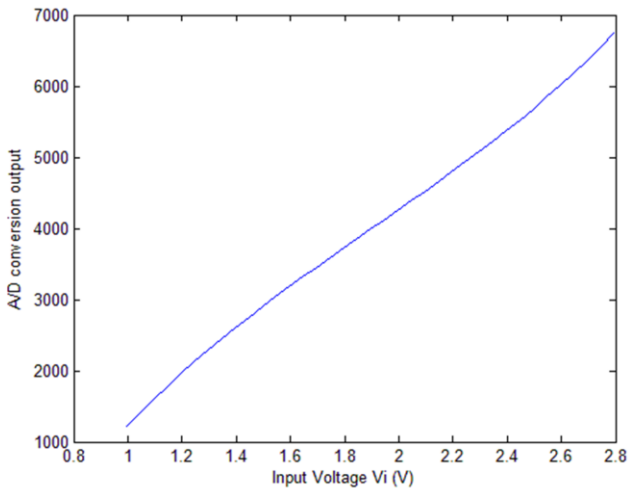


Figure 3. Transfer function of the proposed 2RC ADC for R=10KΩ, C=20nF, T_{osc}=400us, T_{clk}=50ns, V_H=2.7V, and V_h=1.7V.

C. *2RC ADC limitations*

To guarantee the correct functioning of this circuit, the maximum value of V_c must be higher than V_H and its minimum value lower than V_h. These relationships can be graphically represented as in Fig. 4. These constraints can be mathematically expressed as:

$$\left.\begin{matrix} V_{c\_M} > V_H \\ V_{c\_m} < V_h \end{matrix}\right\} \quad (13)$$

and by substituting (4) and (5) in (13), the limits given in (14) are obtained.

$$2V_h - \frac{E}{1+E}V_{cc} > V_i > 2V_H - \frac{1}{1+E}V_{cc} \qquad (14)$$

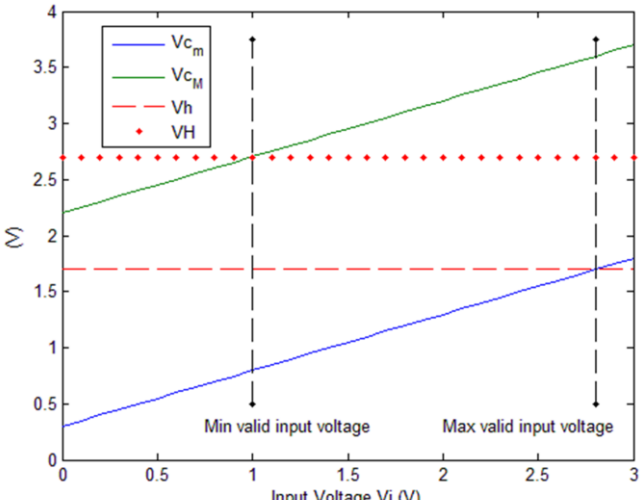


Figure 4. Representation of the maximum and minimum voltages of the capacitor as a function of Vi and the thresholds voltages of the input pad, for the given example.

The maximum and minimum limits given in (14) determines the valid input voltages that can be converted. These limits depend on the RC to T_{osc} ratio as it can be seen in Fig. 5. It is clear that, for low RC/T_{osc}, the ADC increases its input voltage range, with an optimum value about 0.1. For this value, the valid input voltage range is [0.4V, 3.4V]. Although this input voltage range is a limitation in the use of this converter, an input voltage reference can be added as an offset, having a total minimum input voltage above the lower limit of the converter input.

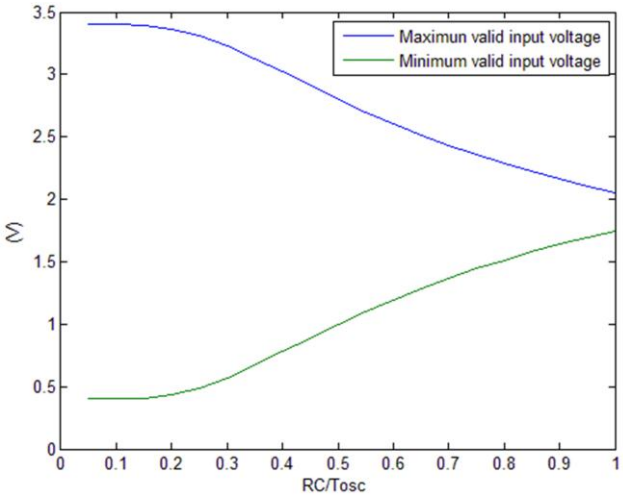


Figure 5. Dependence of the valid input voltage (Vi) range that can be converted, depending on the RC to Tosc ratio (VH=2.7V, and Vh=1.7V).

On the other hand, if we reduce the RC/T_{osc} ratio, the nonlinearity of the transfer function increases, as it is shown in Fig. 6.

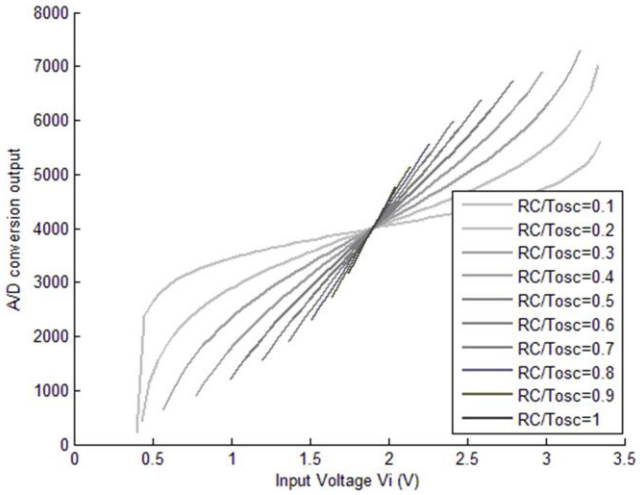


Figure 6. 2RC ADC Transfer functions depending on the RC to Tosc ratio for (VH=2.7V, and Vh=1.7V), represented only for the corresponding valid input voltage (Vi) range.

As a conclusion, the RC to T_{osc} ratio shall be chosen to have a good balance between input voltage range and the linearity of the transfer function. And finally, the residual nonlinearity can be compensated by applying the inverse of the transfer function or a look-up table.

D. *Design Criteria*

In order to facilitate the design of the 2RC ADC for a specific technology, the following procedure is suggested:

a) Use the minimum T_{clk} supported by the digital counter.

b) Choose the number of bits n for the resolution of the converter.

c) Calculate $T_{osc\ (min)} = 2^n T_{clk}$. The conversion time is $T_{con} = 2*T_{osc}$.

d) Select RC/T_{osc} as a tradeoff between input voltage range and linearity. Calculate RC.

e) Determine R to have a desired input impedance for the 2R ADC. Notice that a larger R will force a smaller C, reducing the signal to noise ratio of the circuit.

As an example, the implementation of a 2RC ADC based on the 74HC14 Schmitt Trigger inverter is considered. This technology has the following electrical characteristics: V_{cc}=5V, V_H=2.7V, V_h=1.7V. As this gate has a maximum time delay of 17ns, we will use T_{clk}=50ns. If n=12 bit is used, $T_{osc(min)} = 2^n T_{clk}$ = 204.8 us, so T_{osc}=400us is chosen. The conversion time for this converter is $T_{conv} = 2*T_{osc}$=800us.

If we want to have an acceptable input voltage range with a good linear transfer function, then $RC/T_{osc}=0.5$ is a good choice according to Fig. 5 and Fig. 6. And finally, for an input resistance of R=10KΩ, we deduce C=20nF.

Figure 7. Schematic for the simulation of the 2RC ADC (for R=10KΩ, C=20nF, Tosc=400us, Tclk=50ns, VH=2.7V, and Vh=1.7V.)

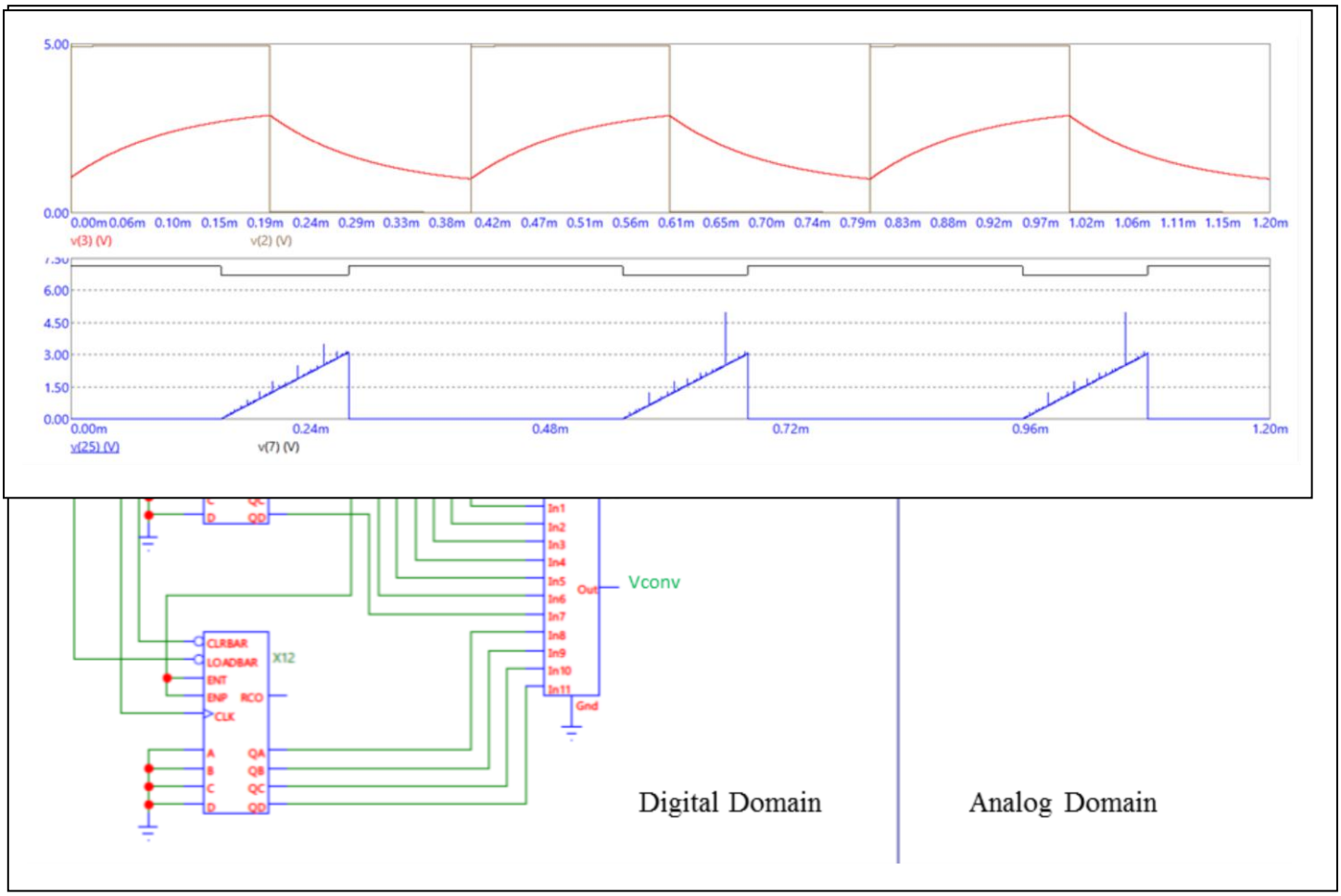
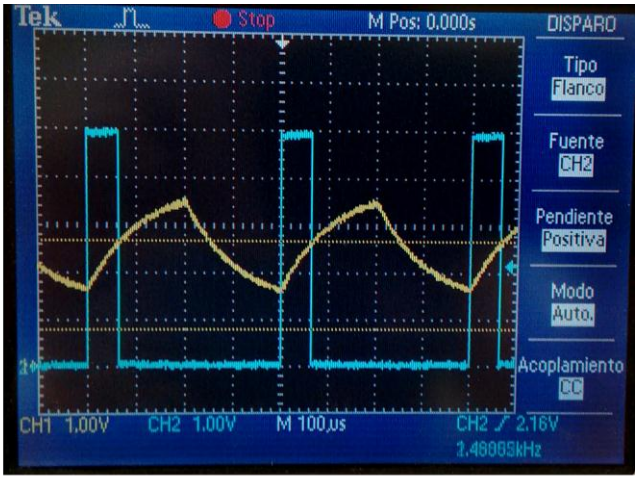


Figure 8. Simulation results for the 2RC ADC, with V(3)=Vc, V(2)=Vosc, V(7)=Vcom and V(25)=Vconv

III. Results

A. *Simulations*

In order to demonstrate the behavior of this converter, it has been implemented in Micro-cap. The schematic capture, including a digital to analog converter for the representation of the converted V_i, is depicted in Figure 7. and the simulated waveforms are given in Fig. 8, where $V(3)=V_c$, $V(2)=V_{osc}$, $V(7)=V_{com}$ and $V(25)=V_{conv}$. After the initial conversions, the charge and discharge of the capacitor reaches its steady state, providing the same A/D conversion value in all conversion cycles.



B. *Implementation*

The proposed A/D converter has been implemented using discrete components ($R_{osc}=R_{in}=10K\Omega$, C=20nF), a Schmitt Trigger input gate (74HC14) and the square V_{osc}=2.5 KHz generated by a waveform generator.

The oscillogram in figure presents the captured waveforms of the 2RC A/D converter for V_i= 760mV, being in accordance with the simulation results.

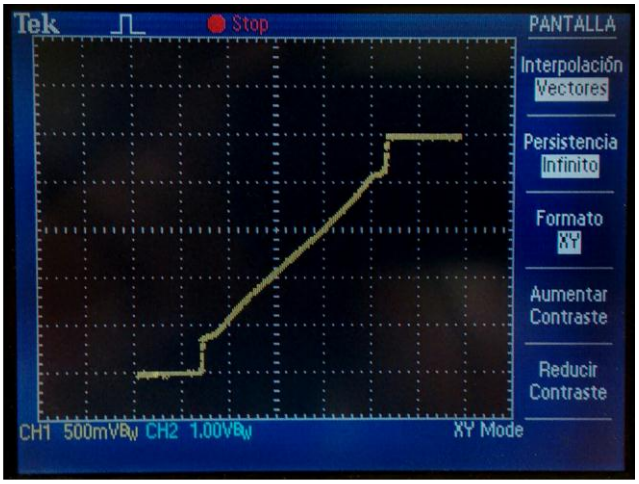
Figure 9. Oscillogram depicting the captured waveforms of the implemented 2RC A/D converter for V_i= 760mV (R_{osc}=R_{in}=10KΩ, C=20nF, V_{osc}=2.5 KHz).

In Fig. 10, the experimental transfer function of the 2RC A/D converter is presented. In order to have an analog signal of the converted value, a DAC has been used. The A/D converter presents a reasonable linear behavior within the expected input voltage range, but it does not convert values above and below the limits.

IV. Conclusions

A very compact ADC has been proposed and validated by simulation. It only makes use of two resistors and one capacitor. Although it suffers from some limitations, such as limited input voltage range and nonlinear conversion, it is valid for applications with massive data capture that do not demand accurate and fast conversions, as in the case of neural interface systems.

Figure 10. XY Oscillogram representing the experimental transfer function of the implemented 2RC A/D converter.



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