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Design and Implementation of MC-CDMA Wireless Communication System Using Partial Reconfiguration in FPGA—A Review

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Abstract— this paper reviews the state of the technique of field programmable gate array (FPGA) for partial Reconfiguration (PR), design methodologies of Wireless Communication System, such as Multi Carrier Code Division Multiple Access (MC-CDMA) technique has been to be suited for future wireless systems that are expected to provide higher data rates and greater flexibility for the services of voice, data, video and Internet to the users due to its property in using the bandwidth in efficient manner. The Software Defined Radio is considered as a wireless system applied by routines so as software. Consequently, the use of SDR allows vehicle manufacturers to familiarize communication applications sustained through cars to appropriate to the standards of the respected country presented in the object oriented programming. FPGAs are playing a very significant role in SDR. However, in modern wireless communication system programs, SDR and CR need to design a wide range of waveforms complex, which it is complicated in design and performance and implementation needs more time. The design of the modulation and demodulation and other signal processing application of PR technique that have the ability to modify blocks of logic dynamically by downloading partial bit files, while the remaining logic is still working without interruption; thus, power consumption and configuration time can be saved for a larger extent. The PR using was allowed to move for fewer or smaller devices as, decrease power and increase system upgradability.

Key words —MC-CDMA, SDR, FPGA, PR, and VHDL

I. Introduction

Traditional wireless devices are designed to present a single communication service using a particular standard [1], were based approaches, imagine that a user must buy a separated device each criterion, because most of them have their own specification of coding pattern types of modulation, frequencies range and reach to the environment. With the steady rise of services and levels of new wireless, single purpose devices with hardware resources allocated are no longer able to meet the needs of the user. It is too costly to maintain and develop system wireless every time the new standard comes into being. Most part of the present research work in wireless technology focuses on the providing several miscellaneous the services and maintain higher bit rate [2]. Thus, there is a need to develop a structure that will be able to support the possibility to return the mobile stations in accordance with a signal receiver. So, the mobile operator has to support all wireless communications systems separately. To solve this issue, the SDR technologies come in handy. It also reduces the total hardware usage and hence it reduces the power [2, 3, 4]. There are a number of definitions can be found on the description SDR, similarly known as software radio. The SDR Forum, working in cooperation with the Institute of Electrical and Electronic Engineers P1900.1 group, has operated to create a definition of SDR that will provide coherence and a clear overview of the technology and the benefits associated with it [2]. We choose a simplified radio in which some or all the physical layer functions are software defined.

Perform the design of QPSK modulator for digital signal processing on based DSPs and sliced FPGA that have a certain level of re-configurability, the QPSK modulator could be implemented almost entirely on a single chip along with an indispensable addition of an analog-to-digital converter to realize the QPSK modulator it is necessary to implement the blocks that will perform functions equivalent to the functions that are performed by circuits with the realization in a conventional approach where, the functions of voltage controlled oscillator in the digital domain are performed by numerically controlled oscillator (NCO). NCO is used for synthesizing a discrete-time, discrete-valued representation of a sinusoidal waveform. Signal shaping filters are finite impulse response (FIR) filters whose transfer function has the shape of the raised cosine. Multiplying the carrier and the modulating signal would require two mixers and signal shaping it is necessary to use at least two filters. [5]

SDR is a collection of Hardware and software in which all the radio functions can be implemented using software coding or firmware on a processing system [6].In [7], proposed the design procedure and implementation of SDR using Altera Cyclone II family board. MATLAB/Simulink, Embedded Matlab blocks, and Cyclone II development and educational board were used for implementation. Addition in the Space Communications, SDR, has an analog and a digital Automatic Gain Control (AGC) and the response of the AGCs to changes in SDR input power and temperature was characterized prior to the launch and installation of the SCAN Test-bed on the ISS [8].In [9], described the design and implementation of the CDMA digital transmitter for a multi-standard SDR baseband stand. The stand involves of reconfigurable a re-programmable hardware platform which provides different standards with a shared platform, and implement with FPGA by generate VHDL pattern of CDMA transmitter. Mahbub, et al., [10], proposed implementation of DS-CDMA

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transmitter using FPGA .They describe the design for pseudo random PN coding and a direct sequence principle based wireless transmitter, the circuit for the transmitter is comprised of basic digital components, such as flip-flops, shift registers, PN code and a BPSK modulator. Verilog Hardware Description Language (VHDL) was used for coding of the design. ModelSim Altera Edition 6.5b was used for functional simulation and logic verification. The Xilinx Synthesis Technology (XST) 12.3 of Xilinx ISE tool was used for synthesis of the transmitter [11]. Represents a Partial Reconfiguration is a feature of segments FPGA, a new era in the field of technology that allows for reconfiguring a part of the Xilinx FPGA while the rest of the device remnants fully operated. Xilinx has provided this feature in FPGA for the high-end, and a series VIRTEX, in access limited BETA since the late 1990s. Recent feature is the production with the support of their tools and their devices through since the release of ISE design suite version 12.1 continue support for this feature to improve in the latest version of ISE 13. The Plan-Ahead design environment can be used to manage assembly design, restraints, and validation of implementation[12, 13, 14, 15]. The [16] presented a practical example for a partial re-flow approach to a series RASIP SDR dynamically. In addition improvements can be made in the rate of data transfer and some functions such as data encryption (W7, E0, HELIX, RC4 etc.), which will improve performance and improve the hardware and take advantage of them for the development of the model with other algorithms using SFF-SDR. SFF-SDR platform provides a heterogeneous including both DSP and FPGA. Being modified function implemented in the reconfigurable (Block A) by downloading one of many partial bit files, A1.bit, A2.bit, A3.bit or A4.bit. Is as shown in Figure 1.The logic is divided into the FPGA design into two types, reconfigurable logic and static logic. The reconfigurable block A represents reconfigurable logic, and the rest are static logic[17].

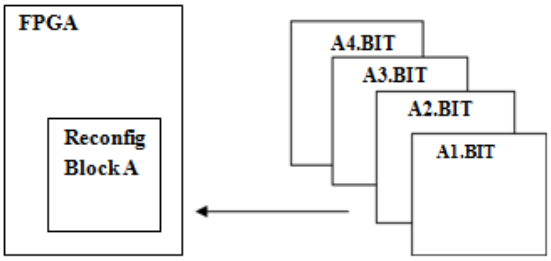


Figure 1 Partial Reconfiguration in FPGA

SDR and CR need to design a wide range of waveforms and design complex, performance and implementation with more time. Since that reduce the time and reducing complexity are critical in the wireless communications, in the [18, 19] design of the modulation and demodulation technique by PR technique to make sure that the user has the possibility to exchange between different modulations and demodulation structures without loading the full bit stream, where designed M-QAM and M-PSK in FPGA by PR and a low power of PSK Modems with PR by using a transmitter, that is a programmable twin channel LUT founded Direct Digital Synthesizer (DDS), which will form part of the Up converter. DDS will generate the required carrier [20]. Allows implementation of OFDM modems using PR faster switch between different OFDM transmitters that uses 1/2 BPSK, 1/2 QPSK, 3/4QPSK, 1/2 QAM and 3/4QAM through runtime in configuring the control record in modems FPGA, with limit minimum of power consumption, which is crucial in cognitive radio. Technology PR can be used to design platform restructuring the entire waveforms of cognitive radios [21]. Using dynamic partial reconfiguration of some modules H.264/AVC video encoding on the path reconstruction achieved the required condition in the area. So this method is not affected productivity and reduce the trade-off is between applications real-time video processing frameworks interfaces. Higher operating frequency is 109.6 MHz and is designed so that easily meets all requirements of the productivity of real-time processing of HTDV [22]. The [23] described ideas, on-going work and future work to exploit the possibility of adopting Dynamic Partial Reconfiguration (DPR) properties FPGA devices to improve real-time systems is an integral part of reliability. Property of the DPR (FPGA) based SRAM allows the use of fixed units with units restructuring, which could lead to the recovery of the system from inside the device to support one solution reconfigure self-chip. This offers significant improvements in the speed of healing, and sensitive applications critical to another.

In addition, Digital Pre-Distortion is a linear method that will negate the impacts of non-linear amplifier power generated while using third-generation large-scale wavelength, such as Wimax, LTE, WCDMA and Tetra [24]. Also using PR, design of frequency hopping synthesizer in which256 bit Blum-Blum-Shub (BBS) generator is used as a random number generator, implementing of the hardware is using Xilinx System Generator and modeling [25]. Ostler and his colleagues work on FPGA boot-strapping method for constructing FPGA circuit units using PR [26], at run-time over PCIe, so that this method achieves a minor, static design that is configured in power even includes a PCIe the endpoint, a configuration controller, and an interface for partially reconfigurable areas. Large, dedicated circuits can be added or modified at run-time without restarting the host device. Development platform bootstrap consists of FPGA module which allows PR across the PCIe link, the interaction between the PR Unit and the host, and a driver for Linux to interact with FPGA on the host.

II. MC-CDMA TECHNIQUE

A lot of attention has been placed on modulation techniques such as Code Division Multiple Access and Orthogonal Frequency Division Multiplexing. CDMA is widely used in current third generation wireless communication systems. Spread spectrum technology, the basic principle behind CDMA was generally used in military communications for improved secrecy and low probability of interception during transmission. Today, CDMA is increasingly deployed in civilian markets, thereby giving increased capacity and better performance; in addition, also OFDM is seen as a possible candidate for fourth generation wireless communication systems that request higher data rates for data transmissions and voice. [27].

MC-CDMA is formed by combining OFDM with CDMA. The OFDM is well suited for high data rate uses, and the CDMA is a multiplexing technique where a number of users are simultaneously available for accessing a channel [28, 29]. MC-CDMA adds the advantages of CDMA with the natural toughness to the frequency selectivity offered by OFDM. In MC-CDMA, the spreading and processing occurs in the frequency domain, rather than in the temporal domain. With MC-CDMA, a data symbol is transmitted above N narrowband subcarriers with every sub-carrier existence encoded based on the spreading code [30]. In traditional DS-CDMA, every consumer symbol is transmitted in the form of sequential chips, each of which is narrow in time and therefore wider in bandwidth. In contrast to this, in MC-CDMA due to the FFT along with OFDM, the chips are longer in time period and thus narrow in bandwidth. Shows basic block diagram of the MC-CDMA system in Figure (2).

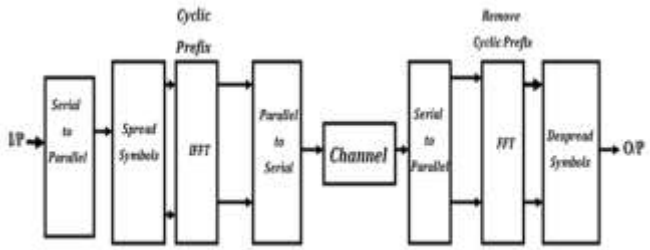


Figure 2 *Block Diagram of MC-CDMA system [31]*

III. PARTIAL RECONFIGURATION (PR) ON FPGAs

Partial reconfiguration helps to reduce costs and board space to provide for flexibility, to change a vital part of the system without shutting down the entire system [32]. Figure 3 shows how the use of PR will reduce the size of the implementation of the design on the segments FPGA. This figure illustrates the FPGA with the design of the three sections of which are dedicated to the areas of fixed, and the rest of the FPGA can be used to implement the PR. The first part of this figure shows the FPGA without the implementation of PR. This part can hold only a small number of different designs within the region of partial reconfiguration of the FPGA. However, after the implementation of PR and a lot of additional designs can be stored outside the FPGA and exchanged if need for changing while running FPGA [33].

A. *Benefits of PR Technology*

Increased flexibility solution through the design and functionality doubling time, reduce the size or number of FPGA ,thus cost, through job sharing time, reduce energy consumption by downloading vital functions on demand, offers real-time litheness in the select of algorithms or protocols available to the application at any instant, enable the use of new technologies in the field of security design, Advances FPGA fault tolerance, accelerates configurable calculating and decreases storage requirements BITSTREAM. The added that it has a distinguished supporting the implementation of the complete design using powerful technology division also, allows entry of the entire design constraint and timing analysis and confirmation. Finally, backings Virtex-4, Virtex-5, Virtex-6, Virtex-7, Kintex-7, Artix-7 family of FPGA and the Zynq™-7000 all programmable SoC family [15].

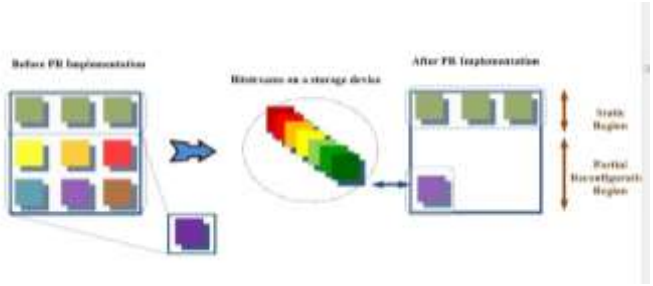
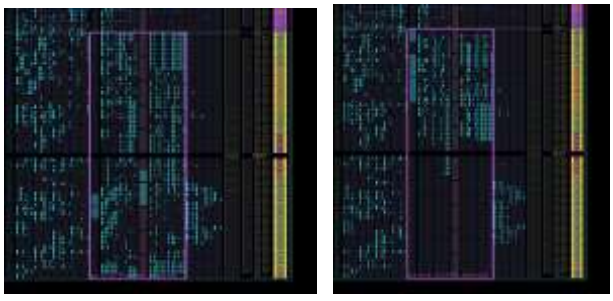


Figure 3 Reducing Size after Implementing PR

B. *PR Design Flow*

Targeting project configuration PlanAhead PR by the ZC702 evaluation platform, when you load the synthesized design, the filter engine module deal with it as a Black Box, where there is no net list associated with it, where the filter engine module is considered as an RP. Then, creating of two Reconfigurable Modules (RM) and by adding the corresponding files net list / constraint files for Sobel and Sepia filter cores. Floor-plan the RP by setting the physical size of the division and the kinds of resources required [34]. XILINX support segments FPGA reshaping CLBs, BRAM, blocks of DSP, in addition to all the resources associated with the directive. When, building design configurations restructuring and training should be the first to be selected for the implementation of one of the most challenging. If all RMs in the subsequent configurations are smaller or slower, easier it will be to satisfy their demands. Configuration is performed Sobel and encourage configuration Sobel said the results of the implementation of the stator design can be reused by the Sepia configuration. After that step is to implement the Sepia configuration, Figure 4 shows a Plan-Ahead display comparing the physical resources inside the RP for the routed Sobel and Sepia configurations. Then, generate bit-streams full and partial configurations Sobel and dark brown[35].



(a) (b)

Figure.4 Plan Ahead Display (a) Placed RP Resources for Sobel Filter (b) Sepia Filter**.**

IV. COMPARISON AND ANALYSIS

The [2] to provide coding modifications, O-QPSK to change QPSK, implementation of FHSS modulation and demodulation in Matlab, to be used to maintain the level of error in the high data rates with SDR, the results of the Frame Error Rate (FER) for models simulate four, where WiMAX systems using RS code with convolutional coding and OQPSK fade almost at 20 dB while existing WiMAX system and QPSK the ratio is high, but before 28 dB and WiMAX turbo using coding and QPSK decreasing linear when FER at 0.5 to WiMAX using RS added turbo coding and QPSK at 0.65.

A lot of papers discussed the communication circuit design using Simulink, Matlab and Xilinx with system generator, Designed [1] transmitter and receiver use QPSK modulation that results were QPSK rate twice slower than binary. The work on the filtered of the signals after being up-sampled at a transmitter baseband stage, also the difference between the IF and harmonic spectrum produced in the DUC is around 30-40 dB and reduction relatively few; transmitter spectrum is created after the signal is fed to the mixer. Keep this process IF signal in the 5 MHz and 15 MHz to 20 MHz to achieve sampling rate receiver. Continued MHz 5 IF signal is identical at 15 MHz and harmonic of 0.10 until 20 MHz in the spectrum, the cut off frequency ,in received spectrum, is maintained at 0.25 MHz From the observation, the attenuation range for the transceiver occurred between 50-60 dB and modulated IF signal set using QPSK modulator transmitter receiver. Sampled signal design transceiver downside is lawful only after 56 samples at 10 MHz, these samples are involved the 28 samples and 28 transmitted contained. Compared with [36], where System Generator's FIR, FFT, FIFO and FDA Tool blocks are used, shows the output of the combined channel spectrum range from an average of two episodes and display spectral output channel spectra in the range of channel banks SDR at 2 MHz bandwidths frequency, and receive the output of this channel as contained in the input without the interference of noise in the output sinks. In [7], a summary of the use of resources is about 29% of the total Logic Elements and about 1% of the IOs and less than 1% of the total Memory bits. Follow that too, and the highest frequency was 44.79 MHz at 22.326 ns maximum period with maximum path delay from any node at 22.326 ns. In addition, the ratios in the [37] for DSPs of Slices, Slice Flip Flops, IOBs, BRAMs are (18, 12, 5, 12) % respectively. Finally, design MIMO-OFDM system based on FPGA in [38], that has replaced SISO to Multiple Input Multiple Output systems, four different types of MIMO respectively 2nd, 4th, 8th and 12th, reduce the power with low cost that find total dynamic power 0.0107W of SISO and (0.0216 0.03211 0.0858 0.1285) W of 2,4,8,12 MIMO Respectively, And the number of Slices used increased from 60 in SISO to up to 270 in 12 MIMO with twice in each type of MIMO, analysis of data rates for MIMO systems and increases the data rate increase with the system when access to 12MIMO, stops data rate to an increase in large quantity. As the number of antennas rise, also increases the cost of the hardware, the data rate extents overhead 1 Gbps in the case of system for 12 MIMO.

In [20] use the same design with the use of technology pipeline design and implementation using a custom block RAMs, which will not use any guidance for programming within the heart, and you will get a reduction of power dramatically, where the total power 2.707 and the dynamic just 0.002 and quiescent power be 2.705. While, Kumar in [18], used four types of M-PSK modulator by programmable dual-channel station based DDS, results have proved that the resource utilized by the modulator and demodulator. Most of them do not exceed the 1% for available, And he, also in [19], implemented 4, 8, 16, 32, and 64 -QAM modems in Virtex-6 FPGA using PR technique, a summary of the use of resources for the fixed part of the entire modem and dynamic part of the-QAM 64 is about 37% of the DSP48 slices and about 1% of the block of the Rams. Follow that too, designing an OFDM transmitter using PR technique by Implementation of the 1/2 BPSK, 1/2 QPSK, 3/4QPSK, 1/2 QAM and 3/4QAM, the full transmitter is implemented as a multi-rate system with three clock domains. The resource utilization summary for the entire static part of the transmitter and the dynamic part with 16-QAM is around 11% of the DSP48 slices and around 79% of the Block Rams and about 50% of the Global Clock Buffer[21]. Self-configure the rest of the FPGA using PR is concluded the FPGA bootstrapping design, so PR is a form of run-time reconfiguration and provides a number of important aids, statistics shows that the use of resources almost 19% of the DSP48 slices and around 2% of the BRAM and less than 60% of the Vorbis in Flip-Flops [26]. In [25], implementation of 256-bit Blum-Blum Shub (BBS) generator random number generator in VIRTEX-6 FPGA implement the entire design. The estimated resources of the generator in this design are consumes about 10% of the entire FPGA and vary depending on the width-bit integer BLUM and seeds. The use of Simulink and the possibility of change and adjustment without the cost of pre-implementation confers an important advantage of the design and high flexibility Moreover, the use of PR in FPGA a major shift toward high performance and reduce cost and complexity by minimizing hardware.

V. CONCLUSION

The aim of this paper detailing contributions to the design of wireless communication systems, and in ways different design, based on partial Reconfigurable FPGA by using the SDR as an ideal solution to the problem of cost and complexity. After a comprehensive description of the Literature Review in the areas design different modulation and demodulation of wireless communications systems in the FPGA and use the PR, indeed, a lot of recent research revolves around the SDR and FPGA, which confirm and prove that the design of wireless communication services based on SDR and the application of many of these services, using modern techniques exist in the FPGA, such as PR. This section was followed, been reviewing the system Multi Carrier-CDMA to can be appropriate for future wireless communication systems, which is expected to provide higher data rates and more flexibility for users of voice, data, video and Internet and propose this system in the

paper, because it was given to the use of his property in a manner effective bandwidth. Multi Carrier-CDMA technology is a mixture of CDMA technology and OFDM technology and combines the benefits of both technologies. In the near future, the complexity of the communication systems will continue to grow. The tasks allocated to the control algorithm will no longer limit the regulation, but you will have to manage the diagnosis and error-adjustment control on the Internet. In this context, research efforts on the applications and the theory of partial reconfigurable in wireless communication systems are critical.

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