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A Comparative Analysis of Performance Gain of 7-nm FinFET over Planer CMOS

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***Abstract*— FinFET has been contemplated as a seemly substitute for the conventional CMOS at the nano-scale regime owing to the projection for application in the integrated circuits fabrication due to its extraordinary properties like improved channel controllability, high ON/OFF current ratio and reduced short-channel effect. In this paper, circuit simulations of 7-nm FinFET and planer CMOS are comprehensively investigated showing a 34.92% and 28.79% increased drain current in 7-nm Fin-FET compared to the existing 22-nm and equivalent 7-nm planer CMOS respectively. A detailed simulation study evaluating the performance of the proposed design is presented exhibiting a 2X increase in drive strength with the increment of fins. Fin thickness of 2.725 nm along with a height of 10.9 nm has been used resulting in an 8X reduction in gate area which is the smallest 7-nm Fin-FET structure yet developed. The indiscriminate variations of the characteristics obtained in various simulations lead to a culmination of shifting to Fin-FET from planer CMOS which is imperative from the prospect of design and manufacture.**

***Keywords*—FinFET, multi-gate FETs, 7-nm, nanoscale, HSpice**

I. Introduction

The steady down-scaling of feature sizes resulting in exponential miniaturization of the CMOS technology in digital circuits has been the driving force for the continual improvement in circuit speed and cost per functionality over the past several decades. Moreover, energy consumption has always been a crucial performance metric for integrated-circuits (ICs) and the voltage down-scaling is quite effectual in reducing the power consumption of ICs which is desirable for some relaxed-performance applications, such as portable wireless devices, medical devices and sensor network nodes [1]. But, with advanced geometry planar FET technologies in the nanoscale regime, such as 20 nm, the source and the drain encroach into the channel, making the leakage current to flow easily which eventually makes it very difficult to turn the transistor off completely resulting in short channel effects, sub-threshold leakage, gate-dielectric leakage, off-state leakage current, delays, power dissipation and device to device variations [2]. Thus, the downscaling of bulk material faces significant challenges below the sub 20-nm that are inhibiting the overall device performance. But, currently, these concerns are unavoidable as transistor size is the most important aspect to be considered by design engineers in the scaling process.

Hence, to solve the scaling concerns, two different paths can be chartered. The first path envisages introduction of new technologies into the conventional planar MOSFET to allow further scaling and boost the performance of scaled CMOS. The second path presupposes adoption of new transistor architectures such as ultra-thin body FETs and multi-gate FETs [3] which inherently have superior electrostatic control over the inversion channel and works at a lower bias voltage.

In this paper, FinFET devices [4], a derivative of multi-gate FETs have been proposed as a promising alternative over the conventional bulk CMOS-based devices at the nano-scale by providing an overview of comparative analysis of these two structures at a 7-nm nano-scale regime. We know, FinFET based designs impose improved control over short channel effects, low leakage and superior yield below 45nm that help to overcome the obstacles in scaling. In this paper, we will demonstrate that FinFET devices offer superior scalability with reduction in gate area, low gate leakage current resulting in higher drain strength and reduced energy consumption by operating at minimum threshold voltage. Furthermore, a detailed simulation study evaluating the performance of the proposed design is presented exhibiting a 2X increase in drive strength with the application of multiple fins. Fin thickness of 2.725 nm along with a height of 10.9 nm has been used in the proposed FinFET structure resulting in an 8X reduction in gate area which is the smallest 7-nm Fin-FET structure yet developed.

II. Description and Simulation Approach

The device schematics of the triple-gate FinFETs modeled in this work are shown in Figure (1). We have used 7-nm FinFET technology by implementing the 7-nm FinFET device model (10nm spacing between edges of the diffusion regions) excerpted from Chen et al. of which the device model extraction and validation are presented in [5]. Synopsys TCAD simulation is used by employing semi-classical transport models with some quantum corrections [6] for analytical process. This device model is constructed by using look-up-tables (LUTs) where the drive strength is calculated utilizing the current equation obtained from [7] and is compatible with SPICE through a Verilog-A interface [5].

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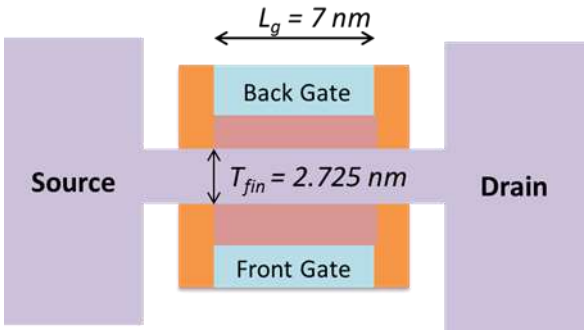

Figure 1. 7-nm FinFET model (top view)

FinFETs are basically 3D structures that rise above the substrate effectively providing more volume than a planar transistor for the same area as a conducting channel. The gate wraps around this thin silicon body called fin, providing better control of the channel and allowing minimum current to leak through the body when the device is in the 'off' state by controlling through the 3 (multiple) gates. This, in turn, enables the use of lower threshold voltages and results in enhanced device performance and less power consumption [8]. In FinFET model, the effective width of the transistor is estimated as $W_{eff} = 2H_{fin} + T_{fin}$ [9]. For this device, the thickness of the fin (T_{fin}) has to be smaller than the gate length L_g so that the short channel effect equations.

TABLE I. EXTRACTED PARAMETERS FOR A 7-NM FINFET MODEL

Parameter	Value in 7-nm FinFET
Physical gate length	4.905 nm
Oxide thickness	1.09 nm (front and back)
Body thickness	2.725 nm
Fin height	10.9 nm
Fin thickness	2.725 nm
Fin pitch	9.725 nm
Source/drain doping	1e20 /cm3
Source-side underlap	1.09 nm
Drain-side underlap	1.09 nm

III. Results and Discussion

Based on the methodology presented in Section II and using the 7-nm FinFET model from [5] having a fin thickness of 2.725 nm, we have estimated an overall performance gain of FinFET in nearly every aspect compared to the 7-nm planer CMOS. From our acquired simulations, we can verify that a 34.92% manifold increased drain current is obtained for 7-nm FinFET compared to the existing 22-nm technology of planer MOSFETs having a minimum gate width of 0.3µm. An equivalent 7-nm planer CMOS shows a 28.79% decreased current with again the minimum gate width of 0.1µm compared to the 7-nm FinFET. Hence the achieved results represent that even if we scale down the conventional MOSFETs to the 7-nm regime we will not be able to reach the equivalent drive strength obtained with just a single fin structure.

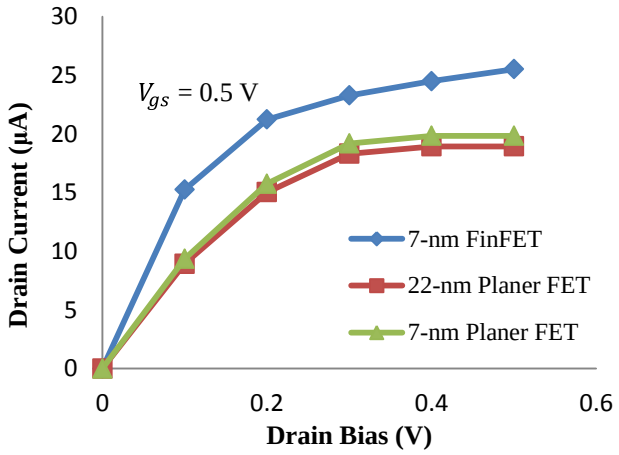

Figure 2. Comparison of drain strength among 7-nm planer, 22-nm planer and 7-nm Fin-FET

As yet, the analysis and all the computations regarding FinFET have been with a single fin structure. Now, rather than a single fin, theoretically by using multiple fins we can obtain an increase in drain current and the corresponding plot clearly shows that there is an almost 50% increase in the drain current with the increase in the number of fins.

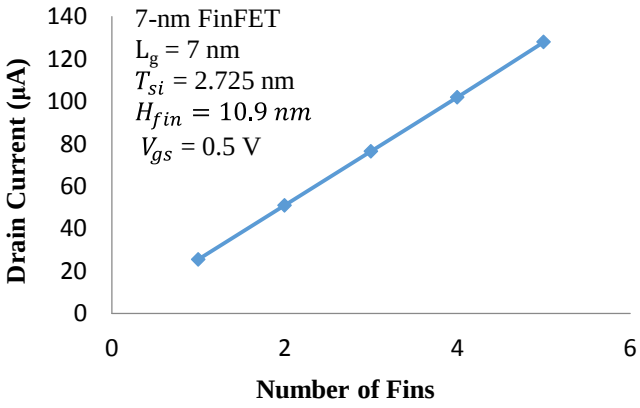

Figure 3. Variation of drain current with increased parallel fins

This clearly surpasses all the past estimations under the 7-nm nanoscale regime for both planer and tri-gate transistors. Utilizing this availability of increasing drain current with multiple parallel fins we made a comparative analysis of the gate area required in both 7-nm planer and Fin-FETs. While the minimum gate width for a 7-nm planer FET is 100 nm, an equivalent 7-nm FinFET having fin width of 2.725 nm and a fin pitch of 9.725 nm can accommodate 8 Fins resulting 204µA drain current which is an increase of 703.1% more drain strength. This evidently favors the concept of scaling in

terms of using 7-nm FinFET with the 8X reduction in the gate area.

Earlier, there have been some proposed designs of obtaining increased drain current under the 7-nm regime. But the drive strength obtained from this model exceeds all the previous designs under this nano-scale region.

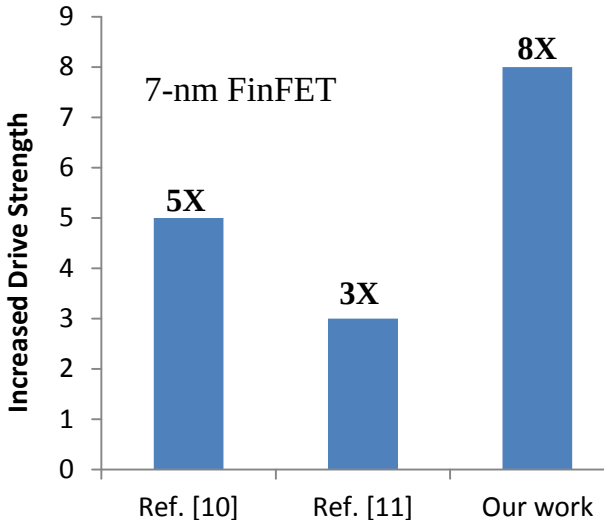

Figure 4. Comparison of drive current among 7-nm FinFET models

Now, as the statistical data shows, FinFET has considerable advantages over planer CMOS and yet the manufacturing challenges make it difficult to go into the fabrication process [12]. As mentioned earlier, this paper contains a relative analysis of both the transistors under the 7-nm regime and henceforth the option of 7-nm planer MOSFET has also been into our consideration. Now, from our simulations we can conclude that we can only obtain the single fin FinFET drain current in figure (2) if the gate width can be minimized to 0.128µm which is 11X more gate width than the FinFET model. Hence, this precisely does not support the requirements for scaling of MOSFETs.

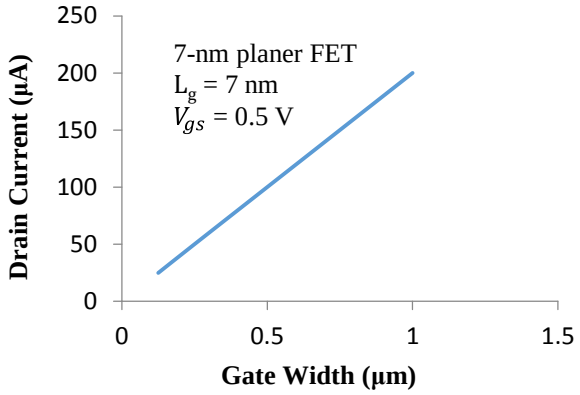

Figure 5. Effect of variation of gate width on drive strength in 7-nm planer transistor.

Apart from decreasing the gate width, an alternative approach to reach the high current obtained in FinFETs can be by varying the supply voltage. For this particular model of FinFET, device simulation data was generated by sweeping gate and drain voltages from 0.1V to 0.5V. Due to linear extrapolation of currents and clamping of capacitances beyond the voltage range (-0.1 to 0.8V) in the Verilog-A model, oscillations may be observed in the simulation output when circuits are simulated close to 0.8V. That is why, the drain voltage is restricted within the range 0<Drain voltage<0.5V [5] in FinFET simulations and this favors the 7-nm planer CMOS as there is no restriction to the maximum sweeping voltage.

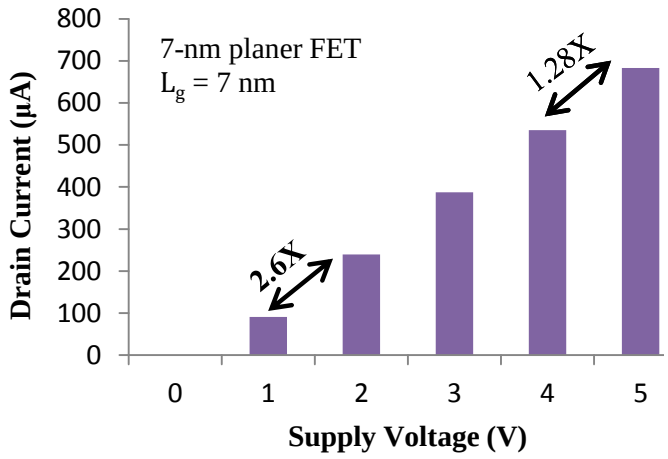

Figure 6. Rate of change of supply voltage in 7-nm planer transistor

And yet, as figure (6) demonstrates with the increase in supply voltage, the rate of drive strength increment reduces counteracting the prospect of increasing the supply voltage for higher drive strength. Moreover, supply voltage scaling is quintessential in order to reduce power density in Integrated Circuits, since increased power density leads to heat which reduces device performance (due to reduced mobility) and further increases standby power consumption (due to increased thermal leakage). Hence, we can state that, neither reduction in gate width nor increasing the supply voltage in case of planer CMOS can reach the drive strength obtained from equivalent 7-nm FinFET.

IV. Conclusion

This paper shows that after careful optimization FinFETs offer high drain current of 28.79% over planer CMOS in 7-nm regime that is advantageous in multiple threshold voltage circuits which requires low-power high-performance transistors. FinFET devices can operate at a lower supply voltage than nominal since they have a decreased threshold voltage which significantly improves dynamic power consumption by 10% as obtained from the supply voltage calculations for a single fin and this constitutes a strong expedition for FinFET adoption. Moreover, the foundation library of FinFET model has the minimum fin height and

thickness standard values compared to the contemporary 7-nm FinFET models resulting in a gate area reduction of 8X whereas earlier works proposed a 3X and 5X reduction assuring lower dynamic power consumption further. Multiple parallel fins have also been examined and a 2X increase in the gate current has been noted. Hence, FinFET devices outperform bulk CMOS devices in ultra-low power designs by allowing voltage scalability, lower power consumption and gate area reduction. Overall, since continuous shrinking of channel length increases the speed of devices in very large scale circuits, the FinFET model of this paper is beneficial over planer CMOS for steady miniaturization at a channel length of 7-nm regime.

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