International Journal of Advancements in Electronics and Electrical Engineering– IJAEEE
Volume 4 : Issue 2 [ISSN : 2319-7498]
Publication Date : 30 October, 2015

Design and analysis of a CFCFC OTA based on the Behavioral Modeling of a 4th Order Low-Pass Hybrid ΣΔ Modulator

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***Abstract*—In this paper SIMSIDES-based behavioral simulation of a 4th order Hybrid ΣΔ (HΣΔ) modulator was carried out to define electrical characteristics of an Analog Building Block (ABB), specifically a fully differential OTA. A set of experiments based on analytical models was defined to analyze the overall performance of the Switched Capacitor (SC) ΣΔ modulator in order to translate the design considerations into a set of values that the design at transistor level can be established by the desired performance of the chosen architecture. In accordance with this design strategy, a fully differential CFCFC OTA was designed according to design rules of a 130nm CMOS process. Simulation results show that an open-loop gain A_0 = 60dB, and unity-gain bandwidth f_{0dB} = 1.0GHz are enough to obtain a Signal-to-Noise Ratio (SNR) of 68dB (±1dB) when this OTA is added to the DT ΣΔ modulator. Furthermore the hand-made small-signal analysis of the chosen OTA topology allow us to obtain an analytic design model useful to correlate not only CADENCE results, but also to identify the most important parameters affecting the frequency response.**

***Keywords*—High level simulation, ΣΔ modulation, OTA, small-signal analysis, analog design, teaching.**

I. Introduction

The design of analog systems consists of three basic steps: architecture selection, establishment of analog building specifications and minimization of the circuit non-idealities effects on the whole system performance [1]. As described in [2] the individual analysis strategy is not the most suitable one as these design steps are deeply correlated, which means that a unique fully-integrated analysis must be developed. In such an approach all design considerations are treated at the highest level of abstraction because of the need to reduce simulation time, mainly when the chosen architecture is analyzed at transistor level. In addition, high level simulation allows the designer to find the desired performance of the selected architecture, which can be converted into a set of values, so that the parameters of the transistor-based circuits can be established directly.

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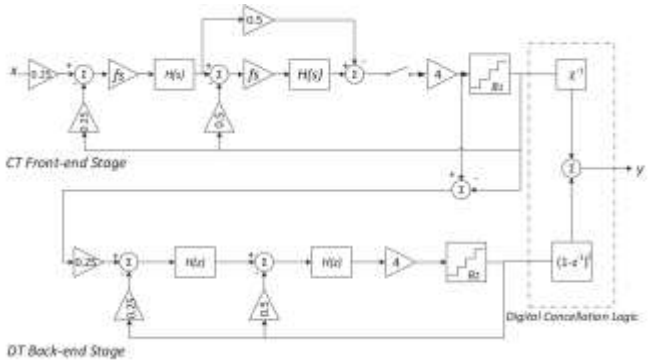

Figure 1. Modulator Architecture

In this scenario the design of an analog system consists of solving a unique problem: the development of a behavioral model that not only minimizes simulation time but also reflects the effects of the so called circuit non-idealities [3]. In this paper, actually a work in progress, SIMSIDES-based behavioral modeling [4] of a 4th order Hybrid ΣΔ modulator is used to design a fully-differential Operational Transconductance Amplifier (OTA) in order to satisfy the design requirements of the DT back-end stage shown in Fig. 1. From behavioral simulation a set of values were found such that the parameters of the transistor-based circuits have been established according to the desired performance of the chosen architecture, where the function of each Processing Basic Block (PBB) is easily identified (see Fig. 1). According to the simulation conditions shown in Table I, the unity-gain bandwidth of the OTA must be at least five times the required sampling frequency value, i.e. f_{0dB} = *1GHz*. Also, both low and high-frequency small-signal analysis were carried out in order to attain a better understanding of the OTA topology.

II. Behavioral Modeling as a starting point in an OTA design

The modulator loop-filter is a 4th order proposal, specifically a 2-stage (2-2) architecture, where the front-end is a CT implementation and the back-end a DT proposal. The strategy behind the high level simulation of the hybrid ΣΔM has been defined as follows: 1) the weights of both modulators were obtained from numerical analysis, 2) for simulation purposes the front-end was assumed to be an ideal system (non-idealities were not taken into account), and 3) the back-end is firstly assumed as an ideal design and then non-idealities are included in order to quantify their effect on the system performance, by comparing both scenarios. With the

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TABLE I. SIMULATION CONDITIONS

Quantizer	Bias	±1.2V
	Number of levels	3
Input Signal	Amplitude	-10dB
	Frequency, f_i	991.234kHz
	Bandwidth	10MHz
	Sampling frequency, f_s	200MHz

TABLE II. SELECTED PARAMETERS

SC Integrator	I_O	0.3mA
	g_m	3mS
	A_0	≥60dB
	R_{on}	250Ω
	Output Swing	±0.6V

help of SIMSIDES (SIMulink-based SIgma-DElta Simulator) the strategy mentioned above was carried out to obtain a set of specific parameters that must be translated into a transistor-based implementation.

In order to define the design specifications of each PBB is of paramount importance to state a list including the most important sources of non-idealities that affect the expected performance of the whole design. It is well known that the physical parameters affecting the overall behavior of the SC integrator are in high percentage the open-loop gain (A_0), the unity-gain bandwidth (f_{0dB}), the input transconductance (g_m) and the maximum output current (I_O) of the OTA [2], [5]. Furthermore, the performance of SC integrator circuits are affected by several other OTA non-idealities, such as slew-rate and settling time, which can be minimized depending on the type of OTA used. According to simulation results, a set of specific characteristics for the OTA were found which are shown in Table II.

III. OTA Design

A. *OTA and CMFB Architecture*

Differential signal processing is the key for designing a robust implementation, thus a fully-differential OTA has been chosen to build a SC integrator. A differential implementation reduces the common mode noise due to power supply and substrate, clock feedthrough, charge injection and also eliminates even-order harmonic components [6]-[7]. Because of the system's sampling frequency (200MHz), an OTA with a unity-gain bandwidth, f_{0dB} = *1GHz*, and a phase margin between 45°-60° that provides good settling behavior [8]-[9], must be designed. The chosen OTA architecture is a Complementary Folded Cascode Feedforward Compensated (CFCFC) shown in Fig. 2, which is very similar to that analyzed in [6], the difference between both proposals resides in the floating capacitor, C_f. In this proposal, cascode stages

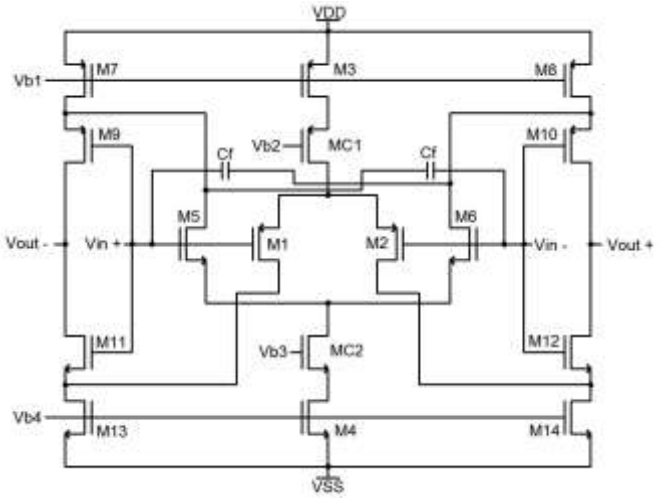

Figure 2. CFCFC OTA [9], [13]

provide high gain and fast operation even when low power supply is used (as low as ±1.2V) [9]. The feedforward technique lends itself for low supply folded cascode amplifiers since the DC bias for the cascode and input transistors is the same, that is the middle point between the positive and negative voltage supply (in this case 0V), allowing the gate connection. The floating capacitor, C_f, is used to feed and change the phase of the input signal forward to the cascode node that provides the input pole cancellation because of the source resistance at the input [10]. The OTA bandwidth is maximized by increasing the transconductance of the input transistors, which is achieved using wide devices and ensuring that the input transistor bias current is larger than the bias of the cascode transistors [8]. The Common Mode FeedBack (CMFB) block senses the common mode voltage at the amplifier's outputs (ideally not the differential mode voltage), process it, and then a voltage is feedback to the amplifier to fix the DC current flowing through the output stage; this process also changes the common mode voltage to a preset value, normally analog ground to maximize the output signal swing. The CMFB implemented (see Fig. 3) when compared to other architectures surpasses them in performance due to its good linearity, high sensitivity to common mode signals and small parasitic capacitance, trading off chip area and power consumption [11]-[12]. The OTA open-loop frequency response is displayed in Fig. 4.

B. *Low-frequency small-signal analysis*

For the CFCFC OTA the DC gain is the product of the effective transconductance and the output resistance

$$A_0 = r_{out} * g_{m,eff} \quad (1)$$

The low-frequency small-signal equivalent circuit is analyzed to obtain a mathematical model where the highest impact transistor level parameters are easily identified. In the simplest analysis several considerations are usually made where the source/bulk voltage and conductances are neglected. In this paper, bulk transconductance is taken into account in order to obtain a correct model for the open-loop gain.

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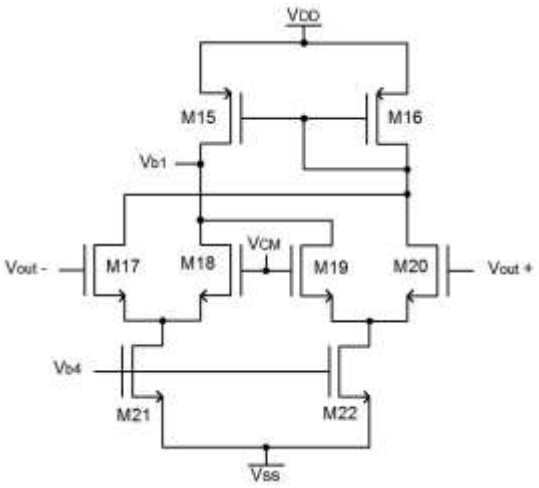

Figure 3. Common Mode Feedback Circuit [12]

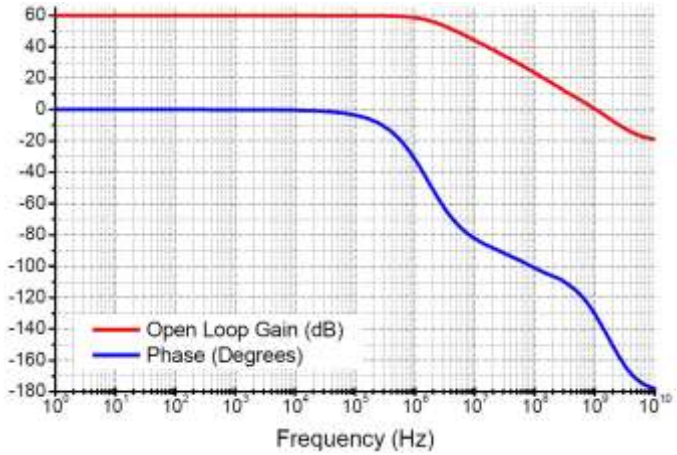

Figure 4. CFCFC AC response

Table III shows the comparison results between several hand-made small-signal analyses, where the last column represents the error when compared to CADENCE. As can be seen, if all the small-signal components are taken into account, the difference between the analytic results and SPICE results is less than 1%.

C. *High-frequency small-signal analysis*

Top level simulations using transistor level circuits usually take a long time, which is why suitable equivalent models are needed. The most important element of a Switched Capacitor integrator filter is its amplifier, therefore if an equivalent circuit is implemented, the simulation time could be reduced significantly. The high-frequency differential half equivalent circuit is shown in Fig. 5. The capacitances and conductances of the circuit are related to the transistors by the following equations:

TABLE III. LOW-FREQUENCY SMALL-SIGNAL COMPARISON

Considerations	r_{out}(Ω)	$g_{m,eff}$(mS)	A_0(dB)	ε_r(%)
✓V_{SB}, ✓g_{ds}	32997	30.2	59.97	0.338
✗V_{SB}, ✓g_{ds}	29592	29.9	58.95	11.38
✗V_{SB}, ✗g_{ds}	23126	29.4	56.64	32.08
[9]	25883	32.4	58.37	17.06

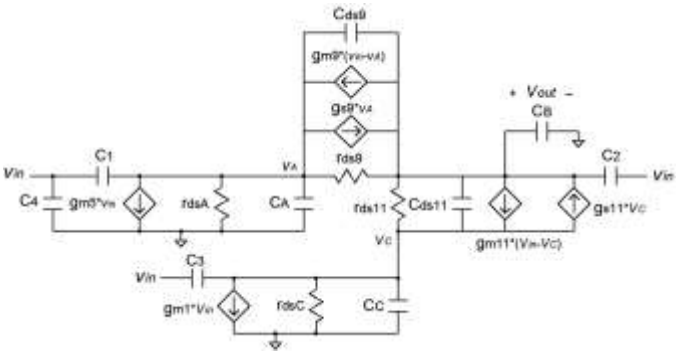

Figure 5. CFCFC High-Frequency differential half Small-Signal Model

$$C_A = C_{db5} + C_{db7} + C_{gd7} + C_{sb9} + C_{ds5} + C_{ds7} \quad (2)$$

$$C_B = C_{db9} + C_{db11} + C_{gd17} + C_{gs17} + C_L \quad (3)$$

$$C_C = C_{db1} + C_{db13} + C_{gd13} + C_{sb11} + C_{ds1} + C_{ds13} \quad (4)$$

$$C_1 = C_{gd5} + C_{gs9} \quad (5)$$

$$C_2 = C_{gd9} + C_{gd11} \quad (6)$$

$$C_3 = C_{gd1} + C_{gs11} \quad (7)$$

$$C_4 = C_{gs1} + C_{gs5} \quad (8)$$

$$r_{dsA} = r_{ds5} \parallel r_{ds7} \quad (9)$$

$$r_{dsC} = r_{ds1} \parallel r_{ds13} \quad (10)$$

where C_L is the load capacitance at the output terminal, and the other capacitive and resistive terms have their usual meaning.

The response obtained when solving the equivalent circuit in Fig. 5 presents great consistency when compared to that of CADENCE (see Fig. 6), allowing its use to reduce significantly the simulation time of the system.

D. *Other Results*

The OTA has been designed according technological design rules of a 130nm CMOS process. A summary of the simulation results is shown in Table IV whereas Table V displays the transistor dimensions of both OTA and CMFB. The results achieved by the CFCFC OTA fulfill not only the performance listed in Table II, but also the expected performance at system level depicted in Table I.

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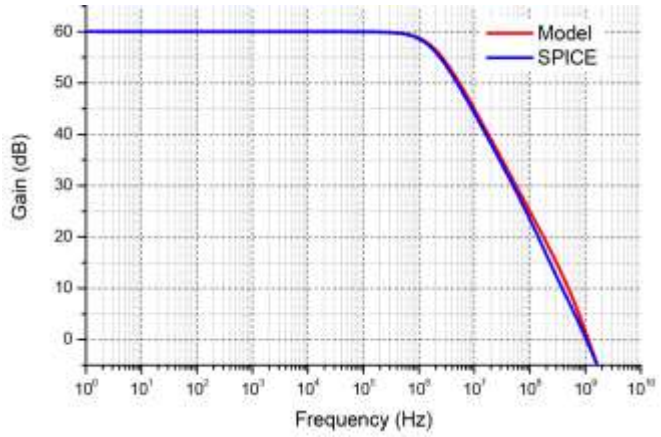

Figure 6. Transistor Level Simulation vs Circuit Equivalent Model

TABLE IV. SIMULATION RESULTS

OTA	I_O	0.311mA
	f_{0dB}	1.047GHz
	A_0	60dB
	C_L	2.5pF
	Φ_M	48.5°
	P_S	11.82mW

TABLE V. TRANSISTOR'S SIZES AND CAPACITORS VALUES

OTA	M1-M2	1371:1
	M3	492:1
	M4	64:1
	M5-M6	416:1
	M7-M10	504:1
	M11-M12	165:1
	M13-M14	56:1
	MC1	614:1
	MC2	75:1
	Cf	2.5pF
CMFB	M15-M16	712:1
	M17-M20	44:1
	M21-M22	56:1

IV. Conclusions

The main advantage of high level simulation is that all the design considerations are converted into a set of values, where the most important parameters of the transistor-based circuits can be easily established according to the desired performance of the chosen architecture which allows the designer to identify key parameters. As shown in Table II, the simulation process has resulted in feasible design values, that if fulfilled, represent an equivalent number of bits (ENOB) of 10.46. However, several parameters still must be optimized, such as parasitic capacitance, integrator settling behavior and current leakage [14]. With the help of SIMSIDES, a system design was carried out in order to firstly obtain a group of specific parameters that show us the viability of a transistor-based system synthesis. The OTA architecture was secondly designed and simulated at transistor level to illustrate the proposed design methodology. Also, on the one hand, the results due to low-frequency small-signal analysis, when considering all of the transistor components, are highly accurate and allow the designer which parameters must be redesigned. The same is true, if needed, to redesign open-loop gain or output resistance. On the other hand, high-frequency small-signal models help us to reduce the simulation time compared to transistor level circuits. Finally, it is important to underline that analog design is an engineering discipline supported by laws of physics, where some of them are included into this design methodology.

Acknowledgment

This work is supported by the Mexican Council of Science and Technology (CONACyT) under grant 169660.

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