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Improved High Speed, Low Power CMOS Multiplier

[Ameen Bin Obadi and Alaa Hussein]

***Abstract*—A high speed four quadrant current mode multiplier is presented. It is based on CMOS devices arranged in dual trans-linear loops and working in saturation region. The designed circuit operates under the voltage supply of ±1.5V. Design simulation was carried out using Tanner EDA Tools v13.0 with level 49 parameters (BSIM3 v3.1) in 0.35µm standard CMOS technology. Simulation results show that the multiplier has a 3dB bandwidth of 440MHz, linearity error of 1.1% and maximum power consumption of 158µW. The analog multiplier is used to carry out amplitude modulation whose results are also reported.**

***Keywords*— CMOS multiplier; translinear loop; current mode; squarer circuit; four quadrant.**

I. Introduction

The multiplier circuit is a fundamental part of most signal processing systems. Many linear/nonlinear functions can be synthesized using multipliers such as multiplication, division, modulation, demodulation, rectification, automatic gain controlling and phase locked loop [1, 2].

Currently, speed, power consumption and linearity are the key parameters in the design of high-performance mixed-signal integrated circuit. Since current mode circuits experience better performance than their voltage-mode counterpart part in terms of the mentioned criteria, design of multipliers in current mode is widely adopted in the literature [2,8].

Most of the reported current mode continuous time multipliers fall in different category of circuits such as: trans-linear principle of MOSFET in sub-threshold [6, 7, 9], square low of MOSFET in saturation [1, 2, 8] or class AB circuits [3, 10]. Almost, all of the different designs depend on the basic principle of design square-difference identity [1, 3].

In this paper, a four quadrant analog current mode multiplier which is an improved version of [1] with higher bandwidth, lower power consumption and enhanced input impedance is proposed. It utilizes dual trans-linear loops of MOS transistors operating in saturation. The circuit works under the supply voltage of ±1.5V, consumes around 158µW of power and operates up to a frequency of 440MHz. This multiplier is used as an amplitude modulator. Tanner EDA simulation results are presented.

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II. Description of Proposed Circuit

A. *Current Squarer Cell*

The current multiplier circuit is designed based on the basic trans-linear loop cell (squarer) shown in fig.1. The trans-linear loop consists of transistors N_1, N_2, P_1 and P_2 which are all biased in saturation region. The relationship between the drain current (I_D) and the gate to source voltage (V_{GS}) of a transistor operating in saturation is given by [1]:

$$I_{DS} = K(V_{GS} - V_{th})^2 \quad (1)$$

$$V_{GS} = V_{th} + \sqrt{\frac{I_{DS}}{K}} \quad (2)$$

Where V_{th} is the threshold voltage, $K = 0.5\mu_o C_{ox}(\frac{W}{L})$ is the trans-conductance parameter of the transistor, μ_o is the electron mobility, C_{ox} is the oxide gate capacitance and $\frac{W}{L}$ is the transistor aspect ratio.
By using KVL in the trans-linear loop gives:

$$V_{GS(P\_1)} + V_{GS(N\_1)} = V_{GS(P\_2)} + V_{GS(N\_2)} \quad (3)$$

Assuming the four transistors are biased in saturation, well matched and having the same value of trans-conductance parameters ($K_n = K_p$), and considering that:

$$I_{DS(N\_2)} = I_{DS(P\_2)} = I_B \quad (4)$$

Where I_B is the biasing current.

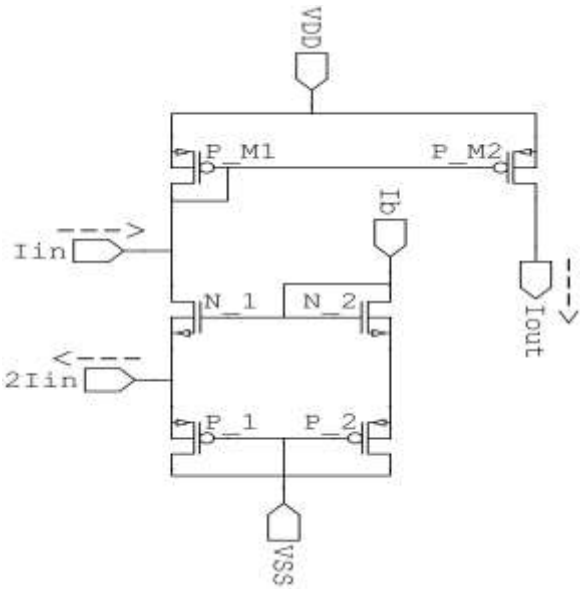

Fig. 1 Current squarer circuit

Then using eq.(2) into (3) yields:

$$\sqrt{I_{DS(P\_1)}} + \sqrt{I_{DS(N\_1)}} = \sqrt{I_{DS(P\_2)}} + \sqrt{I_{DS(N\_2)}} \quad (5)$$
$$\sqrt{I_{DS(P\_1)}} + \sqrt{I_{DS(N\_1)}} = 2\sqrt{I_B} \quad (6)$$

In order to find the relation between I_{in} & I_{out}, KCL equations at the source and at the drain of transistor N_1 will be written:

$$I_{DS(N\_1)} = I_{in} + I_{out} \quad (7)$$
$$I_{DS(P\_1)} = I_{out} - I_{in} \quad (8)$$

Now, by substituting (7) & (8) into (6) and squaring both sides:

$$4I_B = (I_{in} + I_{out}) + (I_{out} - I_{in}) + 2\sqrt{{I_{out}}^2 - {I_{in}}^2} \quad (9)$$
$$4I_B - 2I_{out} = 2\sqrt{{I_{out}}^2 - {I_{in}}^2} \quad (10)$$
$$16{I_B}^2 - 16I_B I_{out} + 4{I_{out}}^2 = 4({I_{out}}^2 - {I_{in}}^2) \quad (11)$$

Then the output current of fig.1 can be written as:

$$I_{out} = \frac{{I_{in}}^2}{4I_B} + I_B \quad (12)$$

It is clear from (12) that the circuit in fig.1 represents a current squarer function. This squarer cell will be the basic building block in the analog multiplier.

B. *Four Quadrant Multiplier*

The circuit shown in fig.2 represents the proposed four quadrant current mode multiplier. The key principle of operation of the proposed multiplier is based on the square – difference identity:

$$(x + y)^2 + (x - y)^2 = 4xy \quad (13)$$

The proposed multiplier contains two squaring cells. Transistors N_1, N_2, P_1& *P*_2 constitute the first squarer with input $(I_x + I_y)$. The resulting output through transistor P_M2 is given by:

$$I_{out1} = \frac{(I_x + I_y)^2}{4I_{B1}} + I_{B1} \quad (14)$$

The other squarer is composed of transistors N_3, N_4, P_3& *P*_4 with input$(I_x - I_y)$. The resulting output through transistor P_M4 is given by:

$$I_{out2} = \frac{(I_x - I_y)^2}{4I_{B2}} + I_{B2} \quad (15)$$

The resulting output (I_{out}) of the multiplier is the subtraction of I_{out1}& I_{out2} :

$$I_{out} = I_{out1} - I_{out2} \quad (16)$$
$$I_{out} = \frac{(I_x + I_y)^2}{4I_{B1}} + I_{B1} - \frac{(I_x - I_y)^2}{4I_{B2}} + I_{B2} \quad (17)$$

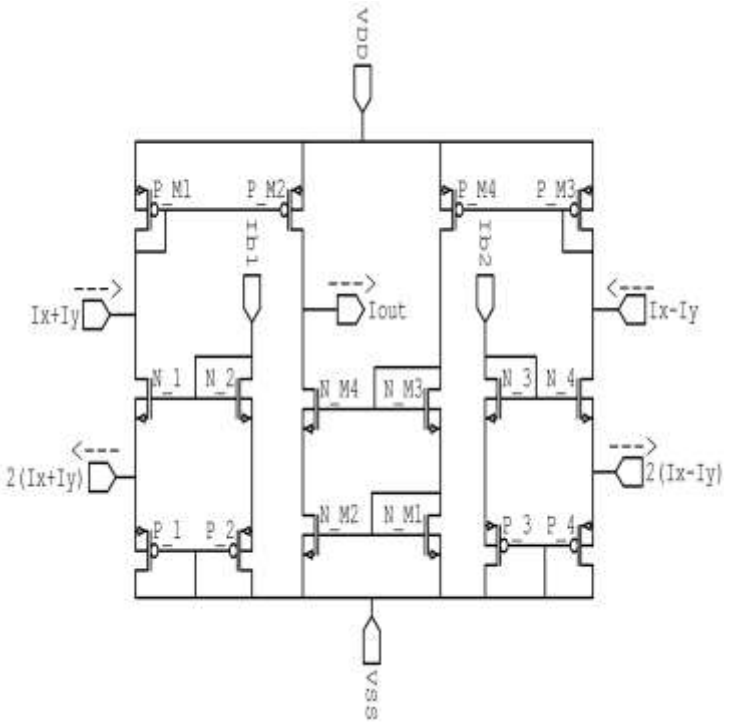

Fig. 2 Proposed current multiplier circuit

Since $I_{B1} = I_{B2} = I_B$ (constant biasing current $= 10uA$) , then:

$$I_{out} = \frac{I_x I_y}{I_B} \quad (18)$$

From (18) it is obvious that the proposed circuit functions as multiplication of two signals $(I_x \& I_y)$ and division by (I_B).

One advantage of this circuit over the one reported in [1], is that it can operate at higher frequencies due to the reduction of the parasitic capacitance generated by the cascade current mirror used. Another addition to this circuit is that the output node is distinct from the input nodes. The high impedance node at $(I_x - I_y)$ in the circuit reported in [1] is used as both input and output node at the same time.

However, in the proposed circuit of fig.2 the two nodes are separated so that the input current node for $(I_x - I_y)$ is at low impedance and the output node for (Iout) is at high impedance. Approximate impedances at all concerned nodes are listed below:

- Input impedance at $(I_x + I_y)$ node:

$$\frac{1}{g_{m(P\_M1)}} // [r_{\circ(N_1)} \left(1 + g_{m(N\_1)} \left(\frac{1}{g_{m(P\_1)}}\right)\right)] \approx \frac{1}{g_{m(P\_m1)}} \quad (19)$$

- Input impedance at $2(I_x + I_y)$ node:

$$\frac{1}{g_{m(P\_1)}} // [\frac{1}{g_{m(N\_1)}} \left(1 + \frac{1}{r_{\circ(N\_1)} * g_{m(P\_M1)}}\right)] \approx \frac{1}{2g_{m(P\_1)}} \quad (20)$$

- Input Impedance at $(I_x - I_y)$ node:

$$\frac{1}{g_{m_{(P\_M3)}}} //[r_{\circ_{(N\_4)}}\left(1 + g_{m_{(N\_4)}}\left(\frac{1}{g_{m_{(P\_4)}}}\right)\right)] \approx \frac{1}{g_{m_{(P\_M3)}}} \quad (21)$$

- Input Impedance at $2(I_x - I_y)$ node:

$$\frac{1}{g_{m_{(P\_4)}}} //[\frac{1}{g_{m_{(N\_4)}}}\left(1 + \frac{1}{r_{\circ_{(N\_4)}} * g_{m_{(P\_M3)}}}\right)] \approx \frac{1}{2g_{m_{(P\_4)}}} \quad (22)$$

- Output impedance at (I_{out}) node:

$$r_{\circ_{(P\_M2)}} //[r_{\circ_{(N\_M4)}}\left(1 + g_{m_{(N\_M4)}} r_{\circ_{(N\_M2)}}\right)] \approx r_{\circ_{(P\_M2)}} \quad (23)$$

Where in all above equations $r_{\circ_x}$ and g_{m_x} are the output resistance and trans-conductance of transistor x respectively.

III. Simulation Results

The simulation of the design was carried out to verify the circuit operation and the theoretical analysis. The analog multiplier in fig.2 is simulated using Tanner with level 49 model parameters (BSIM3 v3.1) of 0.35µm standard CMOS technology. The supply voltages used are $V_{DD} = 1.5\,V$, & $V_{SS} = -1.5\,V$, I_{B1}& I_{B2} are set at value of 10µA and the output port is connected to a 1kΩ resistor.

Fig.3 shows the DC transfer characteristic of the proposed multiplier/divider when both inputs $(I_x$ & $I_y)$ are varied between $-10\mu A$ & $10\mu A$. The results from the figure agree well with the theory. It shows that the circuit operates correctly as a four quadrant multiplier. The Linearity error of the proposed circuit is around 1.1% and the power consumption is about 158 µW.

Fig.4 shows the transient operation of the multiplier having both inputs $(I_x$ & $I_y)$ as sinusoidal signals at 1MHz with two differet amplitudes. The resulting output agrees well with the theory.

The frequency response of the proposed multiplier/divider is presented in fig.5. The 3dB bandwidth of the circuit is about 440MHz. This high bandwidth achieved by the circuit is due to the reduction of the high parasitic capacitance values generated by the cascade mirror in the multiplier circuit of [1].

The use of the circuit as a divider of two currents is shown in fig.6 in which I_B & I_y are varied, while I_x is kept fixed at $10\mu A$. However, since I_B is the biasing current for the circuit, it can be varied only up to some extent in which transistors are still guaranteed to be biased in saturation.

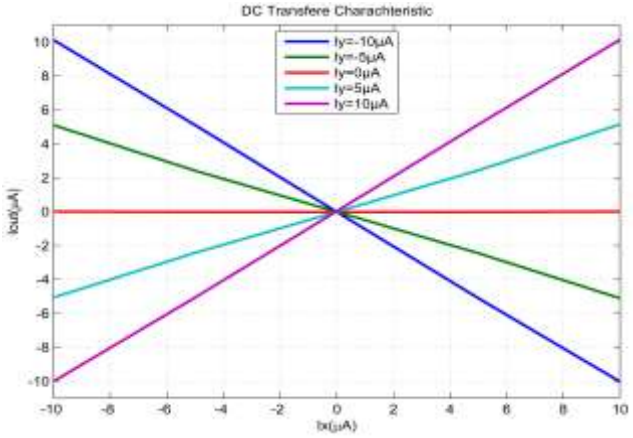

Fig. 3 DC transfer characteristic of the proposed multiplier/divider

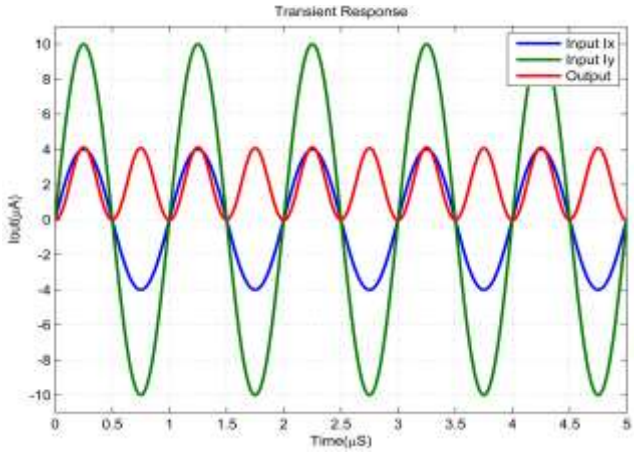

Fig. 4 Transient response of the proposed multiplier/divider

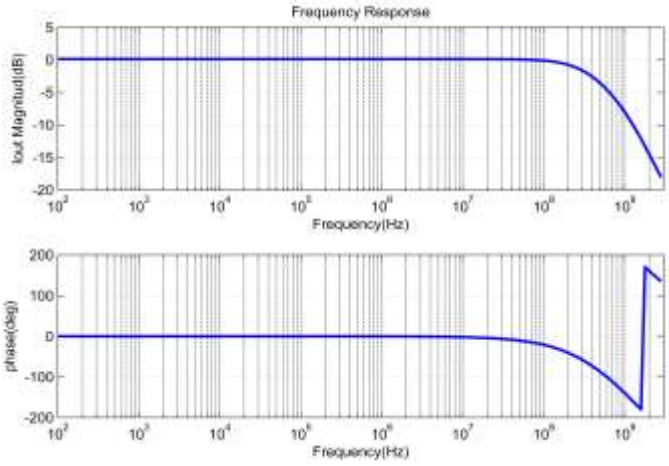

Fig. 5 Frequency response of the proposed multiplier/divider

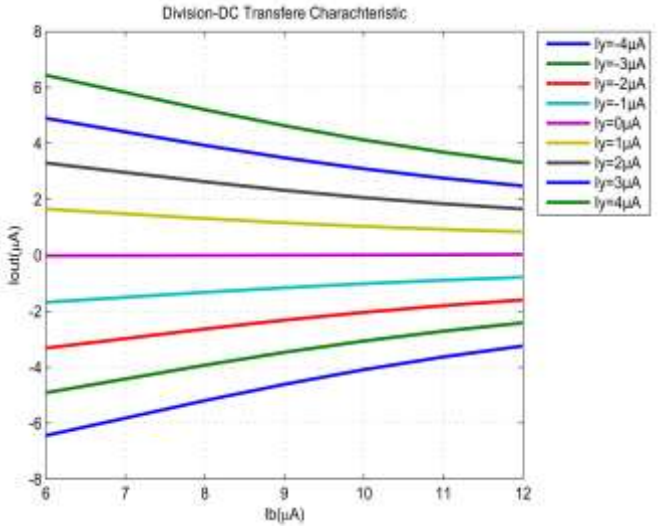

Fig. 6 DC characteristic of the multiplier working as a divider, Ix=10uA

One of the applications of the proposed multiplier in fig.2 is to be used as a modulator. This process requires two signals one is the carrier (high frequency) and the other is the modulating signal (lower frequency). The proposed circuit is used to achieve this process by having Ix as the modulating signal with frequency=10 kHz, amplitude=10μA, and Iy as the carrier with frequency=500 kHz and amplitude=10μA. Simulation results of the input and output waveforms are shown in fig.7.

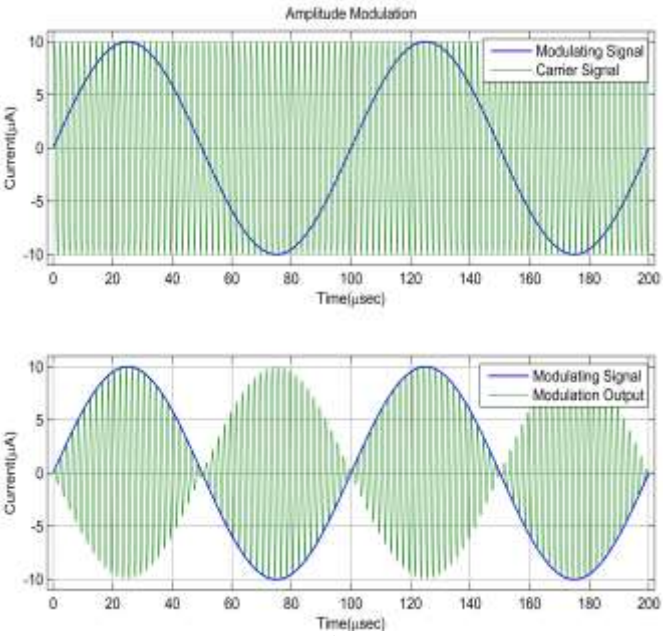

Fig. 7 Simulation results of the amplitude modulation

IV. Conclusion

In this work, an improved four quadrant current mode CMOS analog multiplier based on current squarer was presented. It was designed and simulated using Tanner Tools software. The multiplier achieved a −3dB bandwidth of 440MHz, linearity error of 1.1% and power consumption of about 158 μW . Comparison of the key performance parameters between the designed multiplier and previously reported works is shown table (I). It is clear that the attractive features of the proposed circuit are mainly the high frequency operation, low power consumption and enhanced output impedance. The operation of the proposed circuit as a modulator is verified as illustrated in fig.7. In addition, it can be used in analog VLSI circuit for low power and high speed applications such as variable gain amplifier, filters and phase locked loop.

TABLE I. COMPARISON BTWEEN PROPOSED MULTIPLIER AND PREVIOUS MULTIPLIERS

	[1]	**[3]**	**[5]**	**[8]**	**[12]**	**This Work**
Power supply (V)	+3.3	±1.5	±1.2	+1.8	+3.3	±1.5
Power cons. (μW)	340	460	1200	207	240	158
Linearity error (%)	1.1	1.2	-	-	1.15	1.1
Bandwidth (MHz)	41.8	19	1740	31.2	44.9	440
Technology (μm)	0.35	0.5	0.35	0.18	0.35	0.35

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