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A CMOS Envelope Tracking Power Amplifier with Hybrid Bias Modulator

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***Abstract*—This paper presents an envelope tracking power amplifier (ET PA) using a hybrid bias modulator for mobile terminal applications. The hybrid bias modulator consists of a linear amplifier and a switching amplifier. The CMOS PA has a two-stage single-ended structure. For 1.75-GHz long-term evolution signal with 5-MHz bandwidth, 7.3-dB peak-to-average power ratio (PAPR), and 16-quadrature amplitude modulation, the CMOS ET PA delivers a power-added efficiency (PAE) of 30.5 %at an average output power of 21dBm. The ET PA also delivers a PAE of 24.2 % at average output power of 17 dBmwhich is 6.9 % higher than that of the stand-alone PA.**

***Keywords*—hybrid bias modulator, wireless communication technology,CMOS power amplifier, envelope tracking power amplifier, LTE mobile application**

I. Introduction

The wireless communication system has evolved for higher data rates with wide bandwidth and high peak-to-average power ratio (PAPR). To meet the stringent linearity standard such as 4th generation communication systems like long-term evolution (LTE), LTE-advanced andWiBro-Evolution, the power amplifier (PA) has to operate at back-off power region, where the PA has low efficiency due to the fixed supply voltage. PAs account for the majority of the power consumption aspects in communication systems. Therefore studies to design power amplifiers with the high linearity and high efficiency has been progressed actively.

The various techniques for the PA efficiency improvement are Doherty, Envelope Elimination and Restoration (EER), Envelope Tracking (ET) and so on. Among the techniques, the ET technique is one of the most suitable solutions when considering the linearity and the efficiency aspects. The ET technique improves the efficiency of the PA at the back-off power region by modulating the supply voltage of the PA. Recently, studies on a hybrid bias modulator of ET technique is discussed. The hybrid bias modulator consists of the linear amplifier for the wide bandwidth and the switching amplifier for the high efficiency.

In this paper, the principle of ET technique is demonstrated and optimum operating condition for ET PA is analyzed. The PA is implemented using a 0.18-μm CMOS process and the hybrid bias modulator is designed using a 65-nm CMOS process. Experimental results of the fabricated CMOS ET PA will be shown compared to the stand-alone PA.

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II. Two-stage CMOS ET PA Design

A. *Envelope Tracking Modulation Technique*

The EER and ET techniquesto modulate the drain voltage of PA according to the input signal of the PA improve theefficiency of the PA.In EER systems, EER composed of a high efficiency switching mode PAs (class D or E). Theinput of the PA is the phase modulated RF signal clipped by the limiter and had a constant envelope as shown in Fig. 1.So the power amplifiers of the EER system have high efficiency, low linearity characteristics of switching mode PAs. Unlike EER systems, the original RF signal is supplied to the input of the PAin ET systems. Therefore ET systems utilize a linear mode PAs (class A or AB) to amplify the RF input signallinearly as shown in Fig. 2.

The efficiency of power amplifiers is calculated as the output power (P_{output}) divided by the input power (P_{input}) or DC power consumption (P_{DC}) as represented below:

$$\eta_{PA} = \frac{P_{output}}{P_{input}} \qquad (1)$$

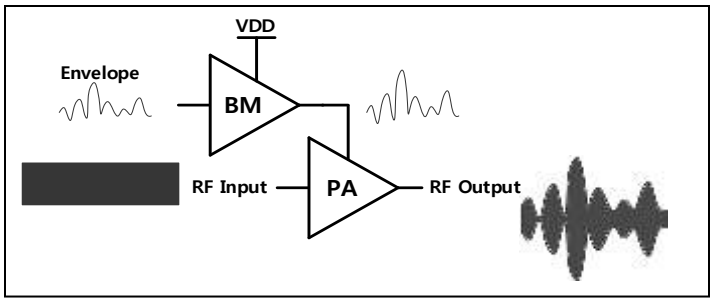
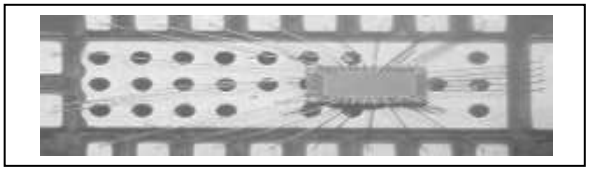
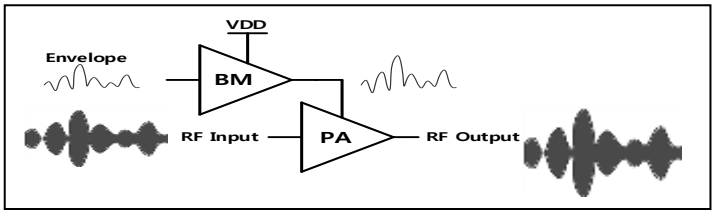


Figure 1. Block diagram of EER systems.

Figure 2. Block diagram of ET systems.



The following equation isefficiency of bias modulators



(BM). It is calculated as the output power (P_{output}) divided by the DC power consumption.

$$\eta_{BM} = \frac{P_{output}}{P_{DC}} \qquad (2)$$

The output power is expressed as the product of load current and average output voltage of the bias modulator.

$$P_{out} = V_{avg.of\ output} \cdot I_{load} \quad (3)$$

The overall efficiency consists of the product the efficiency of power amplifiers and the efficiency of bias modulators as shows the following equation.

$$\eta_{overall} = \eta_{PA} \cdot \eta_{BM} \quad (4)$$

Therefore the efficiency of power amplifiers and bias modulators are both important to improve the overall efficiency [1].

B. Design of Hybrid Bias Modulator

The hybrid bias modulator consists of the linear amplifier for the wide bandwidth and the switching amplifier for the high efficiency, as shown in Fig. 3.

The linear amplifier and switching amplifier operates as the voltage-controlled-voltage source (VCVS). The output stage of the linear amplifier is designed with Class-AB buffer for linear operation and efficiency.

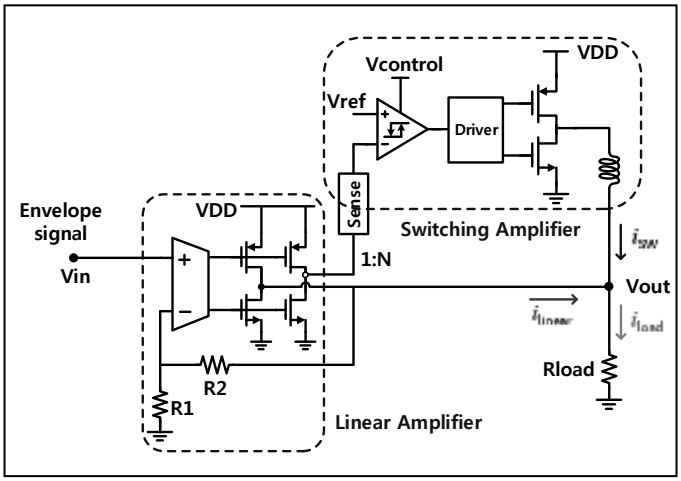


Figure 3. Block diagram of the hybrid bias modulator.

Figure 4. Chip microphotograph of the hybrid bias modulator in a 65-nm CMOS process.

The switching amplifier operates as the current-controlled-current source (CCCS) and supplies most of the current to the load and the linear amplifier provides the rest current and compensates for the ripple current from the switching amplifier.

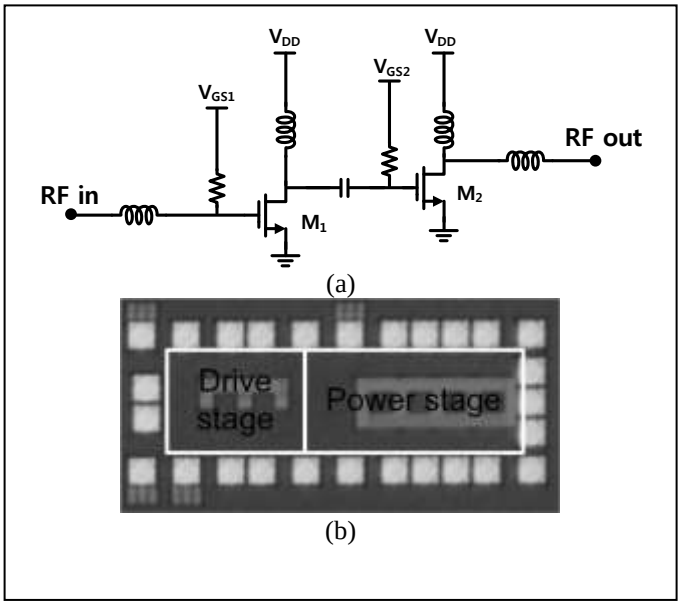
The switching amplifier is composed of a comparator, a driver, and a power switch. The sensed current from the output current of the linear amplifier is compared with the reference voltage at the comparator. The driver generates a dead-time in order to prevent the shoot-through current of the power switch. A size of the power switch is carefully decided by taking the slew rate, the efficiency, and the load condition into account [2].

C. Design ofTwo-stage Power Amplifier

Fig. 5(a) shows a schematic diagram of the CMOS PA.The PA utilizes a single-ended structure and two-stage in order to achieves sufficient gain. Fig. 5(b) shows the chip microphotograph with a chip area of 1.0 × 0.46 mm^2, including bonding pads and the PA is fabricated using a 0.18-μm CMOS process.

For a 1.75GHz single-tone signal, a power gain of 22.5 dB and a power-added efficiency (PAE) of 43.9 % are delivered at an output power of 24.5 dBm with a supply voltage of 3.3 V.

Figure 5. The CMOS power amplifier. (a) chip microphotograph. (b) schematic diagram.



III. ET CMOS PA Experimental Results

The entire ET-based PA system has the CMOS PA IC and the hybrid bias modulator IC, as shown in Fig. 6. The CMOS PA implemented using a0.18-μm CMOS process and the hybrid bias modulator is fabricated using a 65-nm CMOS process. The baseband I and Q signals of LTE 16 quadrature amplitude modulation (16 QAM) 5 MHz are generated using Agilent signal studio. An envelope signal for ET is handled by Matlab program. As shown in Fig. 9, an experiment stand for measurement of the ET PA. The two signal generators (E4438C) and a spectrum analyzer (E4440A) are synchronized by a pattern trigger. The delays between the RF signal path and the envelope signal path are adjusted throughthe RF signal generator.

The CMOS PA under the ET operation use an envelope-shaping function to operate in saturation condition, as shown in Fig. 7 [3], [4].With the envelope shaping, the ET PA achieves improved efficiency over a dynamic range.Fig. 8 shows the measured performances of the stand-alone PA and the two-stage CMOS ET PA for an LTE signal at 1.75 GHz with 5 MHz bandwidth (BW), 16 QAM, and 7.3 dB PAPR. Fig. 8(a)shows the measured gain and PAE comparison of the stand-alone PA and ET PA. Fig. 8(b) shows the measured evolved universal terrestrial radio access (E-UTRA)adjacent channel leakage ratio (ACLR) performances of the stand-alone PA and ET PA.At an average output power of 21 dBm, the stand-alone PA with supply voltage of 3.3 V delivers a PAE of 29.6 %, a gain of 22.2 dB, and an ACLR of -31 dBc and the ET PA achieves a PAEof 30.5 %, a gain of 20.1 dB, and ACLR of -30 dBc. The ET PA also delivers a PAE of 24.2 % at average output power of 17

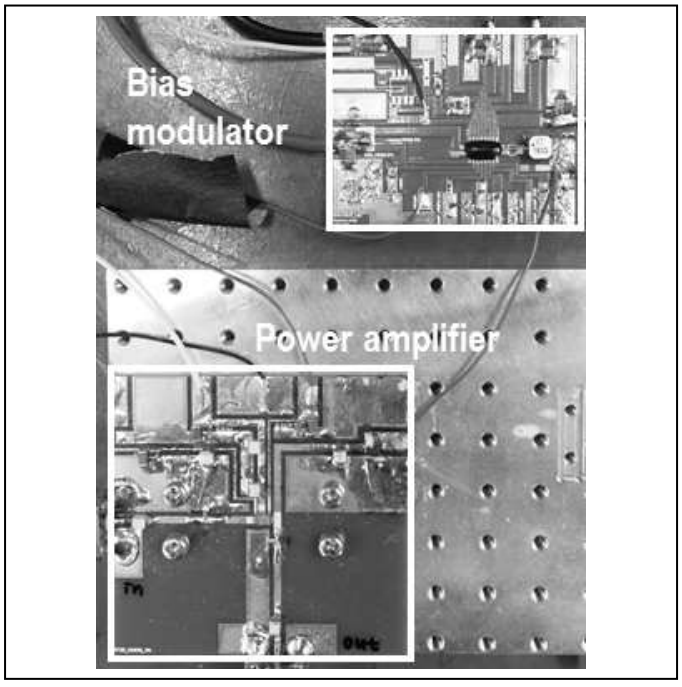


Figure 6. Evaluation board of the ET-based PA system.

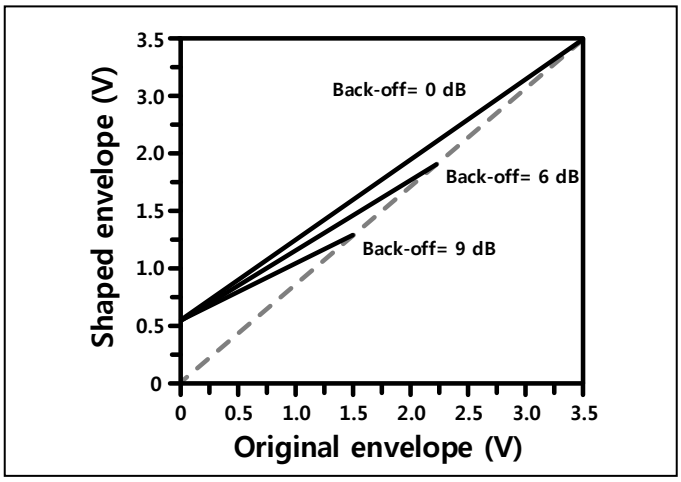


Figure 7. Envleope-shaping functions.

dBm, which is 6.9 % higher than that of the stand-alone PA. The PAE of the ET PA includes the current consumption of the hybrid bias modulator. The performance comparison of the ET PA for LTE application is summarized in Table I.

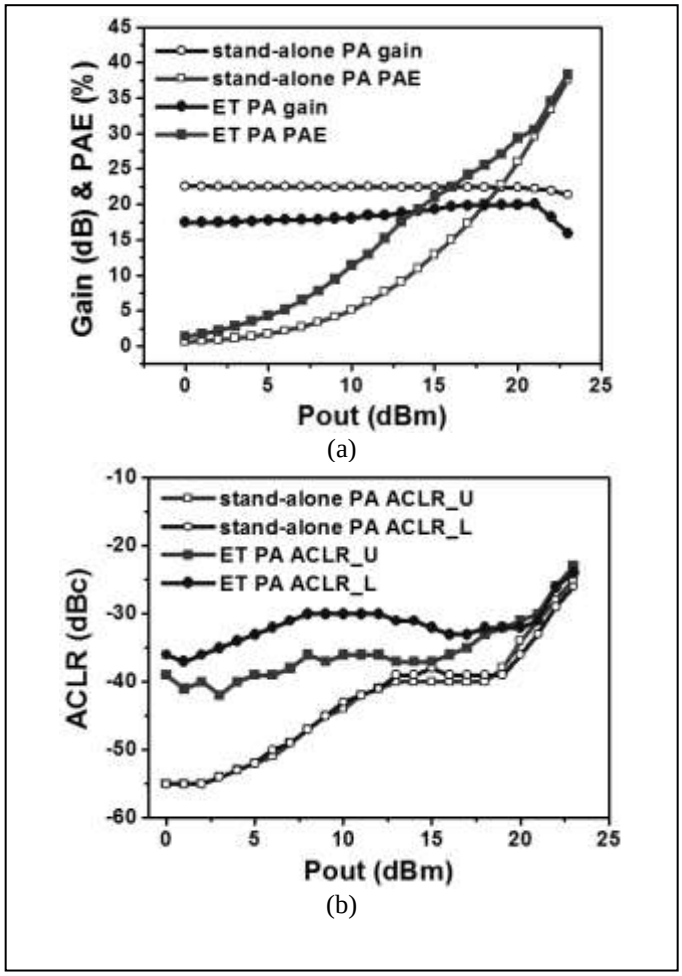


Figure 8. Measured performances of the stand-alone PA and ET PA: (a) gain and PAE. (b) ACLR.

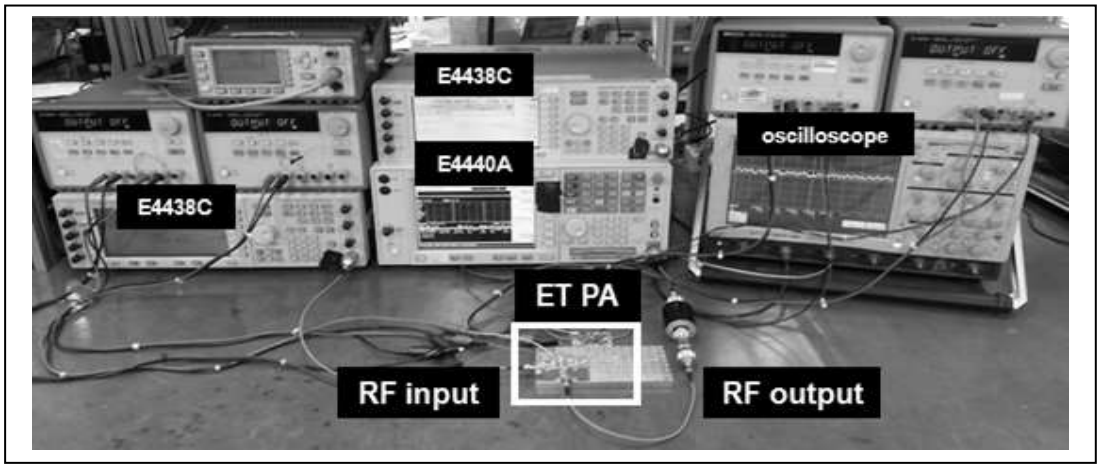


Figure 9. Experiment stand for measurement of the ET PA.

IV. Conclusion

A CMOS ET PA was designed and fabricated. ThePAand the hybrid bias modulator were designedusinga 0.18-μm and 65-nm CMOS processes, respectively. For the 16QAM LTE signal with 7.3 dB PAPR and 5 MHz BW, the ET PA achieves a PAE of 30.5 %, a gain of 20.1 dB, and a E-UTRA ACLR of -30 dBc at an average output power of 21 dBm.It also delivers a PAE of 24.2 % at average output power of 17 dBm, which is 6.9 % higher than the stand-alone PA. These results represent that the ET PA can improve efficiency for the future wireless communication systems, such as 4G LTE or beyond.

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TABLE I. PERFORMANCE COMPARISON OF THE ET PA

Ref.	Application		PAPR (dB)	Supply (V)	Freq. (GHz)	Pout (dBm)	Gain (dB)	ACLR (dBc)	Technology	
	Modulation	*BW (MHz)*							*PA*	*BM*
[3]	LTE 16-QAM	10	7.44	5	1.85	28.9	24.5	-	2-μm InGaP/GaAs	0.13-μm CMOS
[4]	LTE 16-QAM	10	7.5	5/3.4	1.8	26	9	-32.5	0.18-μm CMOS	0.18-µm CMOS
[5]	LTE 16-QAM	10	-	5/2.5	1.74	27	28.3	-35.7	2-μm InGaP/GaAs	0.18-µm CMOS
[6]	LTE 16-QAM	5	7.5	4.2	1.75	24.2	19.5	-	0.35-μm SiGe BiCMOS	0.35-µm SiGeBiCMOS
[7]	LTE 16-QAM	10	7.5	5	1.85	26	10	-34.2	0.18-μm CMOS	0.18-µm CMOS
[8]	LTE 16-QAM	5	-	4.2	1.9	23.1	15		0.35-μm SiGe BiCMOS	0.35-µm SiGe BCDMOS
This work	LTE 16-QAM	5	7.3	3.3	1.75	21	20.1	-30	0.18-μm CMOS	65-nm CMOS

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