

# An Analytic Potential Solution to Ge/Si Core/Shell Field effect Metal-Oxide-Semiconductor Structure

Lining Zhang, Yun Ye, Wen Wu, Wengping Wang, Mansun Chan, Wei Zhao, Caixia Du, Wanning Deng, Jin Yang, and Jin He

**Abstract**—Radial core/shell hetero field effect metal-oxide-semiconductor structures, especially Ge/Si core/shell structure, have recently been extensively studied both experimentally and theoretically, promising novel electronic and optoelectronic devices. An analytic electrostatic potential solution to this hetero-structure is developed in this letter. The analytical expression of the electrostatic potential is derived out from the basic Poisson Boltzmann equation in the core/shell layers under classical device physics. Potential and electric field distribution across the radial of the core/shell structure are analyzed and discussed in the detail, much different from their single component counterpart. The analytic solution presented in this letter has provided useful insight for device scientists and integrated circuit engineers to understand the device physics and further develop compact circuit models of nano-wire field effect transistors with the Ge/Si core/shell hetero-structure for possible circuit application.

**Keywords**—CMOS scaling, nanowire device, integrated circuit, hetero-junction structure, device physics, simulation and modeling

## I. Introduction

Radial core/shell hetero-structures have recently been synthesized and demonstrated to have superior electronic and photonic characteristics [1-9]. These results demonstrated the general potential of radial hetero-structures for the development of novel nanowire-based devices [4-5]. The electronic properties of the nanowire devices are Radial core/shell hetero-structures have recently been synthesized and demonstrated to have superior electronic and photonic characteristics [1-9] of much interest to integrated circuit application. As is known, solution to Poisson Boltzmann Equation (PBE) in the semiconductor material is the basis to investigate the electrostatic distribution and dynamic transport of carriers (electrons and holes), which directly determine the electrical transport characteristics of the devices. The high

performance of the core/shell based devices origins from the gate-all-around structure and the hetero-structures, thus, an analytical solution is required to understand the electrical characteristics and current performance of such a structure.

Theory studies on the core/shell structures and devices have also been performed in some published reports. In [10-12] electronic properties of core/shell hetero-structures composed of different materials are investigated by numerical simulation. In [13-14], thermal conductivity along the radial and axial direction of the core/shell structure is studied. The electrical characteristics of the Ge/Si core/shell NWFET are performed using NEFG method, showing excellent transport properties [10]. Though numerical method is powerful in simulating different devices, an analytical solution on the electrostatic property of the core/shell hetero-structure is very important to reduce larger time consumption of numerical simulation and obtain a concise device physics picture. However, the core/shell system is complicated than their single component counterpart, analytic study on this system has not been available so far compared to the fully investigated single material device [15-17].

In this article an analytical electrostatic potential solution is derived for Ge/Si core/shell structure under hole accumulation. We start from the basic PBE within both the germanium and silicon layers. By solving PBE in silicon shell layer separately and then combining with the potential solution in germanium core, the analytic electrostatic potential solution to the Ge/Si core/shell system is derived out in form of a final transcendental voltage control equation. For different gate bias voltages and different core/shell geometries, one can solve the equation using shooting secant method and obtain the potential distribution across the system. Further the carrier distribution can be easily obtained following Boltzmann statistic once the electrostatic property of the system is available.

## II. Analytical solution development

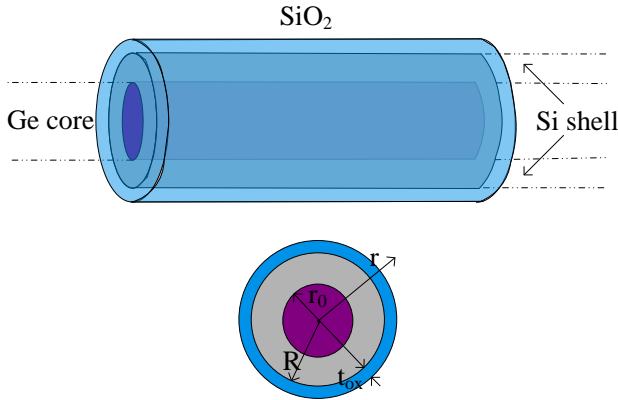
Fig. 1 shows the schematic diagram of the Ge/Si core/shell heterostructure, consisting of a germanium core layer and a silicon shell layer. Here in this article we use the following notations:  $r$  is the coordinate along the radial direction,  $r_0$  is the radius of the core section,  $R$  is the radius of the whole structure and  $t_{ox}$  is the thickness of the dielectric layer, i.e. silicon oxide in this letter. The electrostatic potential is denoted by  $\phi$ , after normalization is  $\omega$ , and  $q$  is the electron

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Lining Zhang, Yun Ye, Wen Wu, Wengping Wang, Mansun Chan, Wei Zhao, Caixia Du, Wanning Deng, Jin Yang, Jin He  
PKU-HKUST Shenzhen-Hongkong Institutions  
China

Lining Zhang, Jin He  
Peking University  
China

charge,  $V_{bi}$  is the self-built voltage of the Ge/Si heterojunction,  $V_t$  is thermal voltage,  $n_{iGe}$  ( $n_{isi}$ ),  $\epsilon_{Ge}$  ( $\epsilon_{si}$ ) and  $L_{Ge}$  ( $L_{si}$ ) are the intrinsic carrier density, the permittivity and intrinsic Debye length of germanium (silicon), respectively.  $V_G$  is gate bias,  $\Delta\phi$  is the work function difference between gate material and intrinsic silicon. The physical parameters of germanium and silicon are taken from [18]. Note that the undoped or lightly doped body is used in the theoretical analysis since it benefits the mobility enhancement proved by the experiment in [4]



1 Schematic diagram of the germanium/silicon core/shell structure.

In silicon shell and germanium core, the Poisson-Boltzmann Equation (PBE) sets can be written as the following form:

$$\frac{1}{r} \frac{d}{dr} \left( r \frac{d\phi}{dr} \right) = - \frac{qn_{iGe}}{\epsilon_{Ge}} \exp \left( \frac{V_{bi} - \phi}{V_t} \right), 0 \leq r \leq r_0 \quad (1)$$

$$\frac{1}{r} \frac{d}{dr} \left( r \frac{d\phi}{dr} \right) = - \frac{qn_{isi}}{\epsilon_{si}} \exp \left( \frac{-\phi}{V_t} \right), r_0 < r \leq R \quad (2)$$

The above equation sets are under the assumptions that (a) electron is negligible in the system, which is always valid when the absolute value of gate voltage is larger than a few thermal voltages; (b) The length of the structure is larger compared to its radius, so the above one dimensional Poisson equation is valid; (c) Boltzmann statistic is applied instead of the Fermi-Dirac one, which is usually the condition when the absolute gate voltage is not too large. This simplification also makes solving the equation sets possible; (d) strain effect and the germanium/silicon interface state are neglected; (e) quantum mechanical effect is not included. Though the above assumptions seem rough, they capture the essential physics and simplify the derivation of our model. Further accounting for these effects in our analytic model deserves the future work.

Equation (2) can be analytically solved as the following form:

$$\phi_{si}(r) = -V_t \ln(2A^2 L_{si}^2 / r^2) - V_t \ln[\beta_{si}(r/r_0)^A] + 2V_t \ln[1 - \beta_{si}(r/r_0)^A] \quad (3)$$

where  $A$  and  $\beta_{si}$  are two dimensionless parameters subject to the boundary conditions. We will see later that Eq.3 is a general solution form for one dimensional PBE in both the shell layer and the core layer of the Ge/Si core/shell structure. The solution of (3) is derived as follows:

Under normalization Eq.2 is expressed as  $\frac{d^2 \omega}{dr^2} + \frac{1}{r} \frac{d\omega}{dr} = \delta e^\omega$  in which  $\delta$  is equal to  $1/L_{si}^2$ , further applying variable transformation of  $\eta = r^2 e^{\phi/V_t}$ ,  $\beta = \frac{r}{V_t} \frac{d\phi}{dr}$  to (2) yields an equivalent differential equation

$$\frac{d^2 \omega}{dr^2} - \frac{1}{r} \frac{d\omega}{dr} - \frac{1}{2} \left( \frac{d\omega}{dr} \right)^2 - \frac{\lambda}{r^2} = 0 \quad (4)$$

The solution to (4) is

$\omega = \ln(2A^2 B / \delta) + (A - 2) \ln(r) - 2 \ln(1 - Br^A)$ , which leads to the above solution of (3).

Eq.1 can also be analytically solved similarly to (3) with the intermediary parameter  $A$  fixed at 2, considering the electric field at the centric point of germanium core is zero.

$$\phi_{Ge}(r) = V_{bi} - V_t \ln(8L_{Ge}^2 / r_0^2) - V_t \ln(\beta_{Ge}) + 2V_t \ln[1 - \beta_{Ge}(r/r_0)^2] \quad (5)$$

The electric field distribution across the structure can be obtained simply by differentiating the electrostatic potential solution (3) and (5) with the radius. Combining (3), (5) and the electric field with Gauss's law at the silicon/oxide interface gives the final voltage control equation:

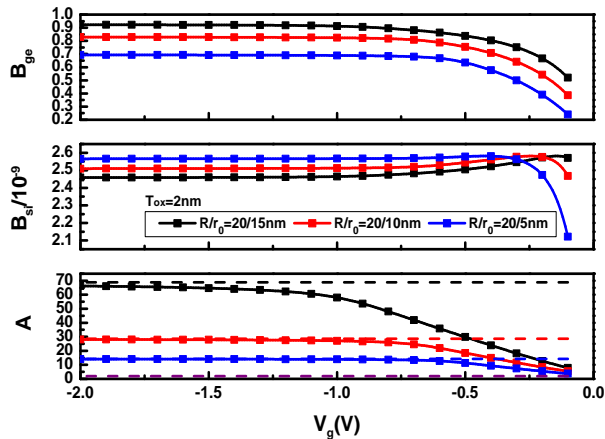
$$-\frac{(V_G - \Delta\phi)}{V_t} = \frac{\epsilon_{si}}{\epsilon_{ox}} \ln\left(1 + \frac{t_{ox}}{R}\right) \left[ (A - 2) + 2A \frac{\beta_{si}(R/r_0)^A}{1 - \beta_{si}(R/r_0)^A} \right] + \ln\left(\frac{2A^2 L_{si}^2}{R^2}\right) + \ln\left[\beta_{si}\left(\frac{R}{r_0}\right)^A\right] - 2 \ln\left[1 - \beta_{si}\left(\frac{R}{r_0}\right)^A\right] \quad (6)$$

The three parameters above can be linked together considering the continuity condition, i.e. the potential and electric flux is continuous at the interface of germanium and silicon according to the basic electromagnetic field theory. After that we can solve the three intermediary parameters for the given bias and structures and give the potential and electric

field distribution in the Ge/Si core/shell structure. The carrier's statistic distribution across the structure can also be obtained.

### III. Result and discussion

In Fig. 2 we show the three parameters as functions of gate bias and structure geometry. As depicted in the figure, the parameter A has an upper limit which is determined only by the geometry. With the absolute gate voltage increases, A is becoming larger and approaching its upper limit. The lower limit of A is 2, just the corresponding value in germanium core region. The parameter  $\beta_{si}$  is always very small, enough accuracy should be taken when solving Eq.6.

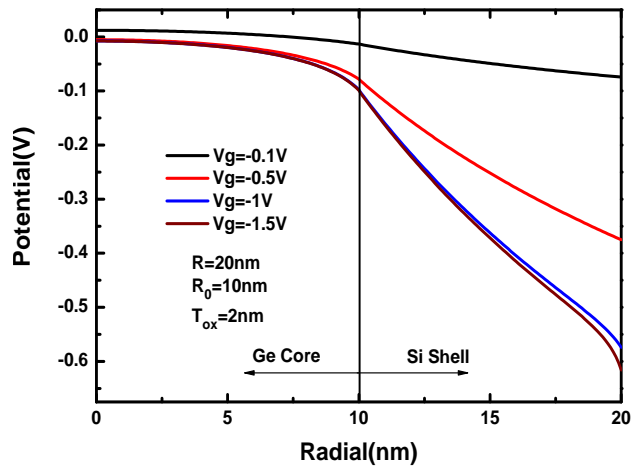


<sup>2</sup> Three intermediary parameters as functions of gate bias for three different geometries. The dashed lines in figure of A-Vg denote the upper limits and lower limit of A.

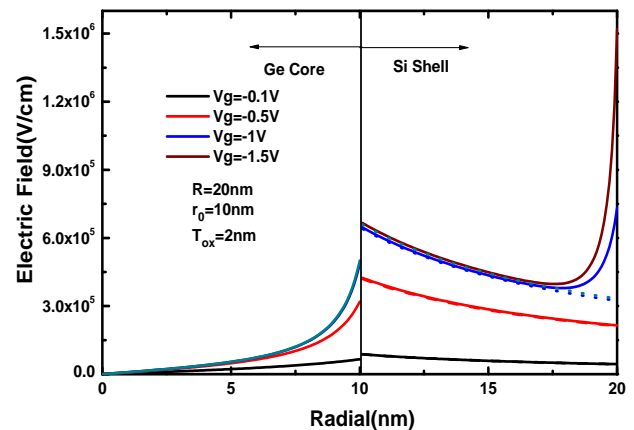
The potential distribution along the radial of the Ge/Si core/shell structure at different gate voltages can be obtained once the intermediary parameters are solved. Fig. 3 presents the analytical electrostatic potential result for one of the geometry structures in Fig. 2. As can be seen from the figure, when the absolute gate voltage is small, the electrostatic potential does not change much along the radial of the structure. "Volume inversion" occurs in both the germanium core and silicon shell, which is similar to the observed phenomenon in nonclassical device, such as DG [19] and SRG [16]. When the absolute gate voltage is larger, e.g. larger than 0.5V, the centric potential in germanium core is not influenced significantly by external bias but the interface potential, volume inversion ends in germanium core while still exist in silicon shell. Further when the absolute gate voltage is larger than 0.8V, the interface potential will also keep unaffected by gate bias, "on" state of this Ge/Si core/shell structure is realized under this operation condition.

As shown in Fig.4 is the electric field distribution along the radial of the same core/shell structure as in Fig.3. It is more clear that at the two lower absolute gate voltages, the electric field in germanium increases sharply from 0 at the centric point of germanium core to the largest value at the germanium/silicon interface, while in silicon it is about inversely proportional to the radial, decreasing from the

largest value at the inner interface to a relative small one at the silicon/oxide interface, following the hyperbolic curve:  $E \propto 1/r$ . That is to say the germanium core is full of carriers but the silicon shell is almost "empty", which is in accordance with the analysis of potential result in Fig.2. When the absolute gate voltage increases, the electric field in germanium core does not change significantly but in silicon shell the electric field gradually departs from the hyperbolic curve. That means carriers begin to accumulate across the silicon shell under this gate bias. At higher gate voltage, electric field in germanium core and inner part of silicon shell stay almost unchanged and that in outer part of silicon shell begin to increase sharply. That is due to higher carrier concentration at the silicon/oxide interface tends to screen the inner parts of the core/shell structure under this gate bias.



<sup>3</sup> Potential distribution across the radial of the core/shell structure under four different gate bias voltages. The structure parameters are marked on the figure.



<sup>4</sup> Electric field distribution across the radial of the same core/shell structure as in figure.3 under four gate bias voltages. The dashed lines in silicon shell denote the approximation result under assumption that no carriers accumulate in the silicon shell. For two smaller gate voltages, the rigorous solution and the approximation coincide with each other. For two larger gate voltages the approximation fails.

## iv. Conclusion

In summary, we developed an analytical electrostatic potential model for germanium/silicon core/shell structure under hole accumulation from basic Poisson-Boltzmann-Equation. The prediction results with the proposed model reveal that the cylindrical structure and radial heterojunction contribute interesting static properties to this structure. Based on the model, the carrier distribution and charge concentration with different geometry structures and external gate voltages can be directly obtained. Therefore, the analytical voltage control equation and its solution in this article have implications for providing a possible method to investigate the dynamic carrier transport characteristic and further develop a compact model for the Ge/Si core/shell NWFET.

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