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Power and Delay Optimization of 1 Bit Full Adder using MTCMOS Technique

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***Abstract*—In this paper, a 28T full adder using MTCMOS technique design is proposed. Combinational logic has extensive applications in quantum computing, low power VLSI design and optical computing. Reducing power dissipation is one of the most principle subjects in VLSI design today. The subthreshold leakage current becomes a large component of total power dissipation. Low- power design techniques proposed to minimize the active leakage power in nanoscale CMOS very large scale integration (VLSI) systems. In this paper the active power and delay of full adder is analyzed with or without MTCMOS. The power and delay evaluation has been carried out using extensive simulation on the HSPICE circuit simulator. The simulation results are based on 32nm and 45nm Berkeley Predictive Technology Model (BPTM). By using MTCMOS technique in full adder a reduction is observed in the active power is 98.3% in 32nm and 99.1% in 45nm. The reduction in the delay is the 21% for sum output and 25% for carry output in 32nm. In 45nm the reduction in delay is 26% for sum output and 29% for carry output.**

***Keywords*—Full Adder, low power, CMOS circuits, MTCMOS, Subthreshold leakage current, simulation**

I. Introduction

As technology increases, silicon technology down scaling continues to meet the increasing demands for higher functionality and better performance at a lower cost. Power dissipation though not entirely ignored, has been of little concern until recently. Another important reason for low power design is reliability. As technology continues to scale not only does the power density increase, but also the current density increases. Therefore, the reliability can only be enhanced if power consumption is reduced [3]. The low power circuit design is very essential in the today's scenario for the fulfillment of green computing, battery life extension and emerging self sustaining applications.

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In this paper, we are going to discuss MTCMOS technique. The MTCMOS technique is an effective technique that provides high performance in the active mode and saves leakage power during the standby mode. The basic principle of the MTCMOS technique is to use low transistors to design the logic gates where the switching speed is essential, while the high V_{th} transistors (also called sleep transistors) are used to effectively isolate the logic gates in standby state and limit the leakage dissipation. The analysis of power reduction involves the implementation of MTCMOS technique as power gating, ground gating and combined gating configuration of power and ground. Multi-threshold CMOS (MTCMOS) is the most commonly used leakage power suppression technique in state-of-the-art integrated circuits In an MTCMOS circuit, high threshold voltage (high-$|V_{th|)}$ sleep transistors (header and/or footer) are used to cut off the power supply and/or the ground connections to an idle low threshold voltage (low-$|V_{th}|$) circuit block [1]

II. Review of Full Adder Design

A 1-bit full adder adds three one bit numbers, often written as A, B and C. A and B is the operands and C is a bit carried in from the next less significant stage. Full adder is usually a component in a cascade of adders, which add 8, 16, 32, 64 etc. binary numbers. The circuit generates a two-bit output sum typically represented by the signals Carry and Sum. Here a full adder is constructed with the help of two half orders by connecting A and B to the input of first half adder, connecting the sum from that to an input to the second adder, connecting C to the other input and OR the two carry outputs. The expression of the sum and carry output is as follows:

$$Sum = A \oplus B \oplus C \quad (1)$$

$$Carry = AB + BC + CA \quad (2)$$

TABLE 1 Truth Table Of Full Adder

Input			Output	
A	***B***	***C***	***Sum***	***Carry***
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

III. Schematic Diagram of 28T Full Adder

A basic cell digital computing system is the 1-bit full adder which has three 1-bit inputs (A, B and C) and two 1-bit outputs (Sum and Carry). The relationship between input and output provided in the equation explained earlier. The CMOS implementation of Full Adder is shown in fig. 1.

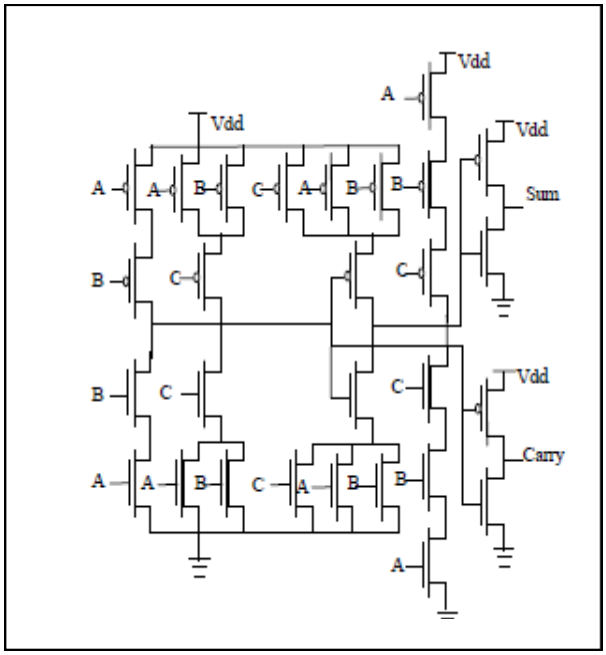

Figure. 1. Coventional 28T CMOS Full Adder

IV. Leakage Reduction using MTCMOS Technique

The continuous scaling of the integrated device design reduces the supply and the threshold voltage of the circuit that leads to an exponential increase in the sub threshold leakage current causing leakage power dissipation. For the effective leakage power reduction, the CMOS circuit is basically designed with low, normal and high threshold voltage transistors in MTCMOS. The low threshold voltage transistors are used to reduce the propagation delay time in the critical path.

On the contrary, the high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path. The implementation is done with active and sleep operation mode.The schematic of MTCMOS power gating technique on full adder is shown in Fig. 2.

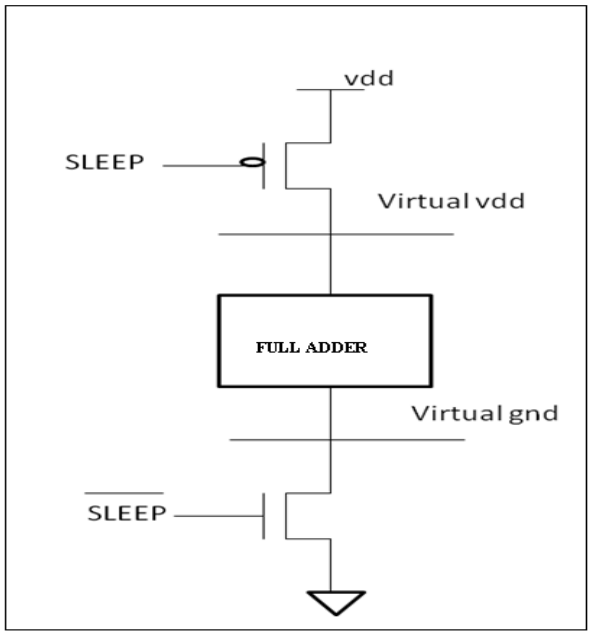

Figure. 2. MTCMOS Implementation in Full Adder

The simulation of the proposed design has been done using HSPICE. The results are shown for the supply voltages of 1V (35nm and 45nm). The data analysis of the input and output of full adder such as A, B, C, sum and carry is shown in Fig. 3.

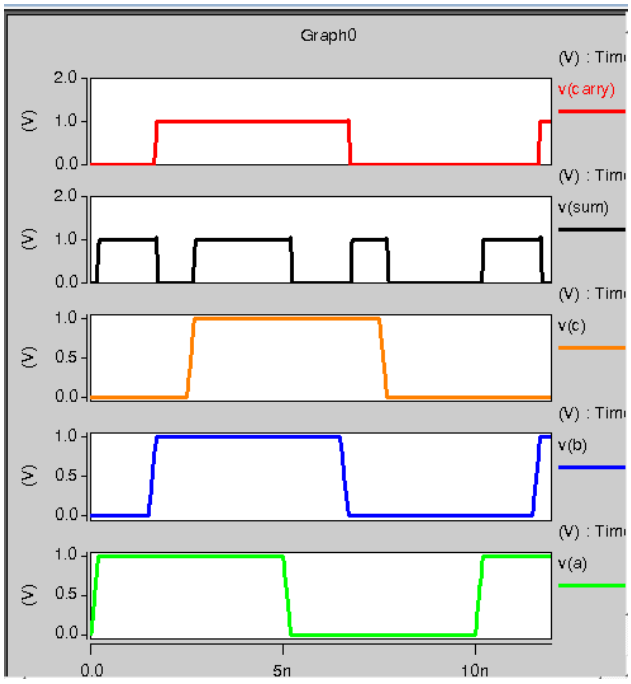

Figure. 3. Sum and Carry output according to applied input

V. Optimization of Power and Delay

Here, at first the 28T full adder circuit is simulated with 32nm channel length i.e. submicron channel with high threshold MOSFET in P-net and N-net. The following results are obtained and shown in Table2.

TABLE II Power and Delay with 32nm Techniques

Parameter	Value (At Input Vector 111)	
	Without MTCMOS	*With MTCMOS*
Average Power consumed	$3.3*10^{-7}$watts	$5.4*10^{-9}$watts
Peak Power Consumed	$9.1*10^{-6}$watts	$7.8*10^{-8}$watts
Delay in Sum Output	1.6ns	1.3ns
Delay in Carry output	1.6ns	1.2ns

Next, the same circuit is simulated with 45nm channel length with low threshold MOSFET in P-net and N-net. The simulation results obtained is shown in Table 3.

TABLE III Power and Delay with 45nm Technique

Parameter	Value (At Input Vector 111)	
	Without MTCMOS	*With MTCMOS*
Average Power consumed	$7.3*10^{-7}$watts	$6.5*10^{-9}$watts
Peak Power Consumed	$4.1*10^{-5}$watts	$1.8*10^{-7}$watts
Delay in Sum Output	1.7ns	1.25ns
Delay in Carry output	1.55ns	1.1ns

VI. Simulation Results

The simulation of transistor level full adder is done by using the HSPICE in 32nm and 45 nm. The behavior of the full adder with or without MTCMOS technique is analyzed in CosmosScope. The simulation results show a reduction in power of full adder in 32nm and 45nm technology. This reduction in power dissipation is shown in Fig. 4 and Fig.5.

The observation of simulation results shows a reduction of power using the MTCMOS technique in both 32nm and 45nm techniques. The significant reduction of approx 98% is achieved using proposed technique.

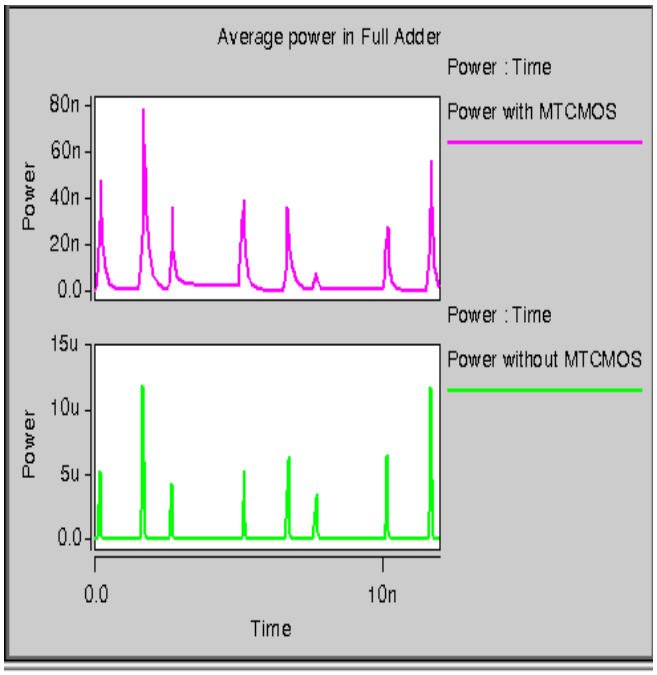

Figure. 4. Power of Full Adder with or without MTCMOS in 32nm technique (*Input Vector 111*)

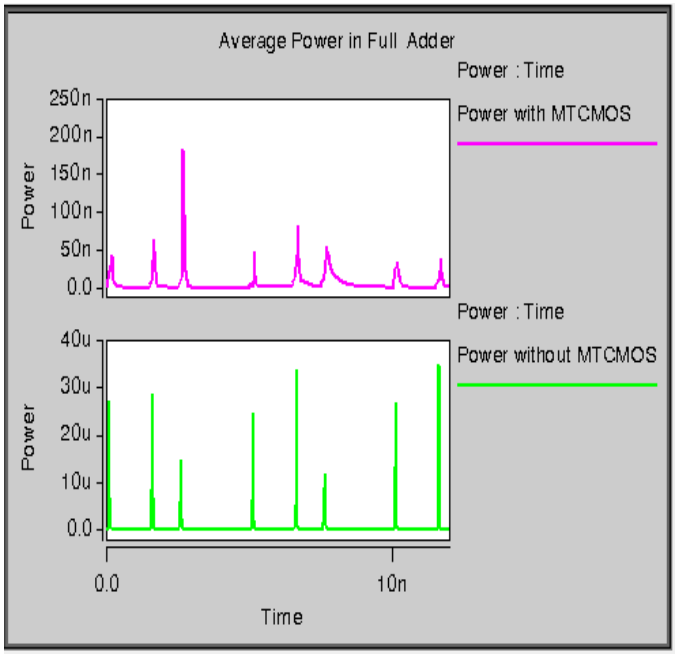

Figure. 5. Power of Full adder with or without MTCMOS in 45nm technique (Input Vector 111)

The Full adder is examined at different input vectors by using HSPICE simulating tool. The observed results are explained in the graphical form in Fig. 6 and Fig. 7.

Average Power in Full Adder without MTCMOS

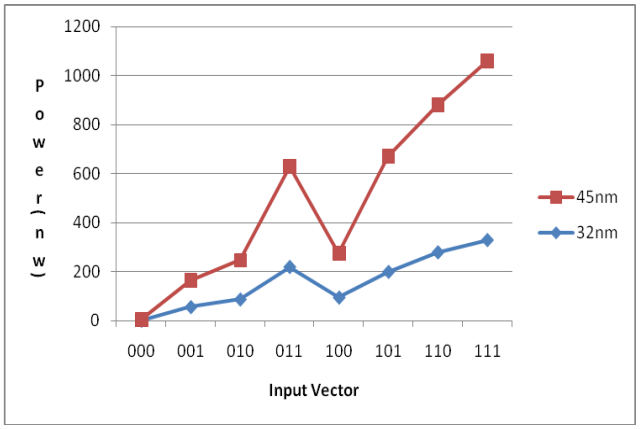

Figure. 6. Power of Full Adder without MTCMOS in different input vector

Average Power in Full Adder with MTCMOS

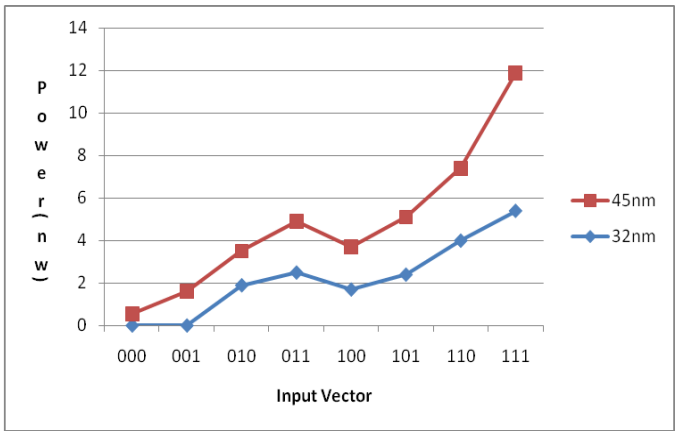

Figure. 7. Power of Full Adder with MTCMOS in different input vector

By observing both the graph, it has been shown that by using MTCMOS in Full Adder the power consumption is reduced by 98%. Thus MTCMOS technique achieves significant reduction in the delay and power.

VII. Conclusion

The performance of digital systems in VLSI design depends largely upon the performance of full adder employed in such systems. The performance of full adder varies as the technology scaling is introduced. In this work, HSPICE simulation of full adder is done at 32nm and 45nm technology using MTCMOS technique to reduce the power dissipation and delay in the full adder design. The simulation result shows lesser power consumption of 98.3% in 32nm and 99.1% in 45nm as compared to conventional full adder. Furthermore, the delay is reduced to 21% for sum output and 25% for carry output in 32nm. In 45nm, improvement in delay is achieved by 26% for sum output and 29% for carry output.

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