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A design approach of an electronic circuit for a low power dissipation

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***Abstract*—we present a design approach to improve the power transfer between the elementary circuits of an electronic system and therefore good energy transfer efficiency for expecting energy leakage minimization.**

***Keywords*—Power supply, low power application, MOS integrated circuits, energy efficiency**

I. Introduction

Within a general framework, the applications using an electric energy are increasing because of their impact on the modernization. For as much the energy efficiency of the systems must be continuously improved in order to minimize the power consumption which is more and more precious.

The necessity for portability of some electronic equipments generated a need for low power battery operating systems like embedded system devices, smart portable devices and hand held multimedia terminals. Low power dissipation is essential in these applications to have reasonable battery life and weight. The ultimate goal in design is closed to have battery-less systems, because the battery contributes greatly to volume and weight.

The various parameters implied in the design of the system elements are recapitulated in Fig.1; the energy consumption is severely constrained by the seven illustrated parameters [1].

In the following, the first part has brought out the mathematical models of the various types of energy consumption in an electronic circuit; in the second and last part, a design technique for the low power dissipation is proposed.

II. Energy consumption sources in an electronic circuit

An active electronic circuit needs external polarization energy to work; it is one of the most necessary energy demands in an electronic circuit and is defined as static.

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In addition to the polarization current, we have during the transient states, the short circuit current, the leakage and conduction current which generate the major energy expenditures; we also have dynamic energy losses from the capacitors and parasitic capacitors of the circuit. The internal noises cause also the considerable losses.

These energy consumption sources can be organized into two main groups relative to the technology and to the frequency.

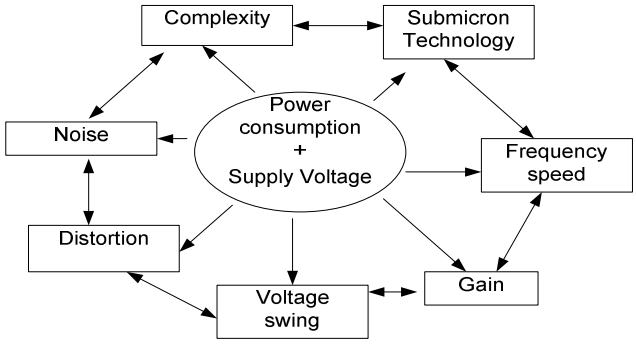


Figure 1: Power supply parameters for electronic system design

In the following, we will focus on an electronic circuit based on the CMOS technology.

III. Global power supply of an electronic circuit

We have in general four power supply sources in a basic CMOS circuit; dynamic (capacitor charge and discharge); static (running and biasing); thermal (by Joule effect) and of short-circuit (during the simultaneous conduction instant of the CMOS circuit transistors). In the logic gate system, more than 90% of the power consumption takes place during transitions between states [2]. For global power supply evaluation in each integrated circuit, let us suppose that it is structured by various elementary functional structures with an input impedance capacitor C (gate capacitor in general) and a conduction resistance Ron as shown in Fig.2. Thus, the input capacitor of each elementary circuit is the load of another one. Hence, the global integrated logic circuit can be modelled by a MOSFET structure.

The basic power supply for a CMOS circuit is evaluated by (1) [3]-[4].

$$P_{IC}(\omega) = \beta C V f V_{DD} + \beta Q_{SC} V_{DD} f + I_{DD} V_{DD} + \beta R_{on} I_{DD}^2 \qquad (1)$$

Where β is the commutation activity (number of transitions per cycle); I_{DD} is the average current supply during

the circuit element time "ON"; f the operating frequency; Q_{SC} is the charge lost due to the short-circuit current towards the mass at each commutation; C is total

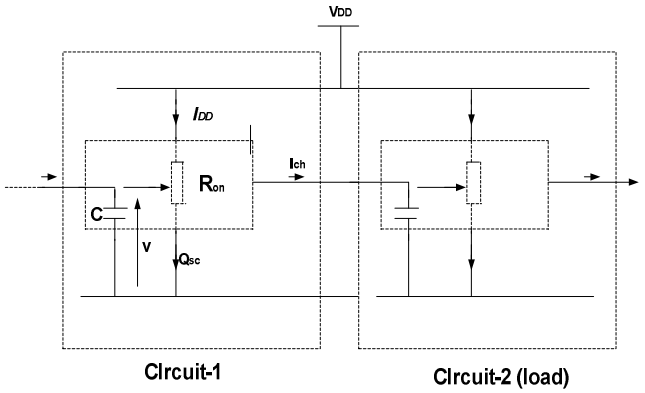


Figure 2: An equivalent functional block of a MOS electronic circuit

capacitor at the various nodes of commutations; R_{on} is the total resistance of the circuit element during conduction instant.

Notice that in our integrated circuit power supply evaluation, we suppose the use of ULV technology, i.e. the charge lost due to the short-circuit current towards the mass will be neglected.

IV. Electronic circuit power supply, optimization and design approach for A low power dissipation

During the conduction instant of the transistors, i.e. circuit in transition states, about the 90% of the energy losses are operated [2]. A low response time and low conduction resistances are the ways to guarantee an attenuation of this large energy expenditure. These conduction resistances and transition time depend on the geometrical parameters of the transistors. It would be thus interested to find an area of agreement between the effectiveness and the low energy expenditure by an optimization of the geometrical parameters.

For this optimization, we have chosen to express the total power consumption in a single CMOS circuit of a system operating in a switching mode in an integrated circuit; it can also be applied to a simple main switching MOS transistor.

According to the different power supply sources described before, we have derived the total power of this CMOS circuit in (2) below.

$$P_{global} = f(C_L + C_{gn} + C_{gp})V^2 + \beta \cdot I_D^2[xR_{on,p} + R_{on,n}(1-x)] + I_{stat}V_{DD} \quad (2)$$

With $C_L = C_g(w_p + w_n)$, $C_{gp} = w_p(C_{ox}\ell + 2C_0)$ and $C_{gn} = w_n(C_{ox}\ell + 2C_0)$.

Here I_D is the average supply current during each elementary conduction time interval; C_g is the gate capacitor per unit of width deduced from the manufacturing process parameters; C_{gp} and C_{gn} are the gate capacitors of the PMOS and NMOS respectively; C_{ox} and C_0 are the process parameters; x is the ratio of the CMOS circuit conduction time to the PMOS conduction time; $R_{on,n}$ is the NMOS conduction resistance defines by (3) below.

$$R_{on,n} = \frac{\ell}{k_n w_n V_{GT}} \quad (3)$$

the same expression can be derived for the PMOS conduction resistance $R_{on,p}$ with the simple substitution of w_n and k_n by w_p and k_p.

According to (3), we can obtain very low resistance values for high w_n values. However, the gate capacitor and the response time will increase with w_n. An optimum must be found. The w_n optimum value must reduce not only the total losses, but also maintain a good response time of CMOS transistors. So, It is very important to find a good ratio between the losses of power, w_n and w_p. The main variables in the global power consumption express by (2) are w_n and w_p. In the CMOS structure, the relation (4) [5] is necessary for the NMOS and PMOS equal response time.

$$\delta = \frac{w_p}{w_n} = \sqrt{\frac{k_n}{|k_p|}} = \frac{1}{\gamma} \quad (4)$$

$$\text{With } \gamma = \frac{R_{on,p}}{R_{on,n}}$$

The optimum expressions of w_n and w_p can be obtained by solving (5) below.

$$\left[\frac{d(P_{global})}{dw_n}\right]_{w_p = cste} = 0 \quad \text{and} \quad \left[\frac{d(P_{global})}{dw_p}\right]_{w_n = cste} = 0 \quad (5)$$

The solution of (5) yields to the optimum geometric parameters $w_{n,opt}$ and $w_{p,opt}$ below.

$$w_{n,opt} = \frac{I_D}{V}\sqrt{\frac{l\beta(1-x)}{k_n V_{GT} f[C_g + (C_{ox}l + 2C_0)]}} \quad (6)$$

$$w_{p,opt} = \delta\frac{I_D}{V}\sqrt{\frac{xl\beta}{k_n V_{GT} f[C_g + (C_{ox}l + 2C_0)]}} \quad (7)$$

According to the expressions (6) and (7), the sourcing current I_{DD} (see Fig.2) depends on both downstream and upstream transistor gate widths. Thus the optimum parameters of the upstream transistors depend on their load circuit. Therefore we should take into account during the design process of a upstream circuit, the corresponding load circuits allowing a good efficiency (i.e. a maximal transfer of supply power from the upstream circuit to its corresponding downstream circuits) ; and then the corresponding average current which will permit an optimum geometric parameter evaluation. So in the following lines, we will derive the design method yields to the good power transfer efficiency and the corresponding supply current for the optimum geometrical parameter calculation.

A. *Energy efficiency, optimization and design method*

Let us suppose that in the CMOS integrated circuit, the various elementary circuit structures have load capacitors of the same values C (gate capacitor in general) as shown in Fig.2, and a corresponding parasitic capacitor αC . The coefficient α represents in general the term which binds the current losses I_{leack_ch} and the total load capacitor C ; it is generally higher than zero for real circuits. Therefore, the total supply current can be defining by (8).

$$i_{DD}(t) = i_{ch}(t) + I_{leack\_ch} \qquad (8)$$

With

$$I_{leack\_ch} = \alpha CfV \qquad (9)$$

and V the control voltage of the load current i_{ch} .

$$i_{ch}(t) = C\frac{dV(t)}{dt} \qquad (10)$$

The total current i_{DD} from the DC source is expressed by (11).

$$i_{DD}(t) = \frac{V_{DD} - V(t)}{R_{on}} \qquad (11)$$

From (8), (9) and (11), we have derived (12) below which is the differential equation for the control voltage V(t) calculation.

$$\frac{V_{DD} - V(t)}{R_{on}} = C\frac{dV(t)}{dt} + \alpha CfV(t) \qquad (12)$$

The resolution of (12) yield to the control voltage given by (13)

$$V(t) = \frac{V_{DD}}{1 + \alpha R_{on} Cf}\left[1 - \exp\left(-\frac{1 + \alpha R_{on} Cf}{R_{on} C}t\right)\right] \qquad (13)$$

The following charge current expression (14) is just deriving according to (10).

$$i_{ch}(t) = \frac{V_{DD}}{R_{on}}\exp\left(-\frac{1 + \alpha R_{on} Cf}{R_{on} C}t\right) \qquad (14)$$

Finally, the total supply current $i_{DD}(t)$ is obtained by (15) according to (11).

$$i_{DD}(t) = \frac{V_{DD}}{R_{on}}\left[1 - \frac{1}{1 + \alpha R_{on} Cf}\left(1 - \exp\left(-\frac{1 + \alpha R_{on} Cf}{R_{on} C}t\right)\right)\right] \qquad (15)$$

For a minimum loss of the power transfer to the load, the efficiency (which is the ratio of the load power to the total supply power) given by (16) must tend to one.

$$Efficiency = \frac{P_{load}}{P_{sup\ ply}} = \frac{i_{ch}V}{i_{DD}V_{DD}} \qquad (16)$$

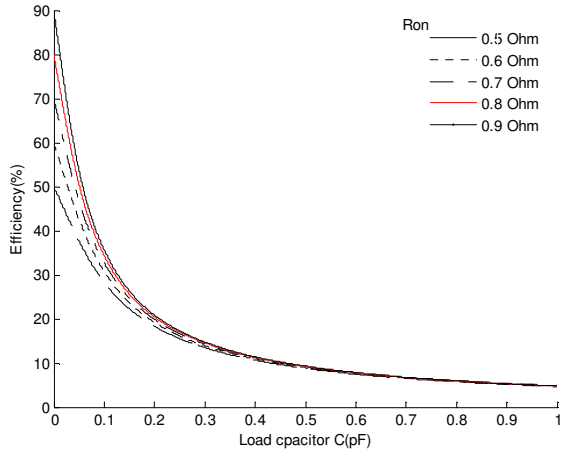
From (13), (14) and (15), we obtain

$$Efficiency = \frac{R_{on}b/a[1-\exp(-a)][1-1/a[1-\exp(-a)]]}{1+b/a[1-a-\exp(-a)]} \qquad (17)$$

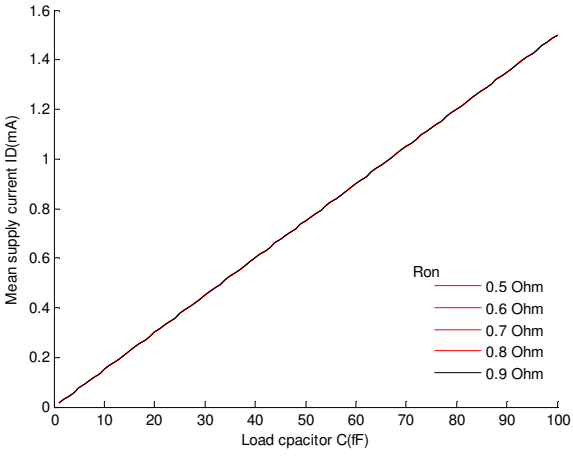
With a and b the defining constant below; χ/f is the circuit element response time.

$$a = \chi\frac{1+\alpha R_{on}Cf}{R_{on}Cf} \text{ and } b = \frac{1}{1+\alpha R_{on}Cf}$$

According to (17), for a chosen constant $\alpha\,(0 \le \alpha \le 1)$ and an expected response time χ/f , during the process we will derive the conduction resistance Ron and the corresponding load capacitance C whose leads to a better efficiency; the deduced average current in the following according to (15) will then be used in the optimum geometric parameter calculation. Therefore, for the optimum energy consumption during the design process, the circuit designs most progressively move from the load element estimation.



(a)



(b)

Figure 3: (a)-Power transfer efficiency variation with the input load circuit impedance (capacitor C) for various conduction resistance values;(b)- load current mean value variation with the load capacitor for various conduction resistance values; $f = 10MHz$; $V_{DD} = 1.5V$; $\alpha = 0.2$; $\chi = 0.001$.

We have in Fig.3-(a) above, the efficiency variation with the load circuit capacitor for the various conduction resistance values; in Fig.3-(b), a derived average supply current

variation with the load capacitor for the same various conduction resistance values.

B. *Application*

From the fig.3, for an example of circuit operating at a frequency of 10 MHz, for a response time element circuit of 0.1ns(i.e. $\chi = 0.001$) and $Ron = 0.9\Omega$, the load capacitor of 40 fF allows an efficiency of 60.8% for an expected average total supply current value of 0.6mA. According to Fig.2, this current estimation should be used to calculate the optimum geometric parameters of the circuit1 element of which the load must be an input impedance capacitor C of a circuit2 element.

v. Conclusion

We have presented in this paper the design method for the low energy consumption in an electronic system. Its interest is not any more to show, especially in embedded electronic devices where the need of design with the battery long lifespan is a major asset. This work can be adapted to any electronic system design process in order to carry out the estimation of the operating energy expenditure and then its optimization for a low final power consumption circuit.

Indeed, one of the challenges in an electronic circuit design is the preliminary estimation of the energy consumption. Essentially, the power expected should be involved along the design process in order to improve efficiency of embedded electronic devices which need a very low voltage battery.

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