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74V High Figure-of-Merit Lateral Trench Gate Power MOSFET on InGaAs

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***Abstract* — In this paper, a power lateral trench-gate metal oxide-semiconductor field-effect transistor (MOSFET) on InGaAs is proposed. The device consists of two gates placed vertically in separate trenches built in the drift region on both sides of P body region. Under ON-state, two channels are created in P-body which carry current simultaneously to enhance performance of the device. The trench structure of the proposed device causes reduced-surface-field effect in the drift region to improved breakdown voltage. The device design also provides a reduction in cell pitch and higher drift region doping to decrease the on-resistance. Two-dimensional numerical simulations are performed to analyze and compare the performance of proposed device with that of the conventional MOSFET. The proposed MOSFET structure gives 80% higher breakdown voltage, 17% lower specific on-resistance, 25% reduction in cell pitch and 3.8 times improvement in figure-of-merit over the conventional device.**

Keywords— **Power MOSFET, InGaAs, trench-gate, breakdown voltage, on-resistance, figure-of-merit.**

I. INTRODUCTION

Laterally diffused metal-oxide-semiconductor field-effect transistors (LDMOSFETs) with silicon channel are playing key role in smart power integrated circuits requiring operating voltages in the range 50-100V for applications such as computer, auto-mobile, aerospace and communication technologies [1], [2]. However, Si based power MOSFETs are reaching their performance limit due to inherent material properties. Therefore, there is a need to have a semiconductor material for power MOSFETs which can provide better device performance as compared to Si. In the recent past, InGaAs has been regarded as a promising semiconductor material for power MOSFETs due to its higher electron mobility leading to higher current density and lower on-resistance at high frequencies [3], [4]. In order to reduce the power dissipation in an LDMOSFET, its on-resistance should be as low as possible at a given operating voltage. In a conventional design of power LDMOSFET, there is a trade-off between breakdown voltage (V_{br}) and specific on-resistance ($R_{on\text{-}sp}$) [5] because both are related with each other. For example, one can reduce the on-resistance by increasing the drift region doping but this also decreases the breakdown voltage. One measure of this trade-off between breakdown voltage and on-resistance is figure-of-merit ($V_{br}^2/R_{on\text{-}sp}$), which should be as high as possible for better design of the device. Several modifications have been made in the conventional LDMOSFET to improve the figure-of-merit of the LDMOSFET [3], [5]–[7]. It has been successfully demonstrated that the trench-gate technology enhances the reduced-surface-field (RESURF) effect in the device and hence improves the reverse blocking voltage. This also allows higher drift region doping to achieve lower on-resistance. A dual trench-gate structure reported [3] on InGaAs has shown to provide appreciable improvements in the device performance when compared to the conventional structure for the same pitch length. In integrated circuits, reduction in cell pitch is also desirable in order to get higher packing densities and reduced cost of fabrication.

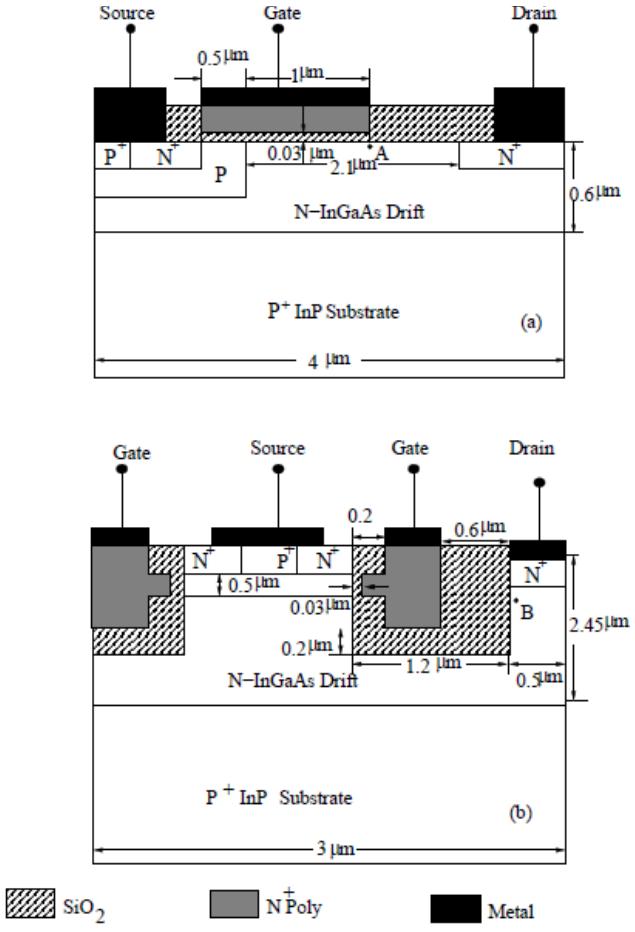

Fig. 1. Cross-sectional view of (a) conventional LDMOSFET and (b) proposed LDMOSFET

Therefore, motive of this work is to propose a power InGaAs channel power LDMOSFET structure which gives significant improvement in on-resistance, breakdown voltage, figure-of-merit and cell pitch as compared to the conventional device. The performance of proposed device along with conventional LDMOSFET is evaluated using two-dimensional simulation in device simulator, ATLAS [8].

II. Device Structure

The conventional power LDMOSFET on InGaAs is shown to have better performance over silicon counterpart as reported in [9]. The cross-sectional view of the conventional LDMOSFET and the proposed device is given in Fig. 1. Both the structures are having an n-type InGaAs drift region over the p-type InP substrate. N^+ polysilicon is used as gate material in both the devices. The conventional device has a gate length of 0.5µm with a field plate over the drift region to shift the peak electric field from the pn junction to end of the field plate and hence improving breakdown voltage. However, the electric field still peaks on the InGaAs surface. In the conventional device, the cell pitch is taken as 4µm which is optimized to get maximum breakdown voltage at a drift region doping of 2×10^{16} cm^{-3}. Other structural parameters used in simulations are also shown in Fig. 1(a). When a positive gate voltage greater than the threshold voltage is applied at the gate electrode, a channel is created under the gate in P-body region resulting current flow from drain to source for positive drain voltages. In case of proposed device, source contact is taken on the top of P-body region and drain contact is placed at left side top of the drift region as shown in Fig. 1(b). On both sides of the P-body region, two gates are placed vertically in the trenches. When a positive gate voltage is applied at both the gates, two parallel channels are created in the P body region and current flows from drain to source in the bulk of drift region. It may be noted that keeping the gate length same as that of conventional device, the cell pitch of proposed device is 3µm even at a higher drift region doping of 4×10^{16} cm^{-3}. This gives a reduction of 25% in cell pitch of the proposed device as compared to conventional device. The parallel conduction of two channels, increased drift region doping and reduced cell pitch leads to lower on-resistance of the proposed structure. Further, the trench structure enhances the RESURF effect in the drift region i.e. peak electric field in the proposed device decreases which results higher breakdown voltage. The other dimensions of proposed structure are given in Fig. 1(b) which also affect the breakdown voltage of the device.

III. Simulation Results

The structures of conventional and proposed devices as discussed in previous section were implemented in the device simulator (ATLAS). Two-dimensional numerical simulations were performed by choosing suitable models for Shockley Read-Hall, concentration-dependent mobility, electric-field dependent mobility, and impact ionization. The simulated breakdown and on-resistance characteristics of both devices are obtained and compared with each other as discussed below.

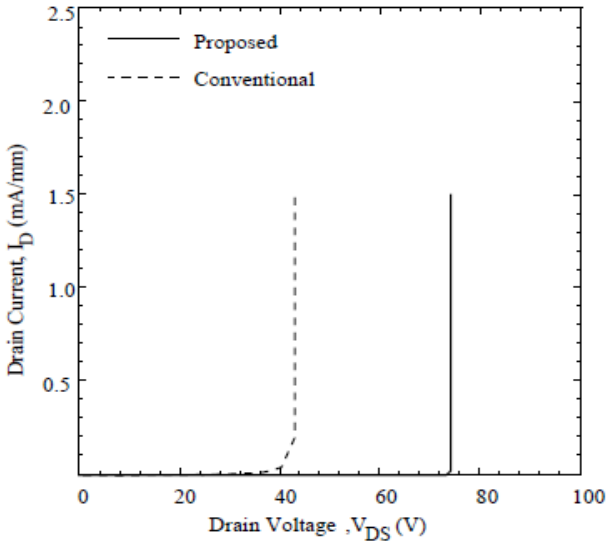

Fig. 2. Off-state breakdown characteristics of the proposed and conventional LDMOSFETs.

A. Breakdown Voltage

Fig. 2 shows the simulated breakdown characteristics of proposed device as compared with that of conventional LDMOSFET under off-state when gate voltage is not applied. As drain to source voltage is increased, the electric field inside the drift region increases and when it becomes equal to the critical electric field of InGaAs, the breakdown of the device occurs. In case of conventional structure, the peak electric field occurs at the end of field plate causing breakdown of device at this point. The simulated breakdown voltage of conventional LDMOSFET is found to be 41V at a drift region doping of 2×10^{16} cm^{-3}. On the other hand, the breakdown voltage of proposed device is obtained as 74V even at a higher drift region doping of $4\times10^{16}cm^{-3}$. This shows an improvement of 80% in breakdown voltage of the proposed device over the conventional one. The reason for large improvement in breakdown voltage is reduction in peak electric field in the drift region of proposed structure due to RESURF effect caused by the trench structure.

Fig. 3 shows two dimensional distribution of electric field in the drift region of conventional and proposed devices at drain to source voltage (V_{DS}) of 25V. It can be seen that for conventional device, the peak electric field occurs at InGaAs surface in the drift region at the end of gate field-plate (point 'A'). Whereas in case of proposed device, a reduced electric field is shifted to the bulk of InGaAs (point 'B'). This indicates that the electric field in the conventional device is higher as compared to proposed LDMOSFET and hence breakdown of conventional structure will occur at lower voltage than that of proposed device. Fig. 4 shows two-dimensional electric contours at off-state breakdown characteristics of the proposed and conventional LDMOSFETs. It is found that the peak electric field at breakdown is same in both the devices.

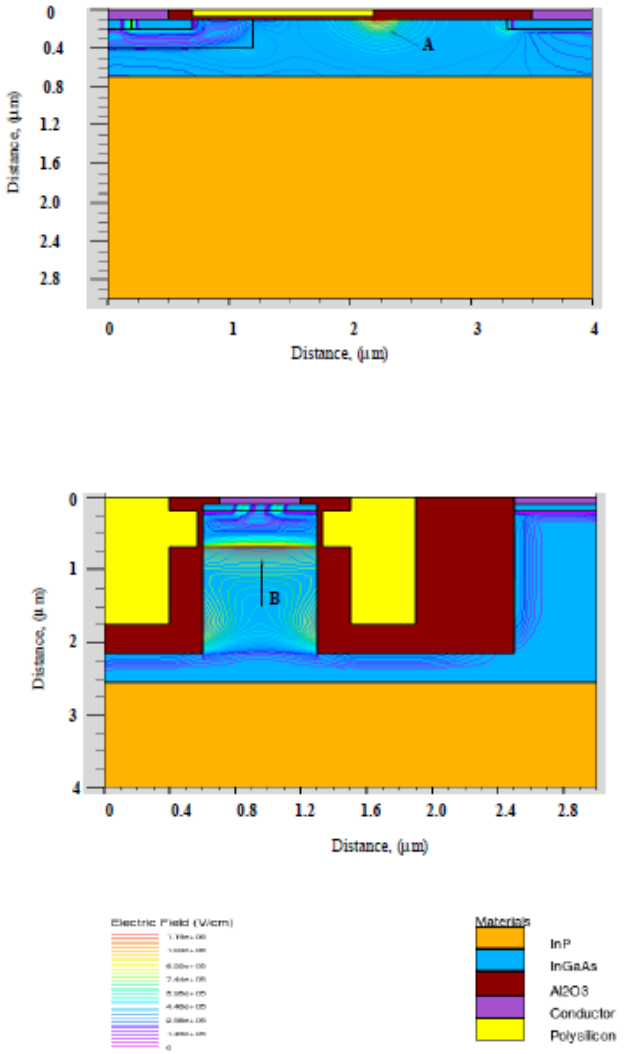

Fig. 3. Two-dimensional electric field contours in the drift region at V_{DS}=25V of conventional and proposed LDMOSFETs.

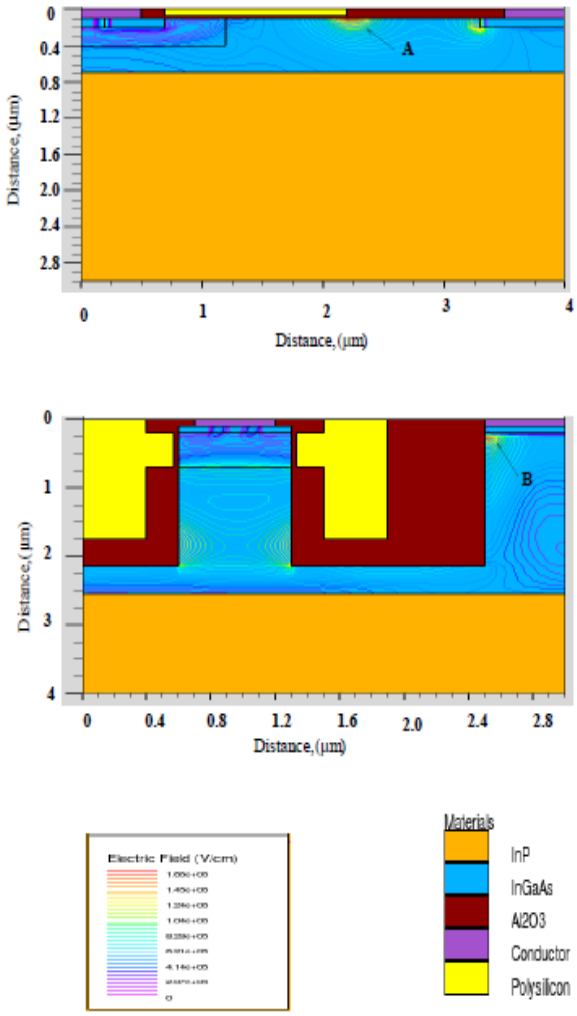

Fig. 4. Two-dimensional electric field contours in the drift region at breakdown of conventional and proposed LDMOSFETs.

B. ON-Resistance

The power dissipation of the power LDMOSFET under on-state condition is determined by the on-resistance of the device. The on-resistance of the device is a series combination of drift region resistance, channel resistance and contact resistances of drain and source. The total on-resistance of a power LDMOSFET can be obtained as ratio of drain voltage to drain current when device is biased in the linear region for low drain voltages and high gate bias so that the channel is completely formed. The simulated drain characteristics of the conventional and proposed device in the linear region at gate bias of 10V are shown in Fig. 5. The specific on-resistance of the conventional and proposed LDMOSFETs is found to be 44 and 53 $m\Omega.mm^2$, respectively. In other words, specific on-resistance of the proposed structure is 17% lower than that of conventional device. This reduction in specific on-resistance is due to reduced cell pitch, higher drift region doping, and presence of two conducting channels in the proposed device.

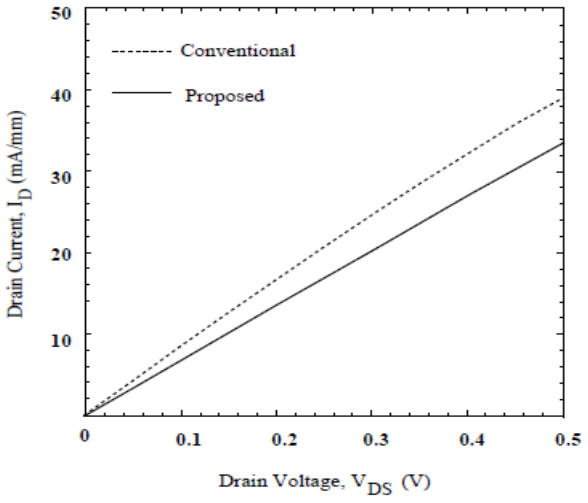

Fig. 5. Drain characteristics of the conventional and proposed LDMOSFETs in linear region.

C. Figure-of-Merit

In the previous sections, it is seen that the proposed LDMOSFET design exhibits higher breakdown voltage and lower specific on-resistance when compared to conventional device. This indicates that the trade-off between breakdown voltage and specific on-resistance has been improved. One measure of this trade-off is figure-of-merit (FOM= V_{br}^2/R_{on-sp}). Using simulation results, the figure-of-merit of conventional and proposed devices is calculated as 3.17 and 12.44 MW/cm^2 respectively. This provides an improvement of 3.92 times in figure-of-merit of proposed device compared to conventional device.

IV. CONCLUSION

A new power LDMOSFET structure on InGaAs is presented. The proposed device is having a dual trench-gate structure to enhance the current conduction from drain to source. Presence of two parallel channels, higher drift region doping and reduced cell pitch results in lower on-resistance of proposed device. Further, large improvement in breakdown voltage has been achieved by reduction in peak electric field inside the drift region of the proposed device due to trench structure. Two dimensional simulations are used to investigate and analyze the performance of proposed trench-gate structure and compare the results with that of the conventional LDMOSFET. Based on simulation results, it demonstrated that the proposed device exhibits 80% higher breakdown voltage and 17% reduction in on-resistance leading to 3.92 times improvement in figure-of-merit as compared to the conventional device. The proposed trench-gate power LDMOSFET also gives 25% reduction in cell pitch resulting higher packaging density and reduced cost of fabrication.

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