

Minimization of Total Harmonic Distortion in multilevel inverter output using artificial neural network based controller

Abhishek Soni (Student, Manipal University Jaipur), Manish Thukral (Asso. Professor, Manipal University Jaipur)

Abstract— This Paper aims to extend the knowledge about the performance of different cascaded multilevel inverter through harmonic analysis. Large electric drives and utility require advanced power electronics converter to meet high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings but also improves the performance of the whole system in terms of harmonics, dv/dt stresses and stresses in the bearing of the motor. Despite of various advantages seen in multilevel inverter the total harmonic distortion has always been a matter of concern. In the presented work a neural network based model is proposed for reducing the total harmonics distortion from multilevel inverter output. For this neural network is trained to perform selective harmonic elimination. The training data is obtained by solving non-linear equation obtained from selective harmonics analysis using genetic algorithm technique. The trained neural network based controller is shown to decide the notches angle for given modulation index. The proposed model is simulated on MALAB Simulink platform. Experimental results are obtained for different modulation index and the performance of the multilevel inverter. The results are further analyzed in terms of total harmonic distortion (THD). (*Abstract*)

Keywords— Genetic Algorithm (GA), Multilevel Inverter, Selective harmonics elimination PWM (SHEPWM), Neural Network. (*key words*)

I. Introduction

Today, Multilevel Inverters are used in applications such as flexible AC transmission system (FACTS) equipment [1], high voltage current lines [2], and electrical drives [3]. There are three types of multilevel inverters are used: diode clamped [4], flying capacitor [5], and cascaded H-bridge multilevel inverter with separate dc sources [6]. Referring to the literature reviews, the cascaded multilevel inverter (CMI) with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications due to their modularization and extensibility. For improving the efficiency at inverter level itself, so many techniques have been developed. They are categorized on the basis of high and low switching frequency. First of them is using various switching strategies, such as sinusoidal pulse width modulation (SPWM), Space vector pulse width modulation (SVPWM), Selective harmonics elimination PWM (SHEPWM), Optimized harmonic stepped waveform (OHSW) [7], [8]. The second method is using a low pass filter in the output of inverters to eliminate higher order harmonics. Final approach is to use multilevel topologies in order to reduce harmonics and Total harmonic distortion (THD). SHEPWM strategy has also been introduced in MI. In this method the aim is to eliminate the lower order harmonics, while the

fundamental component is satisfied. In this approach by solving the n number of equations, $(n-1)$ lower order harmonics from the fifth order can be eliminated and the fundamental component gets satisfied. Solving the non-linear equations major issue is, obtaining the switching angles.

So far several methods has been suggested to calculate the switching angles, which can be categorized in two sets. The first group is based on satisfying the equations called conventional optimization methods. Such as Newton-Raphson (NR) method and Gauss-Seidal method are two of these [10]. They also termed by iterative methods. The disadvantage of these methods is they are very much dependent on the initial guess and divergence problems are likely to occur for the large number of inverter levels. Which can say that they may struck in local minima and global minima is not guaranteed in iterative method. Also those methods may does not give the solutions for infeasible modulation index that exists. In addition using fsolve all roots can be found base on gauss- newton method [11].

Since the first group dos not provided any optimal solutions for infeasible m, the second group of methods have been introduced based on evolutionary optimization techniques. These methods not only find the solutions for infeasible M, where lower order harmonics can be completely removed but also give the global minima too for the optimal output. Evolutionary methods provides the optimum angles and can be used for any number of inverter levels. They are free from derivation. GA is one of the methods that have been used in this paper [14], [15]. In addition Particle swarm optimization (PSO) method [16], Ant colony optimization [17] and Bee Algorithm [18] have been introduced.

In this paper GA is applied to minimize the lower order harmonics and satisfying the fundamental component. Result introduced the probability of reaching the global minima has been compared without using the GA. Experimental results are presented to confirm the simulation results.

This paper is divided into following parts: Introduction, Multilevel Inverter, Selective harmonics Elimination, Proposed Scheme and, Experimental Results.

II. Multilevel Inverter

A. Cascaded H-Bridge Multilevel topology

A cascaded multilevel inverter is a combination of series connected single phase full bridge inverters. Each full bridge generates its own individual voltage and its level is -

V_{dc} , 0, $+V_{dc}$. Total output voltage is the sum of all the individual voltage. However all the inverters can produce staircase output voltage waveform. The number of output voltage levels can be decided by $2*N+1$, where N is the number of the dc sources. For example, phase voltage waveform for eleven level cascaded multilevel inverter with five separate dc sources is shown in figure 2. A firing angle scheme is prepared with respect to neural network to get the corresponding angle in the proposed scheme. A multilevel inverter is shown in figure with sine angle control instead of pulse generator in figure 1. In sine angle control, a sine wave is taken as a reference signal and firing angles are provided to create a dc signal of the desired value by taking the desired magnitude of dc signal so that we can get the necessary notches angles.

A cascaded multilevel inverter has advantages that have been presented in [18]. Each H-bridge inverter unit generates a quasi-square waveform by phase shifting the switching timings of positive and negative phase leg.

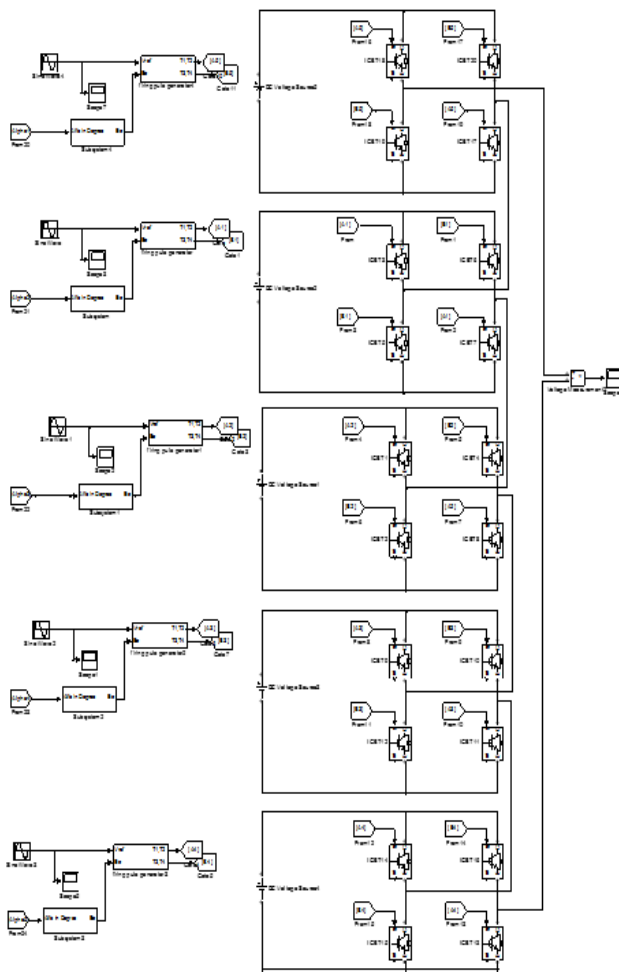


Figure 1. Eleven level inverter with five separate dc sources

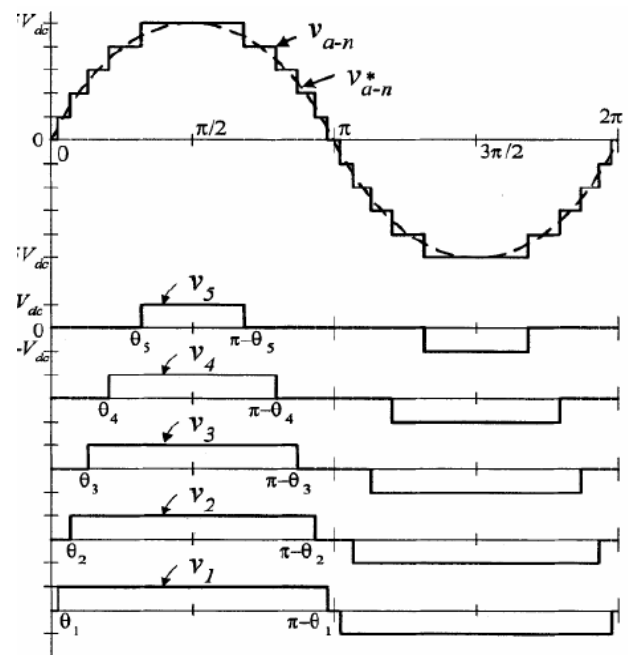


Figure 2 output voltage waveform of cascaded 11 level inverter

Abhishek Soni (Author)
 Manipal University, Jaipur
 India
 Abhishek.soni.abhi@gmail.com

Manish Thukral (guide)
 Manipal University, Jaipur
 India

III. Selective Harmonic Elimination

A 11-level inverter waveform shown in Figure 2 has five variables $\alpha_1, \alpha_2, \alpha_3, \alpha_4$ and α_5 , where $V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}$ and V_{dc5} are assumed to be equal. By taking equal amplitude of all dc sources, The Fourier series for a periodic function $v_0(\omega t)$ can be expressed as:

$$v_0(\omega t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t) \quad (1)$$

For an odd quarter-wave symmetry waveform, $a_0 = 0, a_n = 0$ and

$$b_n = \begin{cases} \frac{4}{\pi} \int_0^{\pi/2} v_0 \sin(n\omega t) d(\omega t) & \text{for odd } n \\ 0 & \text{for even } n \end{cases} \quad (2)$$

The Fourier series expansion of the output voltage for a notched waveform, will be written as

$$b_n = \frac{4}{\pi} \int_0^{\pi/2} v_0 \sin(n\omega t) d(\omega t) \quad (3)$$

$$b_n = \frac{4}{\pi} \left[\int_{\alpha_1}^{\alpha_2} v_0 \sin(n\omega t) d(\omega t) + \int_{\alpha_3}^{\pi/2} v_0 \sin(n\omega t) d(\omega t) \right] \quad (4)$$

$$b_n = \frac{4V_{dc}}{\pi} \left\{ [-\cos n(\omega t)]_{\alpha_1}^{\alpha_2} + [-\cos n(\omega t)]_{\frac{\pi}{2}}^{\alpha_3} \right\} \quad (5)$$

$$bn = \frac{4V_{dc}}{n\pi} \left\{ [-\cos n(n\omega t)]_{\alpha_1}^{\alpha_2} + [-\cos n(n\omega t)]_{\alpha_3}^{\frac{\pi}{2}} \right\} \quad (6)$$

$$bn = \frac{4V_{dc}}{n\pi} \cos n(n\omega t) \left| \begin{matrix} \alpha_1, \alpha_3 \\ \alpha_2, \frac{\pi}{2} \end{matrix} \right. \quad (7)$$

$$bn = \frac{4V_{dc}}{n\pi} \left[\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3) - \cos\left(n\frac{\pi}{2}\right) \right] \quad (8)$$

$$bn = \frac{4V_{dc}}{n\pi} \left[\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3) \right] \quad (9)$$

Switching angles has the constraints between 0 to 90 $\{0 \leq \alpha_i < 90\}$, because of quarter half wave symmetry characteristics, Even harmonics becomes zero and the triplen harmonics are also absent since they will not show their effect in 3-phase balanced systems. The general expression for an output equations will equals to:

$$-\sum_{k=1}^N (-1)^k \cos(n\alpha_k) = M, \text{ for fundamental } (n=1)$$

$$-\sum_{k=1}^N (-1)^k \cos(n\alpha_k) = 0, \text{ for } n = 3, 5, \dots, 2N - 1 \quad (10)$$

Which can be shown as:

$$\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) - \cos(1\alpha_4) + \cos(1\alpha_5) = 5M \quad (11)$$

$$\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) + \cos(5\alpha_5) = 0 \quad (12)$$

$$\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) - \cos(7\alpha_4) + \cos(7\alpha_5) = 0 \quad (13)$$

$$\cos(11\alpha_1) - \cos(11\alpha_2) + \cos(11\alpha_3) - \cos(11\alpha_4) + \cos(11\alpha_5) = 0 \quad (14)$$

$$\cos(13\alpha_1) - \cos(13\alpha_2) + \cos(13\alpha_3) - \cos(13\alpha_4) + \cos(13\alpha_5) = 0 \quad (15)$$

Where M is the Modulation Index, the relation between the fundamental voltage and maximum voltage is given by modulation Index. It is given by m1, is the ratio of fundamental voltage v1 to the maximum voltage. The maximum voltage is given by:

$$V_{1max} = \frac{4}{\pi} s V_{dc} \quad (16)$$

$$m = \frac{\pi v_1}{4s V_{dc}} \quad (17)$$

Now the major concern is to solve those equations to find the notches angles by considering the selected modulation index M.

IV. Genetic Algorithm

Genetic Algorithms are search and optimization techniques based on Darwin's Principle of Natural Selection. Basically this algorithm is a set of instructions that is repeated to solve a problem. Conceptually follows steps inspired by the biological processes of evolution

(gradual working or development). And better solutions evolve from previous generations until a near optimal solution is obtained. Basic principle of GA is "Select the best Discard the Rest".

5 Phases of Genetic Algorithm are:

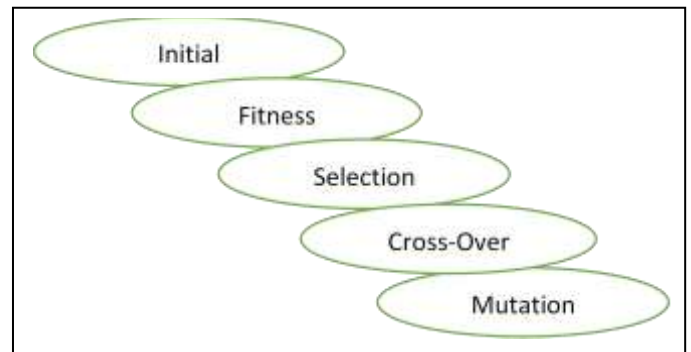


Fig. 3 Basic flowchart of GA

Initial Population Begins with randomly generated states. Fitness Function Produces the next generation of States. Good Function returns better states which depends on initial population. Fitness function gives a score or a value to each state. The probability of being chosen for a reproduction is based on fitness value. In Selection Two Pairs are Select at random. Select based on their fitness value. One may be select more than once or not to be select at all. For crossover, each pair to be mated, a Crossover point is chosen at random from within. Offspring's are created by exchanges between the Parents and the Crossover point.

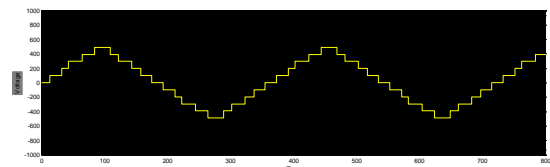


Figure 4. Output waveform of 11- level inverter by using Multi Objective Genetic Algorithm

v. Proposed Scheme

Most people would consider the back propagation network to be quintessential neural network. Back propagation is the training or learning algorithm rather than the network itself. In this paper after solving the SHE non-linear transcendental equations using Genetic Algorithm, an expert controller has created which is trained using the neural network. Since the neural network has trained, gives the best angles for the entire modulation index. The network first initialized by setting up all its weights to be small random numbers say between -1 to +1. Next, input pattern is applied and output calculated called forward pass. The calculation gives an output which is completely different from the target, since all weights are random. We then calculate the error of each neuron which is essentially: Target – Actual output. This error is used mathematically to change the weights in such a way that the error will be smaller, this is called reverse pass. 2 inputs, 3 hidden layer

neurons and 2 output neurons as shown in figure 5. W^+ represents the new, recalculated, weight, whereas W (without the superscript) represents the old weight.

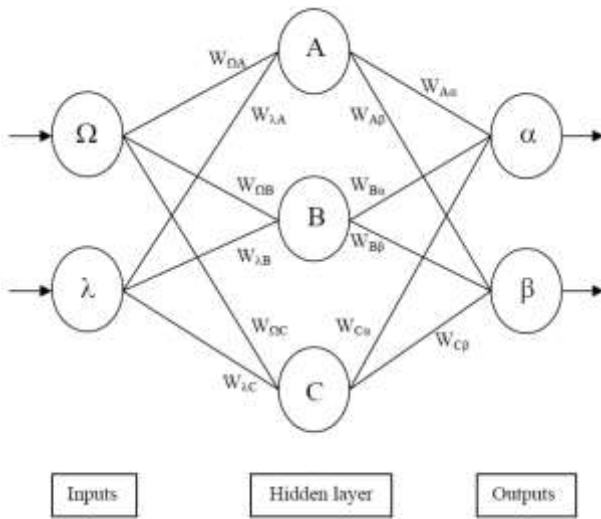


Figure 5. Overview of a neural network

1. Calculate errors of output neurons

$$\delta\alpha = out_\alpha (1 - out_\alpha) (Target_\alpha - out_\alpha)$$

$$\delta\beta = out_\beta (1 - out_\beta) (Target_\beta - out_\beta)$$

2. Change output layer weights

$$W^+_{A\alpha} = W_{A\alpha} + \eta\delta\alpha out_A \quad W^+_{A\beta} = W_{A\beta} + \eta\delta\beta out_A$$

$$W^+_{B\alpha} = W_{B\alpha} + \eta\delta\alpha out_B \quad W^+_{B\beta} = W_{B\beta} + \eta\delta\beta out_B$$

$$W^+_{C\alpha} = W_{C\alpha} + \eta\delta\alpha out_C \quad W^+_{C\beta} = W_{C\beta} + \eta\delta\beta out_C$$

3. Calculate (back-propagate) hidden layer errors

$$\delta_A = out_A (1 - out_A) (\delta\alpha W_{A\alpha} + \delta\beta W_{A\beta})$$

$$\delta_B = out_B (1 - out_B) (\delta\alpha W_{B\alpha} + \delta\beta W_{B\beta})$$

$$\delta_C = out_C (1 - out_C) (\delta\alpha W_{C\alpha} + \delta\beta W_{C\beta})$$

4. Change hidden layer weights

$$W^+_{\lambda A} = W_{\lambda A} + \eta\delta A in_\lambda \quad W^+_{\Omega A} = W_{\Omega A} + \eta\delta A in_\Omega$$

$$W^+_{\lambda B} = W_{\lambda B} + \eta\delta B in_\lambda \quad W^+_{\Omega B} = W_{\Omega B} + \eta\delta B in_\Omega$$

$$W^+_{\lambda C} = W_{\lambda C} + \eta\delta C in_\lambda \quad W^+_{\Omega C} = W_{\Omega C} + \eta\delta C in_\Omega$$

The constant η (called the learning rate, and nominally equal to one) is put in to speed up or slow down the learning if required.

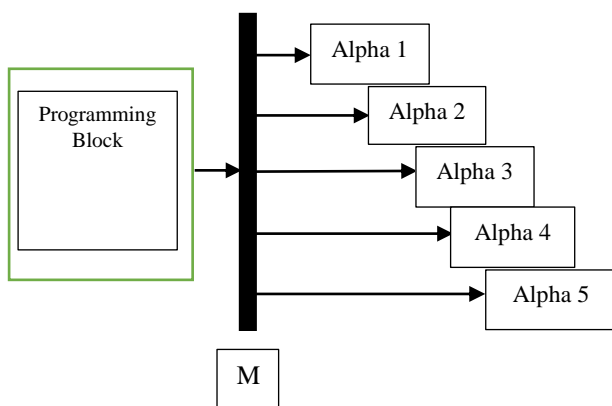


Figure 6. Controller block for generating the firing angles

An Embedded block is created to program and train the neural network controller, and its output is fed to all the individual inverter's firing scheme at particular angle. Neural network controller is shown in figure 6.

VI. Experimental Results

For Optimization, the function has to be created which will be the objective function. For the Modulation Index $M=1$, nonlinear equations is solved and compared its FFT with the generalized output of Multilevel Inverter (fig 7, 8).

Table 1. Data collection of firing angles with respect to modulation Index

MI	CPU Time	α_1	α_2	α_3	α_4	α_5
0.1	1.88	18.47	28.77	39.08	53.46	59.67
0.2	1.77	21.10	32.23	44.33	58.11	73.27
0.3	1.27	26.79	47.08	61.54	74.05	74.38
0.4	2.88	25.78	43.43	50.58	64.60	72.56
0.5	3.36	22.08	38.44	54.53	63.08	83.08
0.6	2.70	8.94	29.30	36.18	55.46	65.50
0.7	1.37	9.38	9.95	25.93	36.13	86.39
0.8	1.03	13.46	20.12	34.66	54.96	67.30
0.9	2.07	11.38	17.34	38.06	48.29	78.17
1	1.01	12.88	31.82	42.37	64.33	84.19

Table 1. Firing angle with for $M=1$, executed for multilevel inverter

M	α_1	α_2	α_3	α_4	α_5
1	12.88	31.82	42.37	64.33	84.19

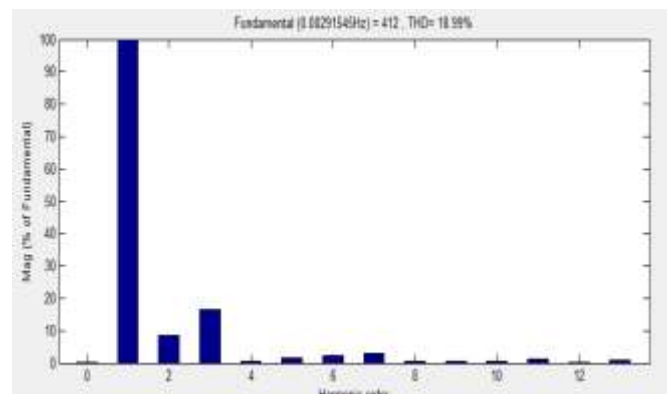


Figure 7. FFT Analysis of 11 level Inverter without using GA

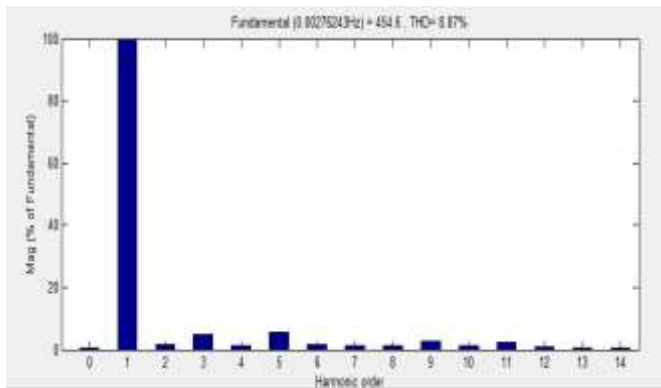


Figure 8. FFT Analysis of 11 level Inverter with using GA

References

- [1] Q. Song and W. Liu, "Control of a cascade STATCOM with star configuration under unbalanced conditions," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 45–58, Jan. 2009.
- [2] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.
- [3] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
- [4] N. Hatti, K. Hasegawa, and H. Akagi, "A 6.6-kV transformerless motor drive using a five-level diode-clamped PWM inverter for energy savings of pumps and blowers," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 796–803, Mar. 2009.
- [5] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multilevel converter based on modified phase-shifted pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1517–1526, Jun. 2010.
- [6] A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 51–65, Jan. 2011.
- [7] A. Kaviani, S. H. Fathi, N. Farokhnia, and A. Ardakani, "PSO, an effective tool for harmonics elimination and optimization in multilevel inverters," in *Proc. 4th IEEE Conf. Ind. Electron. Appl.*, May 25–27, 2009, pp. 2902–2907.
- [8] W. Fei, X. Ruan, and B. Wu, "A generalized formulation of quarter-wave symmetry SHE-PWM problems for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1758–1766, Jul. 2009.
- [9] M. T. Hagh, H. Taghizadeh, and K. Razi, "Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2259–2267, Oct. 2009.
- [10] W. Fei, X. Du, and B. Wu, "A generalized half-wave symmetry SHE-PWM formulation for multilevel voltage inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3030–3038, Sep. 2010.
- [11] T. Tang, J. Han, and X. Tan, "Selective harmonic elimination for a cascade multilevel inverter," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 2006, vol. 2, pp. 977–981.
- [12] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 459–469, Mar. 2006.
- [13] M. G. Hosseini-Aghdam, S. H. Fathi, and G. B. Gharehpetian, "Elimination of harmonics in a multilevel inverter with unequal DC sources using the homotopy algorithm," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 4–7, 2007, pp. 578–583.
- [14] R. Salehi, N. Farokhnia, M. Abedi, and S. H. Fathi, "Elimination of low order harmonics in multilevel inverter using genetic algorithm," *J. Power Electron.*, vol. 11, no. 2, pp. 132–139, Mar. 2011.
- [15] M. S. A. Dahidah and V. G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1620–1630, Jul. 2008.
- [16] R. Salehi, B. Vahidi, N. Farokhnia, and M. Abedi, "Harmonic elimination and optimization of stepped voltage of multilevel inverter by bacterial foraging algorithm," *J. Electr. Eng. Technol.*, vol. 5, no. 4, pp. 545–551, 2010.
- [17] K. Sundareswaran, K. Jayant, and T. N. Shanavas, "Inverter harmonic elimination through a colony of continuously exploring ants," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2558–2565, Oct. 2007.
- [18] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
- [19] D. T. Pham, S. Otari, A. Adidy, M. Mahmuddin, and H. Al-Jabbouli, "Data clustering using the bees algorithm," in *Proc. 40th College Int. pour la Recherche en Productique Int. Manuf. Syst. Semin.*, 2007.
- [20] L. Ozbakir, A. Baykasoglu, and P. Tapkan, "Bees algorithm for generalized assignment problem," *Appl. Math. Comput.*, vol. 215, pp. 3782–3795, 2010.
- [21] N. Farokhnia, H. Vadizadeh, S. H. Fathi, and F. Anvariasl, "Calculating the formula of line voltage THD in multilevel inverter with unequal DC sources," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3359–3372, Aug. 2011.

About Author (s):



Abhishek Soni completed his B.Tech in Electrical Engineering from Arya Institute of Engineering and Technology, Jaipur. Currently he is pursuing M.Tech in Power Electronics and System from Manipal University Jaipur, Jaipur. His area of interest is Industrial drives and applications to Power electronics and attains in depth skills in programing and simulations.