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# A New Technique For Designing Low Power 2-Bit Magnitude Comparator

[Vijaya Shekhawat, *Tripti Sharma and K. G. Sharma]

***Abstract*— In this paper a new logic technique and hence circuit design has been proposed for the implementation of magnitude comparator. This proposed 2-Bit magnitude comparator is design to improve power consumption as well as on-chip area than its peer design. The proposed 2-Bit magnitude comparator has threshold loss of 13%-20%. This threshold loss is due to PTL (Pass Transistor Logic) logic applied at the input end and at the output end TG (Transmission Gate) logic is used, this is done to reduce the number of transistor. The schematic of 2-Bit magnitude comparator is designed using Tanner EDA Tool version 12.6 at 45nm technology.**

***Keywords*— Magnitude Comparator, TG logic, Proposed Technique and Low Power**

## I. Introduction

Binary magnitude comparator is a fundamental component in digital system with many applications such as the decoding of the x86 instruction set, communication systems, encryption devices and the number magnitude comparison in arithmetic logic unit. A high-performance comparator using All-N-Transistor (ANT) dynamic CMOS logic was proposed by Wang [1]. The heavy pipelining was required by ANT logic which made this design unsuitable for single-cycle operation. A design based on single-cycle, relies on priority encoder [2], has shown 16% performance enhancement over [1]. The different method based on priority encoding algorithm such as; parallel-MSB-checking algorithm and MUX based comparator structure where proposed in [3] and [4].This implementation has shown the better performance in terms of delay, at the expense of both power dissipation and number of transistor in comparison to previous work. All the above mentioned works give high performance with help of dynamic logic. But the activity factor dynamic logic is greater than static logic style, which lead to the higher power consumption of dynamic logic. So, the research work tends toward static logic style with low power consumption. In this work, TG logic style because it result compact circuit structures which may even require a smaller number of transistor than their standard CMOS [5].

This paper is organized into five sections. Section I briefs about the previous work and Section II discuss the magnitude comparator using TG logic style with the help of conventional method. Section III shows the feasibility of proposed technique for comparator. Section IV presents the performance analysis of proposed as well as existing TG comparator. Section V concludes the paper with result.

Vijaya Shekhawat, *Tripti Sharma and K. G. Sharma
ECE Department, FET-Mody Institute of Science & Technology
Lakshmangarh, Distt.- Sikar, Rajasthan, INDIA

## II. Prior Work

The traditional method to determine whether A is less than B (F2), A is greater than B (F3) and A is equal to B (F2), firstly check the most significant bit (A and B are two bit binary number input). If most significant bit of both inputs is different, e.g. suppose most significant of A is 1 and most significant bit of B is 0 then A>B and if input condition is reverse then A<B. If most significant bit of both the input is equal then go for next bit and then compare the next bit of both the input. If both the input is same then A=B.

The outcome of 2-Bit magnitude comparator is shown in Table I for different combination of input. The equations are as follow:

$$A > B := A1\,\overline{B1} + A0\,\overline{B0}(\overline{A1}\,\overline{B1} + A1B1) := A1\,\overline{B1} + A0\,\overline{B0}(X1) \quad (1)$$

$$A = B := (\overline{A1}\,\overline{B1} + A1\,B1)(\overline{A0}\,\overline{B0} + A0B0) := X1\,X0 \quad (2)$$

$$A < B := \overline{A1}B1 + \overline{A0}B0(\overline{A1}\,\overline{B1} + A1B1) := \overline{A1}B1 + \overline{A0}B0(X1) \quad (3)$$

Using this equation 2-Bit magnitude comparator is constructed using TG logic style is shown Fig. 1[6].

TABLE I. TRUTH TABLE OF 2-BIT MAGNITUDE COMPARATOR

| A1 | A0 | B1 | B0 | F2 | F1 | F3 |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 |

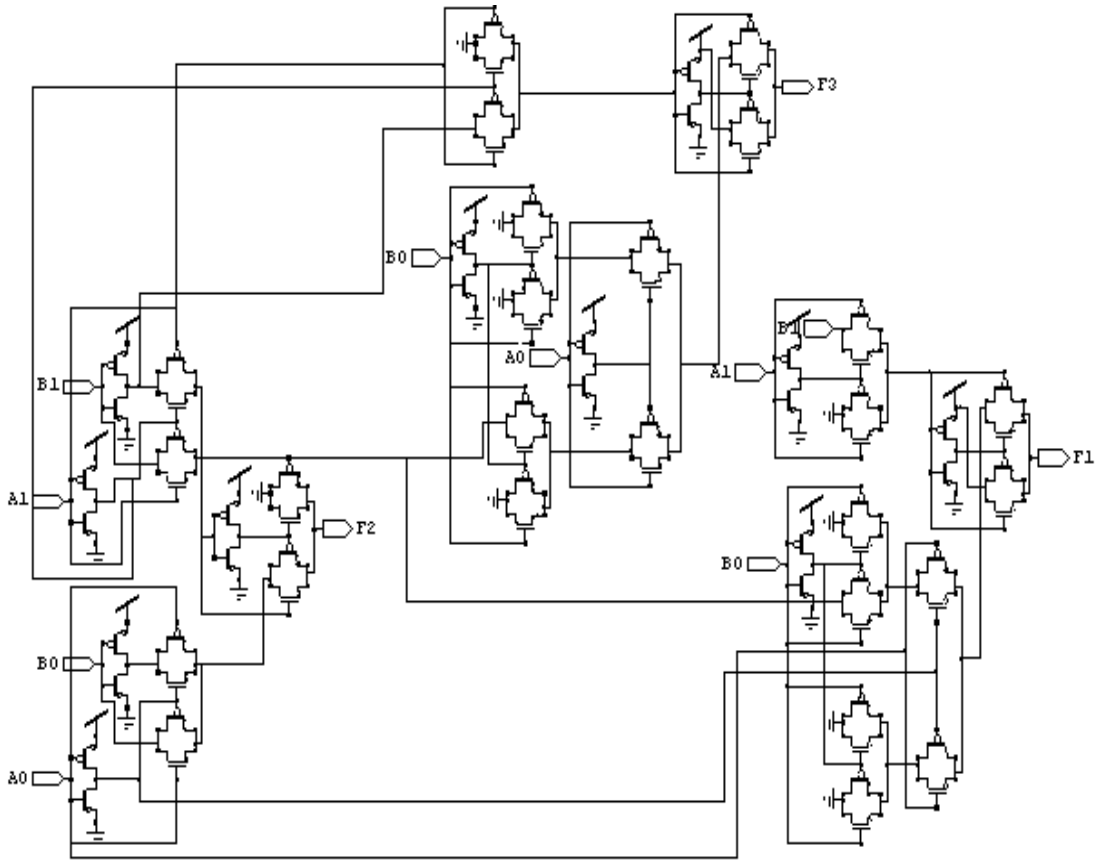


Figure 1. Schematic of 2 Bit Magnitude Comparator using existing technique

By seeing Fig.1, it reveals that 2-Bit Magnitude Comparator requires large no. of transistors i.e.; 76. Large transistor count consume more power and larger area, so to overcome this problem proposed technique has been used to construct magnitude comparator.

## III. Proposed Work

The proposed technique discuss below has introduce to achieve remarkable reduction in power consumption of comparator circuit. In this proposed technique two different tables are used for finding F1 and F2 output condition. For F1 (A<B) and F2 (A=B) we have use two different tables in such way that simpler output expression is derived. For F3 (A>B), NOR gate is used in between F1 and F2.

- If A1=A0=0, then F1=B1+B0
- If A1=0 and A0=1, then F1=B1
- If A1=1 and A0=0, then F1=B1.B0
- If A1=A0=1, then F1=0

The above conditions for F1 (A<B) are derived from Table II. The above condition reveals that it requires 2 gates (1 OR gate and 1 AND gate) at the output end. From this it can be conclude that proposed technique require less number of transistors.

TABLE II. TRUTH TABLE FOR F1

| A1 | A0 | B1 | B0 | F1(A<B) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

TABLE III. TRUTH TABLE FOR F2

| A0 | B0 | A1 | B1 | F2(A=B) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Now looking to Table.III for F2 (A=B)

If A0= B0 then F2=A1 ⊙ B1

If (A0=0 and B0=1) or (A0=1 and B0=0), then F2=0

As well as F3= $\overline{F1 + F2}$

The above condition reveals that for F2 it requires 2 XNOR gate at the output end. For F3 NOR gate is require at the output end. Using this technique 2-Bit magnitude comparator schematic is constructed with the help of TG logic style shown in Fig.2.

The proposed magnitude comparator has reduced transistor count i.e.; 46 in comparison to existing magnitude comparator i.e.; 76. The proposed TG based magnitude comparator shows the threshold loss ranging from 13%-20%, the reason behind this is that for passing the inputs at the first stage of the circuit, pass transistors are used. This is done in-order to reduce the on-chip area covered.

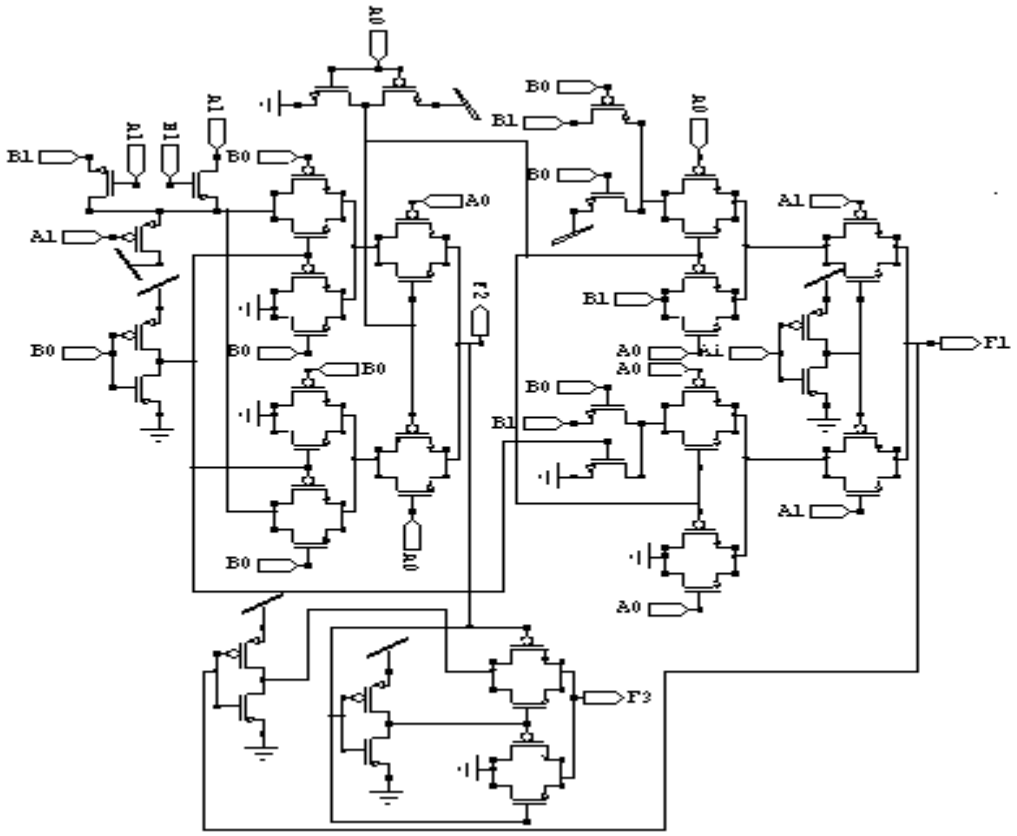


Figure 2. Schematic of 2-Bit Magnitude Comparator using proposed technique

# IV. Simulation Result

In order to prove that proposed design is consuming low power and have high performance, simulation are carried out for power consumption at varying input voltages, temperature and operating frequencies. The graphs shown in Fig.3-Fig.5 depict that the proposed TG magnitude comparator is the viable option for efficient design. The performance analysis with respect to temperature and frequency is done at 0.8V Input Voltage.

The graph shown in Fig.3 reveals that the power consumption of proposed TG magnitude comparator is remarkably reduced (56.3% to 60%) than the existing TG magnitude comparator. Also Fig.4 shows that power consumption of proposed circuit is constant on vary temperature at different range on increasing temperature the difference of power consumption increase which shows that power consumption of proposed consume low in comparison to existing comparator.

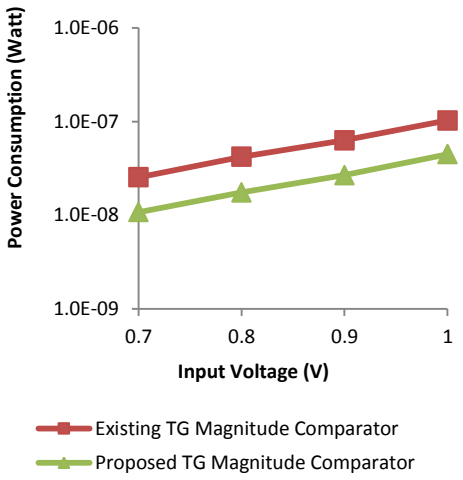


Figure 3. Power consumption at varying input voltage

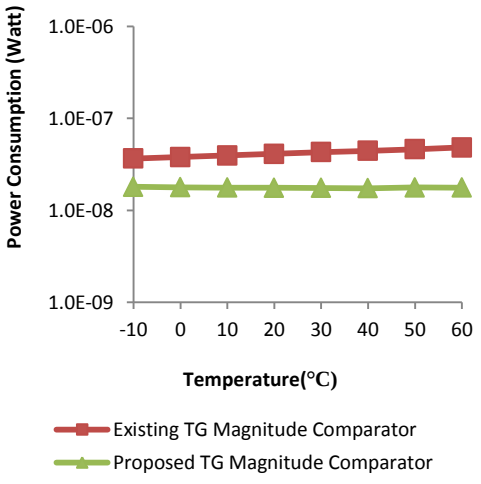


Figure 4. Power consumption at different range of temperature

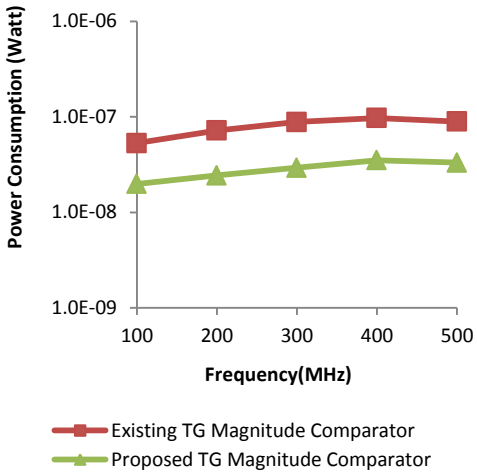


Figure 5. Power consumption by varying frequency

Fig.5 reveals that proposed design outperforms the existing design over the range of operating frequencies.

# V. Conclusion

The TG magnitude comparator using proposed technique has shown better performance in terms of power consumption and area in comparison to its peer design. From the above analysis and discussion it has been concluded that the proposed technique is outperforming the conventional technique and can be a better option for future work. The proposed logic technique can be used with various design technique to provide most viable option for circuit design.

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About Author (s):

Vijaya Shekhawat was born in June 16,1990. She received her B. Tech Degree in Electronic and Communication Engineering in 2012 and pursing M. Tech (VLSI Design) from Mody Institute of Technology and Science (Deemed University), Rajasthan, India. Her research area is in Digital low power.

**DR. TRIPTI SHARMA** earned B.E. degree in Electronics Engineering from North Maharashtra University in 2001 and M. Tech. degree in VLSI Design from Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan in 2010 as well as achieved Ph.D. in the field of low power high performance digital VLSI circuit design from Suresh Gyan Vihar University, Jaipur. After stepping into professional world, she started as lecturer with C.S.J.M University, Kanpur and continued it up to late 2003. After that she joined Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan. Her working habits and discipline made her popular among the university and she was later awarded with designation of Asst. Professor in 2009. Her current research interests include low power digital VLSI circuits. She has more than 45 papers published in International Journals and International / National Conferences. Dr. Sharma is the life member of Indian Society of Technical Education (ISTE).

**DR. K. G. SHARMA** received the B.E. degree in Electronics and Communication Engineering from Madan Mohan Malviya Engineering College, DDU University, Gorakhpur in 2001 and completed his M. Tech. degree in VLSI Design from Faculty of Engineering & Technology, Mody Institute of Technology and Science in 2009. He acheived his Ph.D. degree in the field of low power VLSI circuits from from Suresh Gyan Vihar University, Jaipur. He demonstrated his skills in Research & Development of Industrial Electronics, Kanpur for a briefer period and then he shifted to Academics and shared his knowledge as lecturer at renowned university in Kanpur in the initial stages of his career. He extended his profession as faculty of Engineering and Technology in MITS from 2003 and with experience promoted to Asst. Professor in the same university. Because of his extensive research work, he has more than 46 research papers published in various international/ national journals and conferences. Dr. Sharma is the life member of Indian Society of Technical Education (ISTE).