International Journal of Advances in Electronics Engineering – IJAEE
Volume 4 : Issue 3 *[ISSN 2278 – 215X]*
Publication Date : 30 September, 2014

ANALOGY AND ANALYSIS OF FAST ADDERS USING FPGA

ABSTRACT

Addition play important role in our day to day life the saying goes on "if you count you can control" mathematical operation are mostly used in arithmetic application, it is a basic operation for any digital electronics system, adder is a combinational circuit.Fast adder is used in digital electronics, to increase the speed by reducing the amount of time required to determine carry bit. This project deals with high data rate implementation of adder on field programmable gate array (FPGA).Different adder architecture is compare on the basis of their clock speeds & the resource utilization.

Keywords—*layout in terms of area, speed of operation, reduce propagation delay, Carry select adder, ripple carry adder,*

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I. INTRODUCTION

Digital Adder is a digital device capable of adding two digital n-bit binary numbers, where n depends on the circuit implementation. Digital adder adds two binary numbers A and B to produce a sum S and a carry C. Adder circuits are basic building blocks of digital circuits. There are a wide variety of commonly Used adder circuits, each possessing unique design tradeoffs in the balance of speed versus gate Count. Adders are also very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Fast adder circuits described in this paper are designed for operating speed, area layout, and delay. In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations.

II. FPGA TECHNOLOGY

In this paper we had designed and implement different adders on the FPGA, to classify the propagation delay, the bit slice consume by the adder and the LUT's.A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). As FPGA designs employ very fast I/Os and bidirectional data buses it becomes a challenge to verify correct timing of valid data within setup time and hold time

III. RIPPLE CARRY ADDER

Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers .Each full adder inputs a Cin**,** which is the Cout of the previous adder. This kind of adder is a Ripple Carry Adder**,** since each carry bit "ripples" to the next full adder. The ripple carry adder is constructed by cascading full adders (FA) blocks in series. The carryout of one stage is fed directly to the carry-in of the next stage. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry the first full adder may be replaced by a half adder. The block diagram of 4-bit Ripple Carry Adder is shown here below

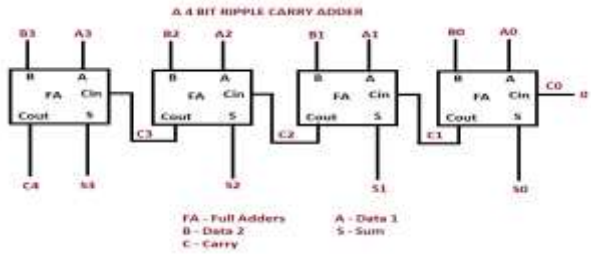

Fig.1 Ripple carry adder

The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic .In a 32-bit [ripple carry] adder, there are 32 full adders, so the critical path (worst case) delay is 31 * 2(for carry propagation) + 3(for sum) = 65 gate delays. Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry are the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. Consider a NOT gate, When the input is "0″ the output will be "1″ and vice versa. The time taken for the NOT gate's output to become "0″ after the application of logic "1″ to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out (Cout) signal.

Fig.2 RTL view of 8 bit ripple carry adder

Fig 3. Stimulation Result of 8 bit ripple carry adder

IV. CARRY SELECT ADDER

Carry select Adder is a better choice especially in the case of Carry delay. As in a ripple-carry adder, every full adder cell has to wait for the incoming carry before an outgoing carry can be generated. This dependency can be eliminated by pre-calculating i.e. by taking both possible values of the carry input and evaluating the result for both possibilities in advance. Once the real value of the incoming carry is known, the correct result is easily selected with a simple multiplexer stage. The concept of the carry-select adder is to compute alternative results in parallel and subsequently selecting the correct result with single or multiple stage hierarchical techniques In order to enhance its speed performance, the carry-select adder increases its area requirements. In carry-select adders both sum and carry bits are calculated for the two alternatives: inputs carry "0" and "1". Once the carry-in is delivered, the correct computation is chosen (using a MUX) to produce the desired output. Therefore instead of waiting for the carry-in to calculate the sum, the sum is correctly output as soon as the carry-in gets there. The time taken to compute the sum is then avoided which results in a good improvement in speed. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known.

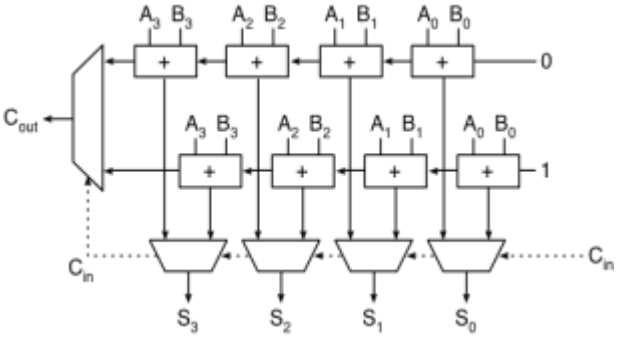

Fig.4. 4 bit carry select adder

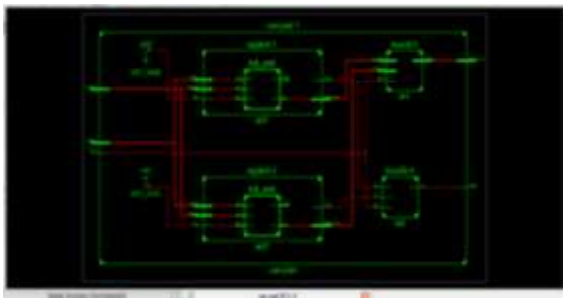

Fig 5 RTL view of 8 bit carry select adder

Fig 6.Stimulation Result of 8 bit select carry adder

V. CONCLUSION

The propagation delay of carry for ripple carry adder is more as compare to the select carry adder. The ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. in ripple carry adder the next block of adder is depend upon the carry-in of the previous adder block, but in select carry adder the appropriate carry is select with the help of the multiplexer.

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