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Implementation of Steer by Wire using FPGA

[Abd Kadir Mahamad, Sharifah Saon, King Diaw and Mohd Firdaus Mahayudin]

***Abstract*—This project is described the modeling of steer by wire (SbW) technique that implement using DE1 board to control the positioning. The variable resistor and servomotor are uses as input and output respectively. The actual position of variable resistor is translated into analog voltage signal using voltage divider theorem. The analog signal later on is converted into 10-bit digital form using A/D converter embedded in the PIC16F873A. An output from A/D converter is connected to the DE1 GPIO port as an input to the controller. The VHDL code is used to program the FPGA on DE1 board. The controller algorithm is successfully translated into the VHDL code and the DE1 boards completely act as a controller for this project. As a result, the motor pointer can follow exactly the desired pointed by the variable resistor.**

***Keywords*—Steer by Wire (SbW), DE1 board, FPGA, VHDL, PIC16F873A.**

I. Introduction

The goal of this project is to understand about the motor position controlled using DE1 board. The VHDL code is used to program the FPGA on the DE1 board in order to implement the control system such as PID control technique. Next, DE1 board was used to control the rotation of the DC motor position so that the motor can point to the angle (target) desired by user in the most stable manner. There are two project objectives. The first objective is to develop a project that a motor can be control or rotates as variable resistor rotates in highly accurate. The second objective is to implement servo motor control algorithm in FPGA board.

II. System Architecture

A. *Drive by Wire (DbW)*

DbW technology in the automotive industry replaces the traditional mechanical control systems with electronic control systems using electromechanical actuators and human-machine interfaces such as pedal and steering feel emulators [1]. Hence, the traditional components such as the steering, shafts, pumps, hoses, belts, coolers and vacuum servos and master cylinders are eliminated from the vehicle.

Abd Kadir Mahamad, Sharifah Saon, King Diaw and Mohd Firdaus Mahyidin
Embedded Computing System, Department of Computer Engineering, Faculty of Electrical & Electronic Engineering, Universiti Tun Hussein Onn Malaysia
Malaysia

B. *Steer by Wire (SbW)*

This is currently used in electric forklifts and stock pickers and some tractors. Its implementation in road vehicles is limited by concerns over reliability although it has been demonstrated in several concept vehicles such as ThyssenKrupp Presta Steering's Mercedes-Benz Unimog, General Motors' Hy-wire [1] and Sequel and the Mazda Ryuga. A rear wheel SbW system by Delphi however is called as Quadrasteer is used on some pickup trucks but has had limited commercial success.

C. *Altera DE1 Development and Education board*

The board offers a rich set of features that make it suitable for use in laboratory environment especially for university and college students, for a variety of design projects, as well as for the development of various digital systems. The DE1 board features a state-of-the-art Cyclone® II 2C20 FPGA in a 484-pin package. All important components on the board are associated to pins of this chip, allowing the user to manage all aspects of the board's operation. While the specification components on DE1 board including Cyclone II EP2C20F484C7 FPGA and EPCS4 serial configuration device, I/O devices, 8-MB SDRAM, 512-KB SRAM, 4-MB flash, switches, displays, LEDs, and clocks.

D. *Servomotor*

A servomotor is a rotary actuator that allows for precise control of angular position [2]. It consists of a motor coupled to a sensor for position feedback with reduction gearbox. It also requires a fairly sophisticated controller, regularly a dedicated module designed specifically for use with servomotors. The image of the servomotor used in this project shown as in Fig. 1.

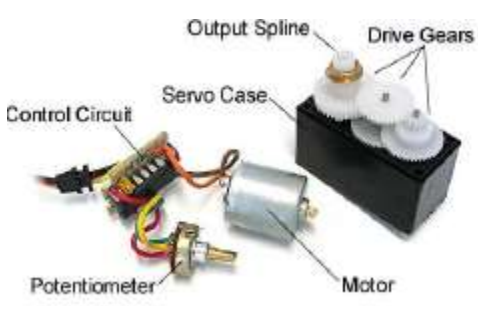

Figure 1. Servomotor

E. *PIC16F873A as A/D converter*

This microcontroller is powerful which capable to execute an instruction within 200 ns, yet easy-to-program with only 35 single word instructions. It used CMOS FLASH-based 8-bit microcontroller packs. One of the features embedded in this microcontroller is Analog-to-Digital (A/D) Converter module. The conversion of an analog input signal results in a corresponding 10-bit digital number. The analog and digital module has high and low-voltage reference input that is software selectable to some combination of Vdd, Vss, RA2 or RA3 as describe in Fig. 2.

III. Methodology

To achieve the goal, an algorithm as describe in flow chart shown in Fig. 3 is used in this project. Since the output is a servomotor that has controller circuit embedded inside it. Our task is just identified the position that motor pointer needed to move. Secondly, convert the desired position into the PWM signal that will be used to control the servomotor.

A. *Project Hardware Arrangement*

The operation of this project can be described as block diagram shown in Fig. 4. By applying voltage divider theorem, the variable resistor can be used as position sensor. Since the DE1 board not have built-in A/D module, the analog signal from outside cannot connected directly to the DE1 board. Thus, in this project the PIC16F873A is used to convert analog voltage from variable resistor by converted it into 10-bit digital representation.

An input from the user is processed by FPGA according to the program that has been written. As a result, the 64 *kHz* Pulse Width Modulation (PWM), produces a control signal to the servomotor, in the operational range of 0.5 *ms* to 2.5 *ms*. While the PWM signal is connected to the servo motor through GPIO port. Table 1 describes the GPIO port used to interface with the A/D input and PWM output.

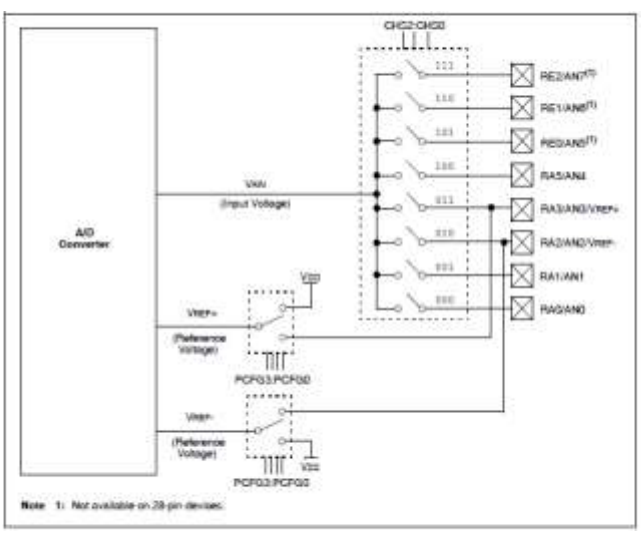

Figure 2. A/D Converter Module

TABLE 1. GPIO PORT USED TO INTERFACE WITH THE A/D INPUT AND PWM OUTPUT

GPOI port (JP1 connector)	Interface to
IO_A11	ADC(0)
IO_A13	ADC(1)
IO_A15	ADC(2)
IO_A17	ADC(3)
IO_A19	ADC(4)
IO_A21	ADC(5)
IO_A23	ADC(6)
IO_A25	ADC(7)
IO_A9	ADC(8)
IO_A7	ADC(9)
IO_A5	PWM

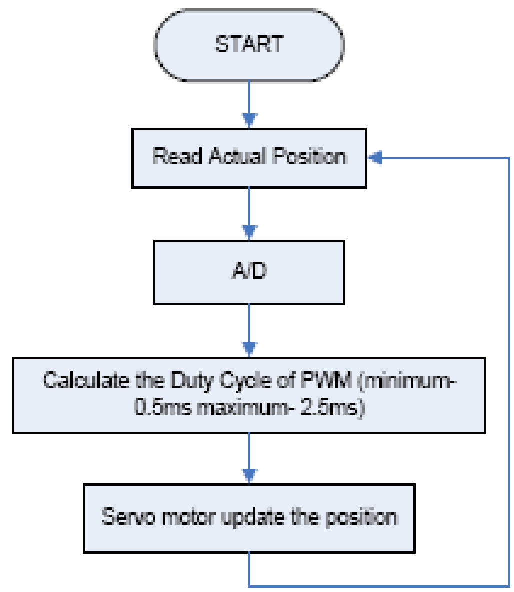

Figure 3. Flow Chart of Controller Algorithm

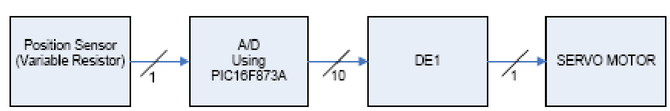

Figure 4. Project Block Diagram

B. *Servo Motor Control with VHDL*

The rotation of servomotor can be control by applying PWM to the signal cable of servomotor continuously [3]. The control signal for the servomotor is based on refresh frequency of 50 *Hz* and pulse width range from 0.5 *ms* to 2.5 *ms*. In order to design the control signal, the following steps are required:

a) Range operation as in (1)

$$range = time_{max} - time_{min} = 2.5\,ms - 0.5\,ms = 2\,ms \quad (1)$$

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b) The resolution for the servo motor using (2)

$$f_{needed} = \left(\frac{range}{revolutions} \right)^{-1} \quad (2)$$

where, revolution is the number of position of servomotor.

Thus, $f_{needed} = \left(\frac{2\,ms}{128} \right)^{-1} = 64\,kHz$

c) Onboard crystal oscillator of 50MHz is used, and Fig. 5 shown the flow chart for frequency divider 64 *kHz*.

d) Write the servo module in VHDL to implementation three inputs: 64 *kHz* clock, reset, and a vector that take the values from 0 to 127.

e) Finally, use PORT MAP instruction to write VHDL code as describes in Fig. 6.

IV. Data Analysis and Discussion

This section will focus on discussion and analysis the simulation and actual result. The VHDL code will be simulate using software Quartus II to observe the waveform. While for the actual result, the waveform is observe using digital oscilloscope.

A. *PWM Signal for Servomotor*

Generated PWM signal is produced with the frequency of 64 kHz, so that the FPGA need a frequency divider of 64 kHz. Since the Fosc on DE1 board is 50MHz. Thus, the "clk" is set to 50 MHz. Fig. 7 shown the result of simulation waveform. The period of the "clk_out" bit is 15.625 μs (f = 64 kHz). Meanwhile, functional simulation of VHDL code for two values of "pos" variable which is 0 (minimum) and 127 (maximum) is done to represented the range of 0.5 ms and 2.5 ms respectively. The simulation waveform for Ton 0.5ms and 2.5ms are shown in Fig. 8 and Fig. 9.

B. *FPGA Analysis*

The FPGA of DE1 board is used to store the VHDL code that makes the board act as a controller for this application. Since inside the FPGA is a logic element, the VHDL code that loaded into FFPGA will used logic element to perform the task. The tool such as RTL viewer can be use to aid the user to visualize the VHDL code inside the FPGA board. Fig. 10 illustrates the RTL viewer for this project. As describe in RTL viewer, this project uses three inputs which are "clk_in", "adc[9…0]" and "reset" and two output which are "pwm" and "ledr[6…0]. The "pwm" signal is to control the position of the servomotor and "ledr" is used to display the logic input of the "pos" signal. Finally Fig 11 shows the overall proposed system of steer by wire using DE1 board.

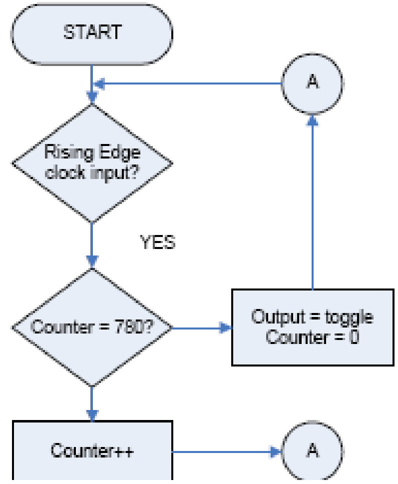

Figure 5. Flow Chart for Frequency Divider of 64 *kHz*.

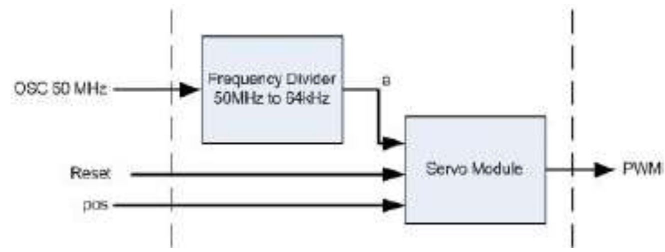

Figure 6. Block Diagram of PWM Generator for Servo Motor

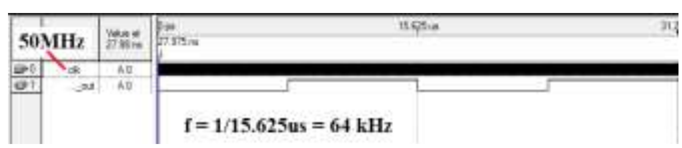

Figure 7. Frequency Divider 50 MHz to 64 kHz

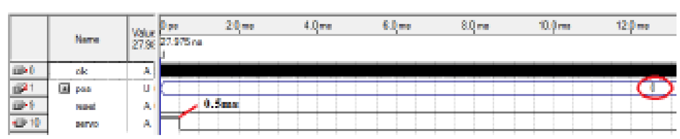

Figure 8. Servo Signal when "pos" is Set to 0

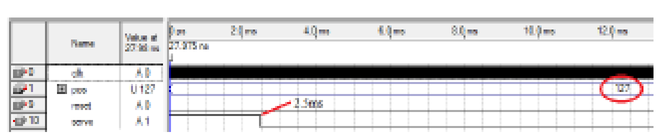

Figure 9. Servo Signal when "pos" is Set to 127

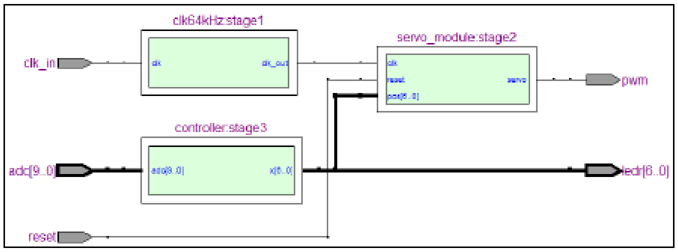

Figure 10. RTL viewer

Figure 11. Proposed System of Steer by Wire

V. Conclusion

As the conclusion, all the objectives project were achieved. The actual position of variable resistor is translated into analog voltage signal using voltage divider theorem. The analog signal then is converted into 10-bit digital form using A/D converter embedded in the PIC16F873A. An output from A/D converter is connected to the DE1 GPIO port as an input to the controller. The VHDL code is used to program the FPGA on DE1 board. The controller algorithm is successfully translated into the VHDL code and the DE1 boards completely act as a controller for this project. As a result, the motor pointer can follow exactly the desired pointed by the user.

Acknowledgment

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About Author (s):

Abd Kadir Mahamad received his B.E. and M.S. in Electrical Engineering from Universiti Tun Hussein Onn, Malaysia and PhD in Electrical Engineering from Kumamoto University, Japan. He is currently a Senior Lecturer at Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia. His research interests include intelligent systems application, fault diagnosis and prognosis especially for electrical rotating machinery.

Sharifah Saon received her B.E. and M.S. in Electrical Engineering from Universiti Tun Hussein Onn, Malaysia. She is currently a Lecturer at Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia. Her research interests mainly on signal processing.

King Diaw received his B.E. in Electrical Engineering from Universiti Tun Hussein Onn, Malaysia. He is currently pursuing M.S degrees at Universiti Tun Hussein Onn, Malaysia, and a lecturer at Politeknik Tunku Syed Sirajuddin, Perlis, Malaysia.

Mohd Firdaus Mahayudin received his B.E. in Electrical Engineering from Universiti Tun Hussein Onn, Malaysia. He is currently pursuing M.S degrees at Universiti Tun Hussein Onn, Malaysia, and a lecturer at Politeknik Sultan Haji Ahmad Shah, Kuantan, Malaysia.