International Journal of Advancements in Electronics and Electrical Engineering – IJAEEE
Volume 3: Issue 2 *[ISSN 2319 – 7498]*
Publication Date : 25 June 2014

Multilevel System for Thermal Design, Control and Management of Electronic Components

K. O. Petrosyants, I. A. Kharitonov, P.A. Kozynko, N.I. Ryabov

***Abstract*- The methodology and software tools for multi-level thermal and electro-thermal design of electronic components are presented. The discussion covers 2D/3D constructions of: 1) discrete and integrated semiconductor devices; 2) monolithic and hybrid ICs and VLSIs; 3) Hybrid ICs, MCMs and PCBs. The actual test validation using IR thermal measurement is demonstrated for all types of components.**

Keywords - thermal design, heat conduction, semiconductor devices, circuits and VLSIs, PCBs, packages, IR temperature control.

I. Introduction

The modern electronic devices, chips, PCBs and units demonstrate growing power density and element temperatures. High working temperatures due to increasing power density impact not only electrical parameters of elements on a chip or a board, but they force undesirable physical-chemical processes in their materials and constructions as well. These may lead finally to the fault. The most effective way to provide safe thermal regimes of electronic equipment is temperature investigation in the different levels of electronic components: semiconductor devices, chips, PCBs, units. The leading industrial companies have developed application-specific software tools for thermal design of microprocessors [1, 2], power devices and electronic systems [3, 4], digital CMOS VLSI's [5], analog ICs [6] and other applications.

The novel trend in thermal control and management for different families of electronic systems-on-chip/board is the development of general modeling, control and management platforms like THERMINATOR [7]. This platform is based on integrated methodology. For different types of components different types of models are developed: numerical accurate electro-thermal TCAD device models; circuit-level SPICE ET device models; ET macromodels for circuit fragments; behavioral logic-thermal models for digital blocks. Thermal interaction between devices, chips, blocks as well as thermal transportation to/from environment are accounted by the models generated for the substrate, the package and the board. In [7] only the strategy of developing new paradigma of thermal design was discussed, practical results were not presented.

In this paper the real working version of a multi-level system for thermal design of electronic components is presented (see Fig. 1). It consists of two parts. The hierarchical set of thermal simulation tools is coupled with common hardware/software subsystem for IR temperature control and measurement to verify the results of thermal and electro-thermal design of different types of components and systems-on-chip/board.

K. O. Petrosyants, I. A. Kharitonov, N.I. Ryabov
Moscow Institute of Electronics and Mathematics of National Research University "Higher School of Economics"
Russia

P.A. Kozynko,
Mentor Graphics
USA

II. Level 1: Discrete Semiconductor Devices and IC Elements

For these components it is necessary to take into account the effect of selfheating due to the high power density dissipated in device structures. For this purpose two types of electro-thermal models are used: 1) TCAD models for simulation of temperature distribution in 2D/3D physical structures of devices; 2) compact SPICE electrical models with additional "thermal subcircuit" for following electro-thermal circuit simulation.

A TCAD Software Tools for Numerical Simulation of Coupled Electrical Transport and Heat Conduction Phenomena

The tools Sentaurus (Synopsys) and SELFHEATING (MIEM) solve the 2D-3D problem of temperature distribution in different device constrictions. In Sentaurus the thermodynamic version of the carrier transport equation in semiconductors is used. The flow of currents due to the gradients of the electrical potentials and temperature is coupled with the classic heat conduction equation:

$$\overrightarrow{J_{n,p}} = -nq\mu_{n,p}(\nabla\Phi_{n,p} + P_{n,p}\nabla T), \quad (1)$$

$$c\frac{\partial T}{\partial t} - \nabla\lambda\nabla T = -\nabla(P_n T + \Phi_n)\overrightarrow{J_n} + (P_p T + \Phi_p)\overrightarrow{J_p}, \quad (2)$$

where: μ_n and μ_p are the electron and hole mobilities; Φ_n and Φ_p – quasi-Fermi potentials; P_n and P_p – absolute thermoelectric powers; λ – the lumped electron-hole-lattice thermal conductivity; c – lattice heat capacity.

The 2D temperature distribution in bipolar transistor structure of 0.8 μm – BiCMOS VLSI is shown in Fig. 2. BJT dissipates the power of 10 mW. The "hot spot" with temperature ~80 ºC is located in the depth of base-collector junction under emitter area. This example illustrates the fact that for submicron elements of VLSIs critical "hot spots" are usually located in the depth of the device structure and cannot be measured by traditional IR thermography methods. TCAD modeling is the only real method to predict the thermal behavior of the device.

The SELFHEATING software tool (developed by us) is used for device layout optimization. The classic 3D heat conduction equation is numerically solved for multi-layer device structure Fig. 3:

$$gc\frac{\partial T}{\partial t} - \lambda\nabla^2 T = -P, \quad (3)$$

where P(x,y,z,t) is power density, g – specific gravity.

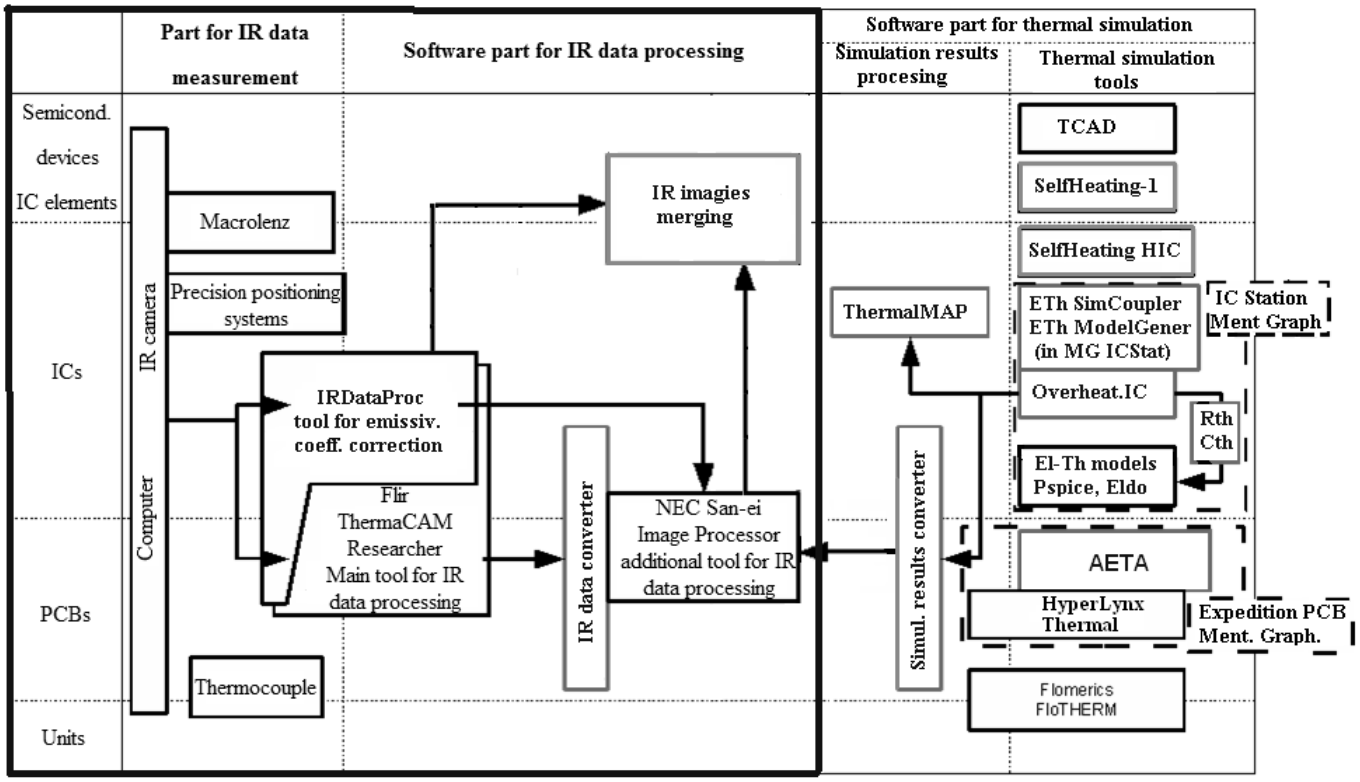


Figure 1. Multilevel subsystem for electronic components thermal regimes investigation

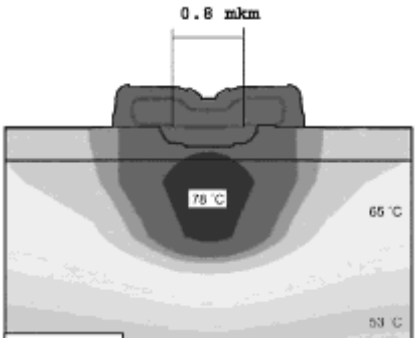


Figure 2. TCAD Simulated temperature distribution in bipolar transistor structure cross section.

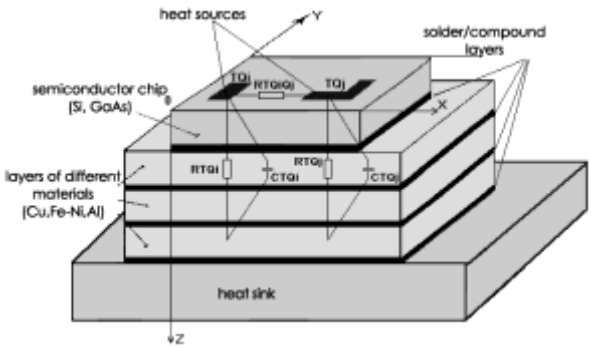


Figure 3. Multi-layer semiconductor device/IC structure

Simultaneously with (1) the 2D equation for electrical potential U_ξ and current density j_ξ distributions in the device layout *(X,Y)* is solved:

$$\nabla\left[\rho^{-1}\nabla U_\xi\right] = j_\xi(x, y, U_\xi, T_\xi)\,, \qquad (4)$$

where: ρ_ξ is local resistivity in ξ-th semiconductor region.

The example of power bipolar transistor layout with built-in temperature emitter-sensor is presented in Fig. 4 as an example. BJT power is 1.3 W. It is important to note that simulated temperature distribution and equipotential lines along the semiconductor device layout help the designer to provide the device layout optimal from the electro-thermal point of view.

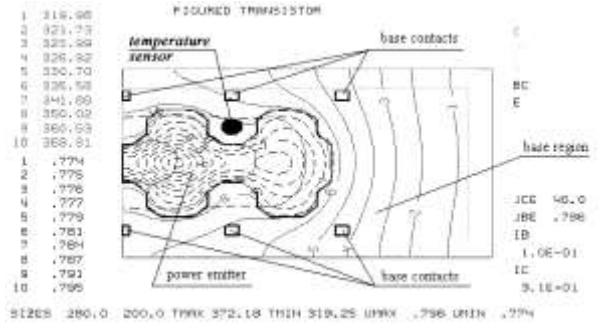
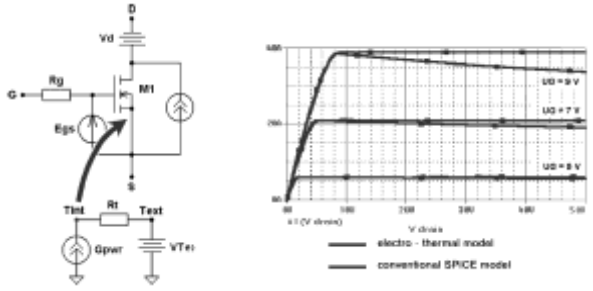


Figure 4. Simulated temperature distribution along layout of the power bipolar transistor with built-in temperature sensor

B. Compact SPICE electro-thermal models

Compact SPICE electro-thermal models were developed for passive elements (resistors and capacitors); power diodes, power BJTs, MOSFETs, MESFETs, IGBTs and elements of submicron and deep submicron VLSIs: BJTs, SiGe HBTs, MOSFETs, SOI/SOS MOSFETs, BiCMOS, SiGe BiCMOS, Bi-CMOS-DMOS, GaAs MESFETs/HEMTs. These models were included into SPICE, HSPICE, Eldo, Spectre model libraries as subcircuits.

For example, electro-thermal model for MOSFET (DMOSFET) is shown in Fig. 5 (a). It consists from electrical and thermal parts. The comparison between output I-V characteristics of power MOSFET simulated with electro-thermal (Fig. 5(a)) and conventional SPICE models is shown in Fig. 5 (b). The well-known selfheating effect of MOSFET is seen.



(a) (b)

Figure 5. Electro-thermal SPICE model for MOSFET (a) and comparison between MOSFET output characteristics simulated with electro-thermal (Fig. 5(a)) and conventional SPICE models

The developed compact electro-thermal models make possible to simulate the whole IC with commercial SPICE like simulation tools and to obtain electrical characteristics and local temperatures of all elements on the chip.

II. Level 2: Monolithic ICs

The thermal design subsystem developed by us and integrated with Mentor Graphics IC Station Framework is shown in Fig. 5 [8].

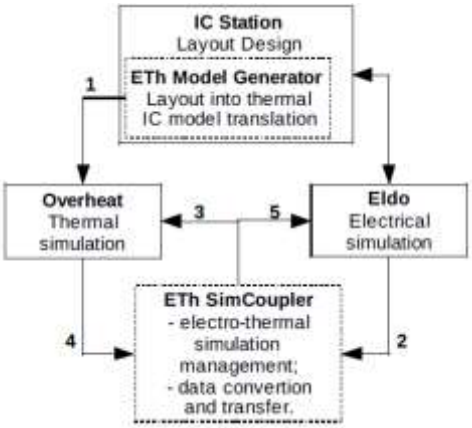


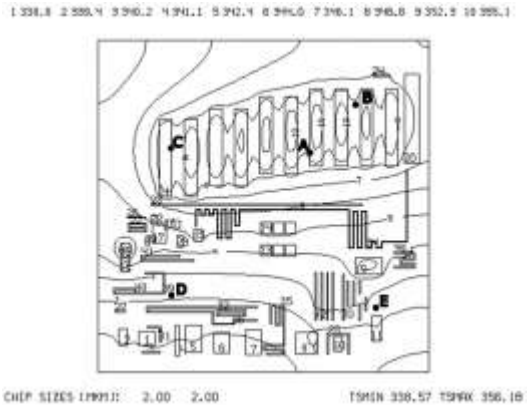
Figure 6. Thermal design subsystem in MG IC Station framework

As it is seen two main software tools, OVERHEAT for quasi-3D temperature simulation, and ELDO for electrical circuit simulation are coupled into an iteration loop to provide the solution of the electro-thermal problem for multi-layer structure of IC chip (Fig. 3). Two additional tools ETh Model Generator and ETh SimCoupler are used. ETh Model Generator converts layout information from IC Station to OVERHEAT native format and creates description of chip layers. ETh SimCoupler carries out the process of electro-thermal simulation coupling of OVERHEAT and ELDO simulators.

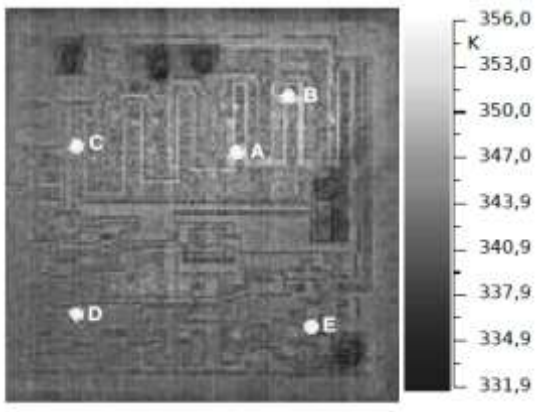
The weak point of the many other known thermal design subsystems is that they don't guarantee the correct values of thermal resistances RT_{ij} and capacitances CT_j for SPICE electro-thermal models (see Fig. 3). This problem does not exist in the presented subsystem because OVERHEAT tool does calculate the thermal resistances matrix and the thermal capacitances column for all elements of the IC chip.

The possibilities of the developed subsystem are demonstrated in Fig. 7. Fig. 7 (a) presents the quasi-3D simulated temperature distribution along the surface of integrated voltage regulator 142EN9 chip (V_{IN}=40 V, V_{OUT}=27 V, P=7 W). The measured temperature distribution along the IC chip surface (see Fig. 7(b)) was obtained with FLIR A-40 IR camera. A good agreement between the measured and simulated 2D temperature distributions can be seen.

To account for package influence on the IC chip thermal behavior the software tool OVERHEAT-BGA was developed. The tool simulates the 3D-temperature distribution in the layers of "chip in BGA package" construction. The quasi-3D approach was used in this tool to reduce CPU time by 6–10 times in comparison with universal 3D simulators like ANSYS and others [9]. Our experience shows that the quasi-3D approach would be effectively applied to modern POP and TSV 3D "IC chip in Package" systems.



(a)



(b)

Figure 7. The simulated with Overheat (a) and measured with Flir A40 IR camera (b) temperature distribution along the voltage regulator 142EN9 chip surface

III. Level 3: Hybrid ICs, Multi Chip Modules and PCBs

For some PCB design systems the thermal simulators can be used together with the built in circuit simulators [10–13]. But the process of power-temperature exchange between electrical and thermal simulators is not automated and is

implemented manually by user. The automation of PCB electro-thermal analysis is the main requirement to provide effective design: to eliminate human errors, significantly decrease labor inputs, simulation time, and increase simulation accuracy and reliability. We have developed the new version of Mentor Graphics automated electro-thermal PCB design system where Thermal tool and HyperLynx Analog tool are coupled into an iteration loop to carry out the process of electro-thermal PCB simulation [14]. The additional tool AETA is introduced to couple HyperLynx Analog and HyperLynx Thermal simulation tools (Fig. 8)

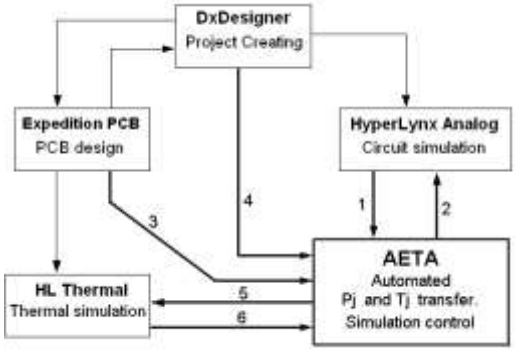


Fig.8. The new version of Mentor Graphics automated electro-thermal PCB design system.

The effectiveness of the new version of electro-thermal PCB design system is demonstrated by the example of DC/DC converter PCB simulation (see Fig. 11) The board contained 98 circuit elements. Converter was simulated for 24 V input voltage, 5 V output voltage and load resistor of 7.5 Ohm. The net list for circuit simulation model was prepared using DxDesigner tool. PCB placement and routing were made with Expedition PCB. Board size was 150×80 mm^2. Fig. 11 shows the 2D temperature distributions on the DC/DC converter board (with dots marked) simulated by HyperLynx Thermal using automated electro-thermal method realized with the help of AETA tool. Comparison of the simulated and the measured temperature values is presented in Table 1. The simulation process finished in 3 iterations and took 8 seconds time of PC computer (4 Gb RAM, 2.6 GHz CPU frequency) with GNU/Linux version 2.4.18 operating system). The accuracy parameter was set to 10 mW. For comparison, the standard non-automated simulation took nearly 80 min of human time.

The tendency of reduction of PCB copper traces sizes involves increase in current density and, as a result, increases of working temperatures. This task was analyzed by us for modern PCB traces with the different sizes and substrate materials using three software tools: ANSYS, HyperLynx Thermal and ELCUT. The simulation results were compared with IR measurement results [15] and are presented in Fig. 9.

IV. Thermal Measurement Subsystem

Normally thermocouples may be used to monitor device temperature on board (PCBs and MCMs). It is a cheap and simple way of thermal measurement. However it is not possible to use thermocouples for systems on a chip because of small size of components and a large number of points to be monitored.

To measure both the IC chip and PCB/MCM temperature maps an IR-camera is used. FLIR A40 IR-camera has thermal sensitivity of 80 mK when temperature is 25 °C, resolution of 320×240 pixels and tolerance of ± 2 °C. The additional 18 micron macrolens is supplied for chip measurement. FLIR THERMACAM RESEARCHER and NEC San-ei Image Processor software tools are used with the camera to provide temperature visualization and image processing. Two additional original software tools have been developed to extend the subsystem abilities: 1) IRDataProc – a tool for object emissivity coefficients map generation and object temperatures correction; 2) IR data converter – an interface between Flir ThermaCAM Researcher and NEC San-ei Image Processor software tools. For submicron VLSIs the temperature measurements are carried out using the QFI InfraScope with high linear resolution.

V. Conclusions

The multi-level thermal design system was developed for different types of microelectronic components: from submicron devices and ICs to MCMs and PCBs. The modeling methodology and software tools for each level of components are discussed and illustrated by practical examples.

Acknowledgement

This work was implemented in the framework of the Basic Research Program of the National Research University Higher School of Economics (HSE) in 2014 and Russian Foundation for Basic Research (grant 12-07-00506).

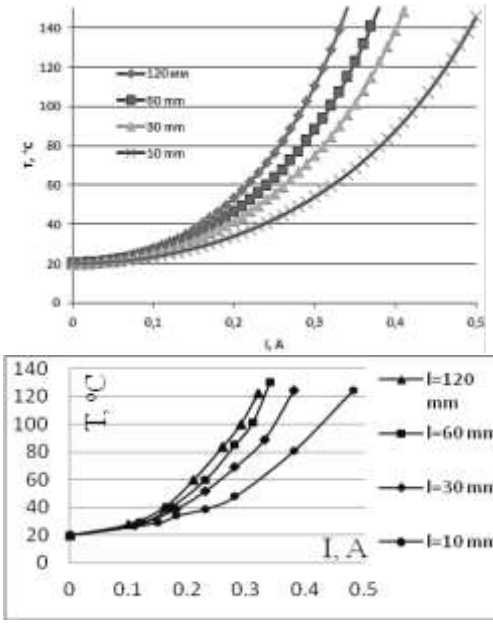


Figure 9. ANSYS simulation results (a) and the measured data (b) for thermal rise in traces with different lengths as a function of current (simulation error is less than 3%)

References

[1]. A. Naveh, E. Rotem, A. Mendelson et al., "Power and Thermal Management in the Intel Core Duo Processor", Intel Technology Journal, vol. 10, No. 2, pp. 109–121, 2006.

[2]. G. Goth, A. Arvelo, J. Eagle, M. Ellsworth, "Thermal and mechanical analysis and design of the IBM Power 775 water cooled supercomputing central electronics complex", Proc. of IEEE Conf. on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), pp. 700 – 709, 2012.
[3] M. Marz, P. Nance, "Thermal Modeling of Power Electronic Systems", White Paper of Fraunhofer Inst. And Infineon Techn., pp. 1–20, April 2000.
[4] SupIRBuck Design Tool, www.mypower.irf.com.
[5] Cheng Y.-K., Rosenbaum E., Kang S.-M., "Improvement on chip-level electrothermal simulator-ILLIADS-T", IEEE International Symposium on Circuits and Systems, ISCAS '96, vol. 4, pp. 432 – 435, 1996.
[6] Szekely V., Poppe A., Hajas G., "Electro-thermal transistor models in the SISSI electro-thermal IC simulator", Proceedings of the 5th International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2004, pp. 105 – 112, 2004.
[7] A. Calimera, A. Macii, E. Macii, S. Rinaudo, M. Poncino., "THERMINATOR: modeling, control and management of thermal effects in electronic circuits of the future", Proc. THERMINIC 2010, pp. 171-176, 2010.
[8] K. O. Petrosyants, N. I. Rjabov, I. A. Kharitonov, P. A. Kozynko, "Electro-thermal simulation: a new subsystem in Mentor Graphics IC Design Flow", Collection of papers on THERMINIC–2009, Leuven, Belgium, pp. 70–74, Oct. 2009.
[9] K. O. Petrosyants, N. I. Rjabov, "Quasi-3D approach for BGA Package Thermal Modeling", Proc. of THERMINIC, pp. 158–161' Sept. 2012.
[10] http://www.ansys.com/Products/Simulation+Technology/Fluid+Dynamics/ANSYS+Icepak.
[11] www.ozeninc.com/downloads/ANSYS_TASPCB.pdf.
[12] http://en.rebeca3d.com/?page_id=184.
[13] Mentor Graphics Corporation Mentor Graphics PCB Design Creation. — http://www.mentor.com/ products/pcb-system-design/design-creation/;
[14] Petrosyants K., Kozynko P. A., Kharitonov I. A., Sidorov A., Chichkanov Y., "New Version of Automated Electro-Thermal Analysis in Mentor Graphics PCB Design System", Proceedings of IEEE East-West Design & Test Symposium (EWDTS'12), pp. 289-292, Sept. 2012.
[15] K. O. Petrosyants, A. A. Popov, "Experimental Investigation of Temperature-Current Rise in Fine PCB Copper Traces on Polyimide, Aluminium and Ceramic (Al_2O_3) Substrates", Advanced Materials Research, vol. 739, pp 155-160, 2013.

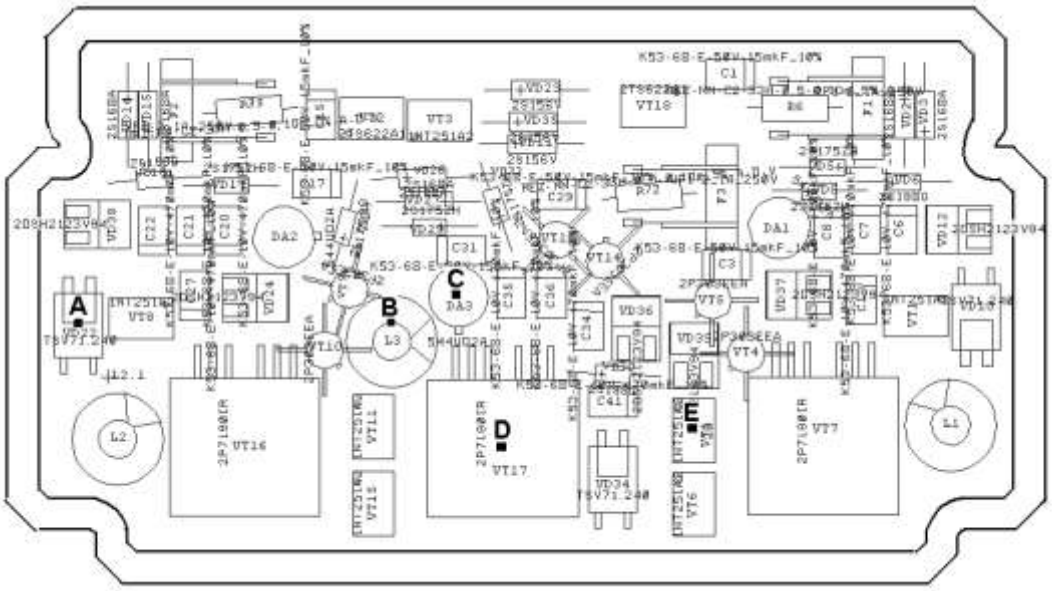


Figure 70. DC/DC converter PCB

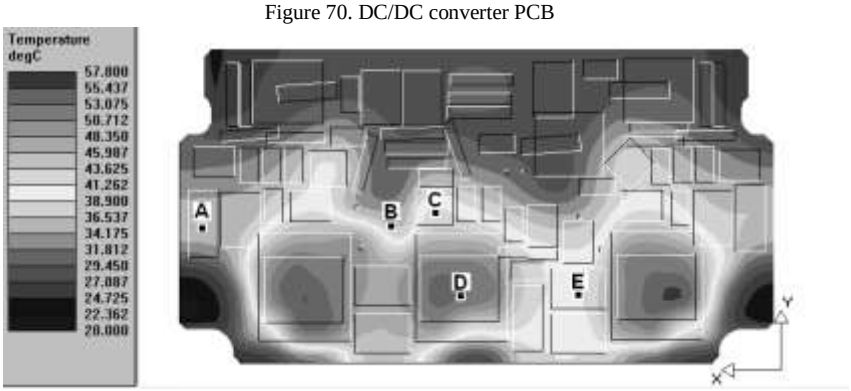


Figure 8. Temperature map on the DC/DC converter board simulated with the automatic electro-thermal scheme

TABLE I. COMPARISON BETWEEN THE SIMULATED AND THE MEASURED TEMPERATURE VALUES OF PCB CONVERTER (FIG. 12) ELEMENTS

	Temperatures, °C				
Points on the board surface	***"A" Power Diode***	***"B" Inductance***	***"C" OpAmp***	***"D" Power transistor***	***"E" Medium power transistor***
Automated electro-thermal simulation	36.5	35.4	41.3	57.68	41.2
IR measured values	38	38	39	55	43
Error, %	3,9	6.8	4.4	2.4	4.2

About Author (s):

Konstantin O. Petrosyants -
Professor, Dr. of Eng. Science, Head of the Department of Electronics and Nanoelectronics, Moscow Institute of Electronics and Mathematics of National Research University of Higher School of Economics.
He was born in Moscow on April 9, 1944. In 1968 he graduated from Moscow State Institute of Electronics and Mathematics in Electrical Engineering and joined the Department of Microelectronics.
His area of interests is modeling of semiconductor devices and VLSI circuits taking into account thermal and radiation effects. He has more than 260 publications, among them – 4 technical monographs.
He has presented the results of his scientific research at many international conferences, symposiums, exhibitions in USA, UK, France, Germany, Italy, Belgium, Portugal, Spain, Finland, Greece, Poland, Hungary, Japan, China, Singapore, India, Uruguay and South Africa.

Igor A. Kharitonov -
Bachelor of Eng. Science, Professor of the Department of Electronics and Nanoelectronics, Moscow Institute of Electronics and Mathematics of National Research University of Higher School of Economics
He was born in Moscow on February 10, 1962. In 1985 he graduated from Moscow State Institute of Electronics and Mathematics.
His areas of interest are semiconductor devices and circuits characteristics investigation and SPICE simulation with account for thermal and radiation effects, Infra Red thermography application for electronic components investigation. He has more than 90 publications.
He has presented the results of his scientific research at Russian and international conferences, symposiums, exhibitions in Germany, Spain, China, South Africa.

Nikita I. Ryabov -
Bachelor of Eng. Science, Assistant Professor of the Department of Electronics and Nanoelectronics, Moscow Institute of Electronics and Mathematics of National Research University of Higher School of Economics.
He was born in Prague on July 29, 1954. In 1976 he graduated from Moscow State Institute of Electronics and Mathematics.
His area of interest are electro-thermal simulation of semiconductor devices and circuits. He has more than 50 publications.
He has presented the results of his scientific research at Russian and international conferences, symposiums, exhibitions in USA, Germany, Spain, South Africa.

Petr A. Kozynko-
Bachelor of Eng. Science, Assistant Professor of the Department of Electronics and Nanoelectronics, Moscow Institute of Electronics and Mathematics of National Research University of Higher School of Economics.
He was born in Moscow on June 21, 1980. In 2003 he graduated from Moscow State Institute of Electronics and Mathematics.
His area of interest is electro-thermal simulation of ICs and PCBs. He has more than 40 publications.
He has presented the results of his scientific research at Russian and international conferences, symposiums, exhibitions in USA, Germany, Spain, Finland.