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# Design and Simulation of RF-CMOS SPST Switch for Reconfigurable RF front-end

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***Abstract*— The consumer demands on having multi-functional wireless communication devices have driven current mobile handset to be more complex than it has ever been before. In particular, radio frequency (RF) front-end has evolved to adapt with multi-standards terminals. Thus, by having integrated switches and resonators on the same chip may be considered as a compact solution. In this paper, the design and simulation of RF-CMOS SPST switch is presented. The switch exhibits insertion loss of 1.15-dB and 1.155-dB at 850MHz and 1.125GHz respectively. On the other hand, the isolation is > 22dB in this frequency range while its P1dB is > 20dBm. Pre and post layout of the switch is included in this paper to observe the effect of parasitic capacitance in the layout design.**

***Index Terms*— Complementary metal-oxide semiconductor (CMOS), surface acoustic wave (SAW) resonator, microelectromechanical systems (MEMS), single pole single throw (SPST), radio frequency**

## I. Introduction

TO date, mobile communication technology has shown remarkable advancement in radio frequency (RF) regime. Mobile handset capabilities have evolved from supporting only voice communications to complex smartphones with wireless data and voice communications. New standards for wireless communication such as 3G, 4G, wide code division multiple access (WCDMA), and long term evolution (LTE) require the mobile handset to cope with numerous operating frequency bands in the receiver site[1,2]. In this regard, a reconfigurable transceiver RF front-end architecture can realize multi-band single chip solution [3]. This approach may modify current superheterodyne architecture that resides in RF front-end mobile handsets. As a result, RF channel-select filter which consists of an array of microelectromechanical systems (MEMS) resonators and switches on the same chip could be implemented as shown Figure 1. Based on work in [3], they implemented this approach using aluminum nitride (AlN) technology for both the resonators and the switch designs. Although they have proven the ability to integrate MEMS resonator and switch on the same chip, the fabrication steps involved in realizing the MEMS structure could be very tedious. In this work, a fully integrated complementary metal oxide semiconductor (CMOS) MEMS SAW resonator integrated with CMOS switch as a compact solution is proposed. This approach differs from the one in Upenn's group of researchers that has already been implemented [3]

According to Piazza, by having MEMS resonators, switches and filters integrated on the same chip, parasitic capacitance and power consumption could be reduced since there are less interconnections between RF front-end components [3]. In this paper, the design and simulation of RF CMOS switch for reconfigurable RF front-end is discussed. Later, this CMOS switch will be integrated with MEMS surface acoustic wave (SAW) resonator different to that of the one developed in [3]. The CMOS switch design is based on single pole single throw (SPST) topology. The proposed design for reconfigurable RF front end, theoretical aspect of CMOS switch, followed by pre and post layout simulation is discussed in section II, III, IV and V respectively.

## II. Reconfigurable RF Front-end

As shown in Figure 1, the RF front-end could be reconfigured from single-band multichip to multi-band single chip implementation. Typical passive components use for filtering is mainly SAW filters, quartz crystal, ceramic filters, and film bulk acoustic resonator (FBAR) filter while RF MEMS switches are of interest for transmit/ receive (T/R) switches components [4][5]. In this case, both designs of RF CMOS switches and SAW resonators are fabricated in 0.35µm standard CMOS technology. Standard CMOS technology is used due to its low cost and less number of steps needed to fully realize the structure of SAW resonators unlike fabrication of the GaAs device used in [1]. For clarity, the design would consist of two SAW resonators integrated with RF CMOS switch. The RF CMOS switch design is based on SPST topology mentioned earlier in section I. In addition, for the design of SAW resonators, it is based on previous work

which has been reported in [6]. The full design is expected to be operating at two distinct frequencies i.e. 850MHz, 1.125GHz and is currently under development.

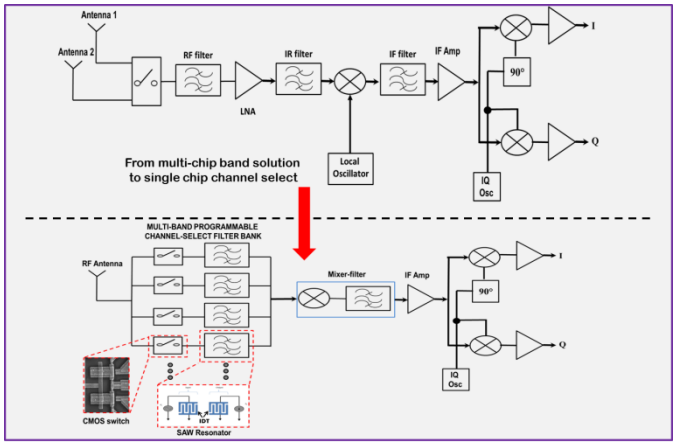


Fig.1: Reconfigurable RF front-end with multi-band single-chip implementation [3]

## III. RF CMOS Switch Design Theory

The objective of having an RF CMOS switch in this design is to alternately connect between individual SAW resonators according to desired frequency. A good RF CMOS switch can be measured in terms of low insertion loss, high isolation, as well as optimum power handling capacity [7]. In this paper, common designs of RF CMOS switch which is presented.

### A. *Single MOS Transistor*

Instead of analyzing the whole schematic, a single MOS transistor analysis would be sufficient to provide useful parameters that affect the switch performance. Figure 2 (a) illustrates the single transistor switch in 50 Ω system together with its approximate equivalent circuit shown in Figure 1 (b). The transistor's on resistance, $R_{ON}$ is depicted in Figure 2 (b) plays an important role in determining the insertion loss. $R_{ON}$ of the transistor when operating in low frequency is relatively small as compared to that of GHz frequency range. In order to analyze circuit in Figure 2, assume that the transistor is operating in linear region and thus $R_{ON}$ can be calculated as shown in (1). From this equation, it could be noted that $R_{ON}$ is inversely proportional to the total width of the transistor.

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \quad (1)$$

On the other hand, total capacitance, $C_T$ is the equivalent capacitance of Figure 2 (b) and shown in equation (2). Insertion loss could be calculated theoretically where $\omega$ is the radian frequency, $Z_0$ is the characteristic impedance, $R_B$ is the substrate resistance associated with the transistor as shown in equation (3) [8].

$$C_T = C_{DB} + C_{SB} + \frac{(C_{GD} + C_{GS})C_{GB}}{C_{GD} + C_{GS} + C_{GB}} \quad (2)$$

$$IL = \frac{1}{|S_{21}|^2} = \frac{(R_{ON} + 2Z_0)^2 + \omega^2 C_T{}^2 \left[(R_{ON} + 2Z_0)R_B + (R_{ON} + Z_0)Z_0\right]^2}{(2Z_0)^2 \left(1 + \omega^2 C_T{}^2 R_B{}^2\right)} \quad (3)$$

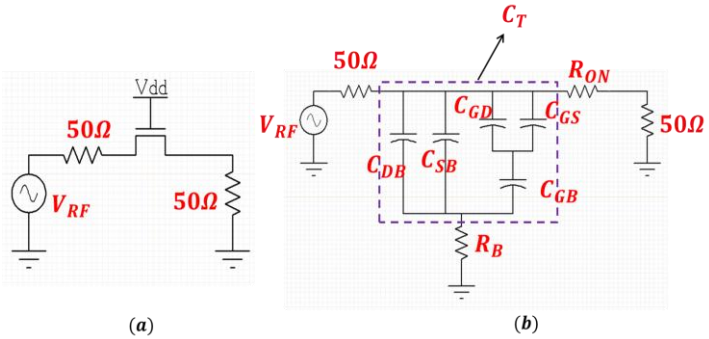


Fig. 2 (a) A single MOS transistor in 50Ω system (b) An approximate equivalent circuit [8]

### B. *Single Pole Single Throw Topology*

As shown Figure 3 below, an NMOS SPST switch design consists of two transistors $M_S$ and $M_P$ . Transistor $M_S$ will perform the main switching function while transistor $M_P$ is used to improve the isolation by grounding the RF signal when the switch is off [8]. In this design, the DC voltage on top of bypass capacitor $C_B$ is set to 0.5V and the same DC voltage is applied to $RF_{in}$ node. This to ensure that static power consumption is kept near zero when the switch is on [8]. According to Huang, n-channel MOSFET provides lower insertion loss per unit device area as compared to p-channel MOSFET's at high frequency. In this regard, since the operating frequency is in GHz range, NMOS is of interest for the CMOS SPST design. On the other hand, the presence of bias resistance, $R_{GS}$ and $R_{GP}$ is used for improving DC bias isolation [8] [9]. In this design, a typical value of bias resistance which is 10kΩ is utilized

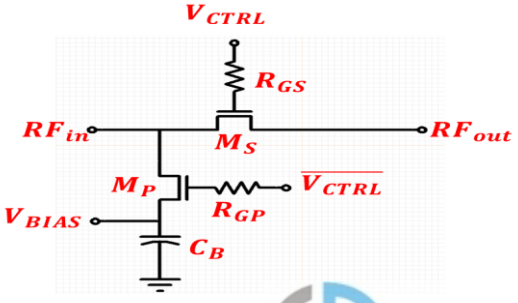


Fig.3: Circuit schematic of an NMOS SPST switch [8]

# IV. RF CMOS SPST Simulation

Critical switch parameters that affect its performance were verified in simulation. Pre and post layout simulation were done to clarify the effect of parasitic capacitance in this layout design. Figure 4 shows pre and post layout simulation for insertion loss of this RF-CMOS SPST switch with maximum frequency of 2GHz. The difference of pre and post simulation is relatively small considering the effect of parasitic capacitance in the layout design. In contrast, pre and post simulation for isolation is shown in Figure 5. Isolation of more than 20dB is obtained for operating frequencies up to 2GHz at $V_{CTRL}$=3.3V while $\overline{V_{CTRL}}$ = 0V and drain/source-to-body reverse bias ($V_{DB}$/$V_{SB}$=0.5V). Furthermore, pre and post layout simulation for P1dB were done to check the switch performance in terms of power handling capacity as shown in Figure 6. The P1dB compression point is tested at maximum frequency of 2GHz since a very slight difference of pre and post layout simulation is observed at 850MHz and 1.125GHz range. The summary of these parameters is shown in Table 1 to compare this design with the previous work done by others.

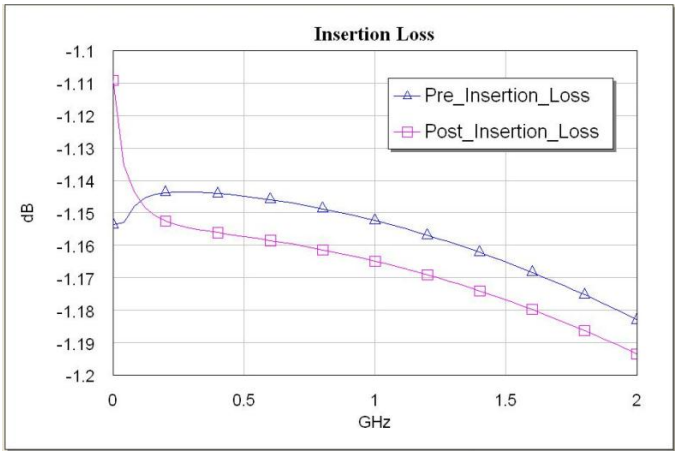


Fig. 4: Pre and post layout of RF-CMOS SPST switch for insertion loss

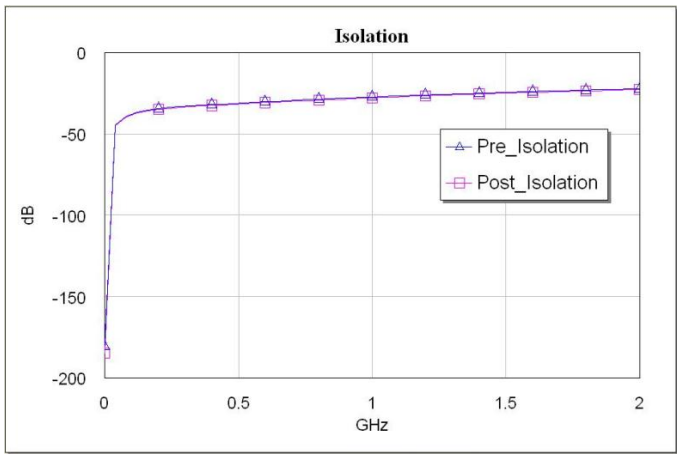


Fig. 5: Pre and post layout of RF-CMOS SPST switch for isolation

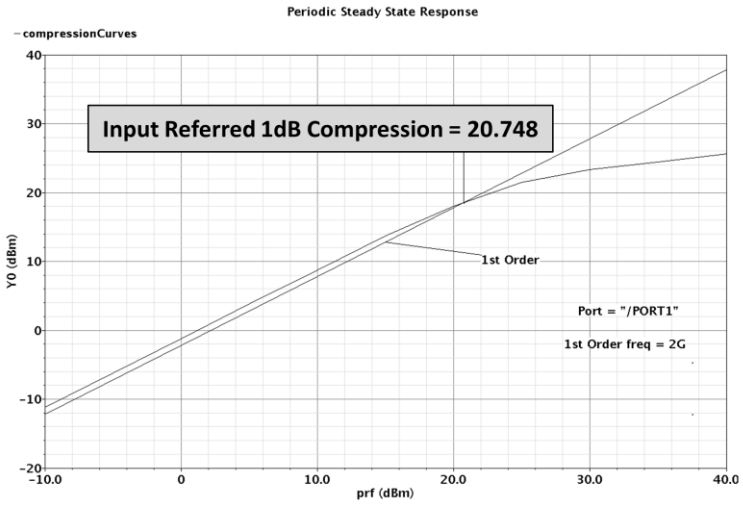


Fig. 6(a): Pre layout of RF-CMOS SPST switch for P1dB compression

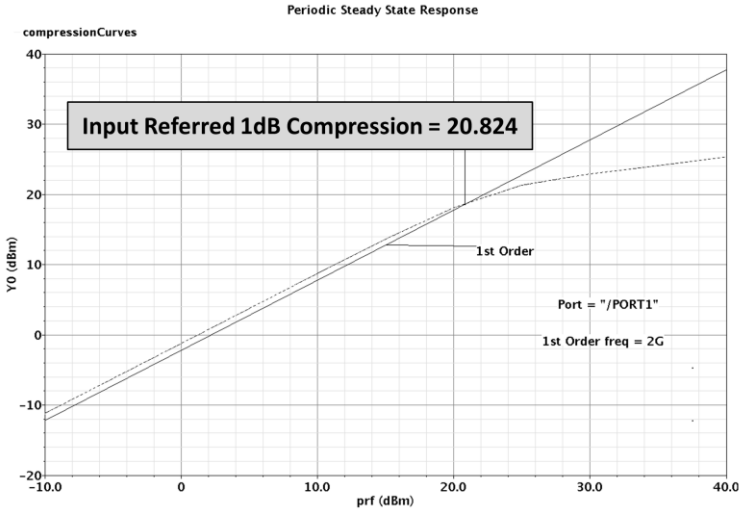


Fig. 6(b): Post layout of RF-CMOS SPST switch for P1dB compression

# V. Discussion

The control voltage, $V_{CTRL}$ and $\overline{V_{CTRL}}$ as shown in Figure 3 is set to 3.3V and 0V respectively. Instead of having pad for $\overline{V_{CTRL}}$ , $V_{DD}$ pad is placed to provide supply voltage for the inverter used in this design. The inverter is used to provide alternating control voltage during on and off state of the RF-CMOS SPST switch. Key figures of merit of a T/R switch such as insertion loss, isolation and power handling capability measured by power 1-dB compression point (P1dB) could be optimized by considering certain aspects of the CMOS switch itself. One of the factors that affect the insertion loss of the switch is the width of the transistors $M_S$ and $M_P$. When the transistor width is increased, the on resistance decreases causing the insertion loss to be decreased as well.

TABLE 1
PERFORMANCE OF CMOS SWITCHES

| Process | Frequency | Insertion Loss (dB) | Isolation(dB) | P1dB (dBm) | Chip Area |
|---|---|---|---|---|---|
| 0.18µm CMOS[9] | 900MHz | 0.94 | 35.2 | 30 | 0.15mm$^2$ |
| 0.35µm CMOS [10] | 928MHz | 0.46 | 39.5 | 17.7 | 531µm$^2$ |
| 0.25µm LDMOSFET [11] | 900MHz | 0.82 | 25 | 18 | NA |
| 0.18µm CMOS [12] | 900MHz | 3 | 40 | 13 | 0.67mm x 0.94mm |
| This work 0.35µm CMOS | 850MHz/1.125GHz | 1.15/1.155 | 28.31/22.25 | 20.68/20.70 | 618µm x 524µm |

Nonetheless, if the width of the transistor is increased drastically, the signal loss through capacitive coupling to the substrate is observed [8]. This will increase the insertion loss quite significantly especially in high frequency range. In this regard, the width of the transistors $M_S$ and $M_P$ is chosen to be 120µm to have minimum insertion loss at 850MHz and 1.125GHz. Furthermore, the body floating technique is applied to improve the power performance of the CMOS switch [13]. Using this technique, the body of the transistor is connected to the ground with 10kΩ resistor. The gate bias resistors $R_{GS}$, $R_{GP}$ and resistors used in body floating technique are implemented using n-diff resistors.

DC bias voltage condition as mentioned earlier in section III is important to improve the insertion loss and P1dB. RF node as well as sources of $M_S$ and $M_P$ are DC biased to 0.5V instead of 0V. This voltage reverse biases the source/drain-to-body junctions, lowering the capacitance and as a result improve the insertion loss [8]. As shown in Figure 7 below, a poly capacitor is used for the design of 20pF capacitor. Port 1 and 2 represent the TX and RX port in real RF front end. The chip area is 618µm x 524µm.

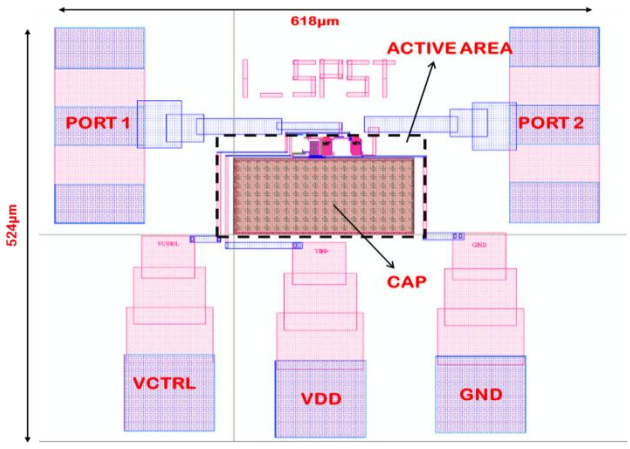


Fig. 7: RF-CMOS SPST layout

# VI. Conclusion

A RF-CMOS SPST switch has been presented in this paper. The full design of this switch is currently under development using a foundry 0.35µm CMOS process. Based on simulation, the switch exhibits 1.15-dB insertion loss in 850MHz and 1.155-dB in 1.125GHz. In addition, the isolation and P1dB of the switch is relatively good as compared to other reported work. On top of that, the switch is designed to be integrated with SAW resonators for reconfigurable RF front-end.

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