International Journal of Advances in Electronics Engineering – IJAEE
Volume 4 : Issue 1 *[ISSN 2278 – 215X]*
Publication Date : 09 January 2014

Designing of Graphene Nanoribbon based Static Random Access Memory

Abhishek Gune[1], Dr.Anu Gupta[2]

Electrical and Electronics Department, Birla Institute of Technology and Science
Pilani , India

***Abstract*— In the post silicon era as the silicon reaches its fundamental scaling limits graphene nanoribbons is expected to take over and thus continue the Moore's law about the diminishing size of transistors. Graphene nanoribbons facilitates high speed low power switching applications. Low and high field mobilities of the graphene nanoribbons are found to be higher than the CNTs and CMOS keeping the same unit cell. Such properties of graphene nanoribbons are used in the paper to define RAM memory using GNRs as an effective substitute to CMOS and CNTFETs cache memory. Graphene nanoribbon crossbars are used as the basic programmable devices. This 2-D arrangement of GNRs creates programmable diodes at intersection of each horizontal and vertical GNR rod thus opening up new avenues for building high speed memory and digital devices. The graphene nanoribbons based memory is better than the SRAM in terms of speed, density and performance metrics as well. GNR based memory would be operating in the 10 nanometres scale and would be 25-50 per cent denser than the existing SRAM. The GNR based volatile memory would be ternary in nature and thus would account for 3^x bits of memory for x number of programmable node in the graphene nanoribbon architecture. By using the cross bar technique even denser GNR based memory could be produced.**

Keywords*— *Graphene nanoribbon , graphene , carbon nanotubes , Green's function , Hamiltonian operator , lithography , SRAM , ternary memory , interconnects , routing channels .

I. INTRODUCTION

Graphene nanoribbons have generated immense interest for their electrical, physical and transport properties. It is also envisioned to be a potential alternative to silicon as MOS channel material beyond the existing Complementary metal oxide technology. Recent experiments have demonstrated that fabrication of single atom layer graphene sheets with remarkable electron transport properties is now possible. But grapheme is a zero-band gap material hence it cannot be used directly for semiconductor applications. Careful patterning of graphene laterally confined in ribbon like structure gives rise to Graphene Nanoribbons (GNRs). The lateral confinement of graphene to form graphene nanoribbons using lithography appears to be more easy and compatible than controlling the chirality of a carbon nanotube (CNT). Hence graphene nanoribbon(GNR) is expected to be a better alternative to silicon than carbon nanotubes (CNTs). Carbon nanotubes (CNTs) could be longitudinally degenerated using lithography to produce graphene nanoribbons. The paper proposes the use of graphene nanoribbon based memory as a better option than CNT based and the existing CMOS RAM. It also gives directions to harness the extra-ordinary properties of graphene and graphene nanoribbons in context of semi-conductor and in specific to its use as memory. Graphene nanoribbons are promising materials for memory interconnect applications as they can conduct current densities of magnitude larger than copper and aluminium wires. Hence GNR interconnects could be used in the existing CMOS memories as well. The paper studies the aspect of graphene nanoribbons to be used in the above context and benchmarks them against copper and aluminium wires. Graphene is a good electron transport medium as it offers very less hindrance to the electron flow. This has been explained in the paper using Green's function. The HSPICE simulations of the basic cells have been included in the paper. The atomistic and effective mass models have been used in the simulations. Graphene Nanoribbon applications would bring monumental changes to the volatile memory and digital electronics. It could be seen as the start of the nanoelectronics era of graphene nanoribbons.

II. GRAPHENE IN ELECTRONICS

Graphene is a zero band-gap semi-conductor with charge carriers behaving as massless Dirac fermions. Under charge neutrality conditions, the Fermi level is at the interception of the valence and conduction bands, but can be shifted with the application of a vertical electric field to create a majority of holes or electrons. A transition of the Hall coefficient from positive to negative values is then observed; Graphene exhibits very high carrier mobilities at room temperature due to a weak electron-phonon interaction; Electrons travel ballistically in graphene over long distance (of the order of one micrometer) which by far exceed the length of advanced FETs; Graphene can sustain current densities exceeding those of copper at comparable dimensions.

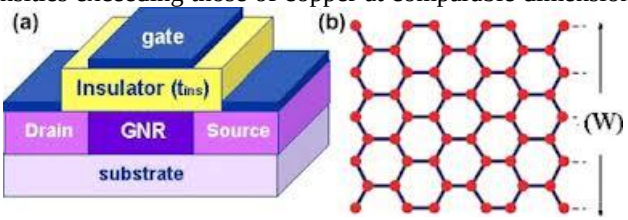

Fig 1. GNR FET [3]

If graphene is lithographically etched to form a narrow nanoribbon with a suitable orientation, an energy gap develops between the conduction and valence bands, the size of which is inversely proportional to the nanoribbon width. It is known as graphene nanoribbon(GNR). It is this shape and structure of nanoribbon that makes grapheme suitable for use

in electronics. It makes graphene potentially suitable for the fabrication of ultra-thin nanoribbon FETs with either single or double gate and low-resistance interconnects. One can expect a very good control of short channel effects due to the monoatomic layer thickness and an excellent switching speed due to the large carrier mobility and the long carrier mean-free path.

In order to investigate the potential of graphene nanoribbon FETs, we are going to study the results of three different simulation models: a nearest-neighbor orthogonal tight-binding (TB) model based on a single pz orbital [3]; (ii) a non-parabolic effective mass (NPEM) model [4] and, (iii) a constant effective-mass (CEM) model. Indicating with the orbital associated with the atom within the slab, the matrix element of the Hamiltonian :-we get the potential energy at the atom site. The transport problem is formulated within the non-equilibrium Green's function (NEGF) formalism [6]. The electrostatic potential is calculated by self-consistently solving the 3D Poisson equation. The box integration method is used on a discretization grid of prismatic elements with triangular base, matching the hexagonal graphene lattice. The electron and hole local charge is directly assigned to the box surrounding the atom.

SRAM Memory

We are using the CMOS 6-T SRAM in the present day technology. But it could be replaced by GNR-FET based 6-T SRAM. It would ensure 25-50 percent better performance due to the better electron transport capabilities of GNR and also on some other important memory metrics like noise margin, power dissipation, etc.

The noise margin curve is plotted by studying the behaviour of cross-coupled inverters.

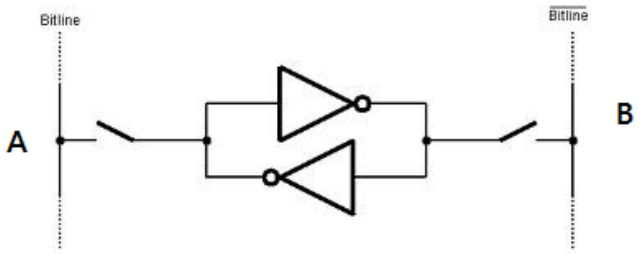

Fig 2 :- Cross coupled GNR-FET inverters

The noise margin is measured by plotting the butterfly curves. The butterfly curves were plotted [fig.3] for GNR-FET cross coupled inverter [fig.2]. It consists of two curves. First you apply input at A and plot the output at B to get the first curve. Then you apply input at B and plot the output at A to get the second curve. Superimposing these two curves gives you the butterfly curve. The length of the biggest square that can fit into the Fig.3 is the noise margin in volts. The noise margin for the CMOS SRAMs that we use presently ranges in 0.9-1.1 volts [3]. While for GNR-FET SRAM it comes out to be around 1.2-1.4 volts [fig.3] which is about 0.2 volts higher with respect to both the lower and the upper limits.

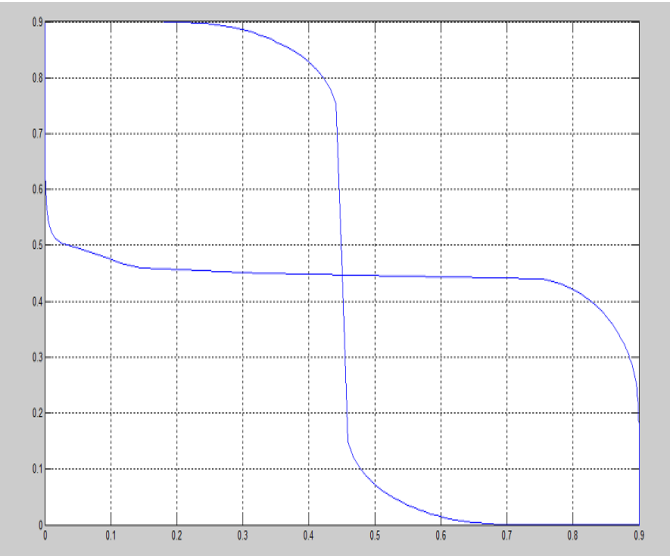

FIG 3 :- BUTTERFLY CURVE INDICATING NOISE MARGIN OF GNR FET CROSS COUPLED INVERTER

Comparison with CNTFETS :-

The CNTFETs have been researched as one of the upcoming technology along with GNRs that has the potential to replace the current CMOS technology as silicon approaches its fundamental scaling limits in the coming years. But it could be well be constituted that GNRs fare better on most of the memory metrics like power dissipation, noise margins, etc.

Even in analog applications GNR-FETs would serve as a better option than the CNTs which is demonstrated in the fig 4.It could be seen that the GNR-FETs reach saturation early and also have saturation currents lower than that of the CNTs.

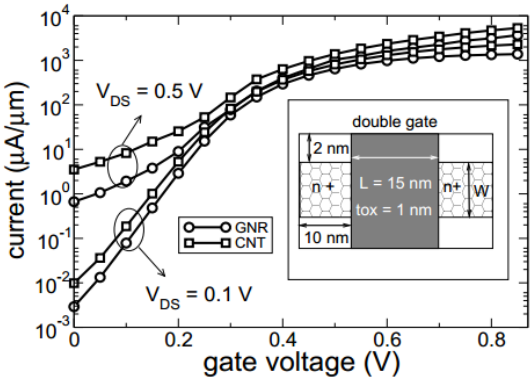

Fig 4 :- Dependence of current on Gate voltage for GNR in comparison to CNTFET[1]

Other than the use of GNRs in FETs for making the SRAMs, GNRs could also be used for the memory interconnect applications. Presently the interconnects of

copper and aluminium are used dominantly. GNRs could be used as a replacement for them in order to have better performance as it offers almost negligible resistance to the flow of electrons and thus better conductivities than copper and aluminium. Thus the study of graphene and GNRs to be used as interconnects could be a further extension of this paper.

Conclusion :-

Graphene Nanoribbon applications would bring monumental changes to the volatile memory and digital electronics. It could be seen as the start of the nanoelectronics era of graphene nanoribbons. The memories will now be consuming significantly less power (25-50 percent) coupled with relatively more noise margins as compared to the existing CMOS technology.The comparative study shows that the GNR-FETs have more potential to replace the silicon era than the CNTs. GNR and graphene also display promising aspects as far as their use for interconnect material is concerned.

---

* 1Abhishek Gune is pursuing B.E (Hons.) in Electrical & Electronics Engineering at BITS-Pilani,(phone:091-7891400298; e-mail: f2010034@pilani.bits-pilani.ac.in).

*2 Dr. Anu Gupta, Head of Department , Electrical and Electronics Department , Birla Institute of Technology and Science- Pilani.(email: anug@pilani.bits-pilani.ac.in).

ACKNOWLEDGEMENTS

The authors would like to thank the faculty of the Electrical and Electronics Department, BITS-PILANI for their fruitful inputs and insightful discussions.

REFERENCES

[1] Y. B. Zhang, Y. W. Tan, H. L. Stormer, and P. Kim, “Experimental observation of the quantum Hall effect and Berry’s phase in graphene,”Nature, vol. 438, no. 7065, pp. 201–204, Nov. 2005.

[2] K. Nakada, M. Fujita, G. Dresselhaus, and M. S. Dresselhaus, “Edge state in graphene ribbons: Nanometer size effect and edge shape dependence,” Phys. Rev. B, Condens. Matter, vol. 54, no. 24, pp. 17954–17961, Dec. 1996J. Breckling, Ed., *The Analysis of Directional Time Series: Applications to Wind Speed and Direction*, ser. Lecture Notes in Statistics. Berlin, Germany: Springer, 1989, vol. 61.

[3] A. Wang and A. Chandrakasan, “A 180mV FFT Processor Using Sub-threshold Circuit Techniques,” *ISSCC*, 2004 .

[4] A. Bhavnagarwala, D. Tang, and J. D. Meindl, "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability," JSSC, Vol. 36, No. 4, April 2001.

[5] B. Cheng, S. Roy, and A. Asenov, "The Impact of Random Doping Effects on CMOS SRAM Cell," ESSCIRC, 2004.

[6] M.P. Lopez Sancho et aI., J. Phys. F, vol. 15, p. 851, 1985

[7] G. Liang, N. Neophytou, D. E. Nikonov, and M. S. Lundstrom, “Performance projections for ballistic graphene nanoribbon field-effect transistors,” IEEE Trans. Electron Devices, vol. 54, no. 4, pp. 677–682, Apr. 2007.

[8] [8] S. Reich, J. Maultzsch, C. Thomsen, and P. Ordejon, “Tight-binding description of graphene,” Phys. Rev. B, Condens. Matter, vol. 66, no. 3, p. 035 412, Jul. 2002.

[9] M. Y. Han, B. Özyilmaz, Y. Zhang, and P. Kim, “Energy Band Gap Engineering of Graphene Nanoribbons,” Phys. Rev. Lett. , vol. 98, May 2007.