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Approaches to Design of Embedded Function-Oriented Microcontrollers: Architectural Solutions and Tools

A.E. Vassiliev
National Research University,
St. Petersburg State Polytechnical University,
Russia, St.Petersburg
avasil@aivt.ftk.spbstu.ru

D. Cabezas
diefercabezas@gmail.com

A.V. Dontsova
dontsova23@mail.ru

***Abstract*—the article describes hardware-software instrumentation for design and research of function-oriented controllers.**

***Keywords*—function-oriented controllers; embedded system; computer-aided design; programmable logic device**

I. Introduction

Nowadays function-oriented controllers (or function-oriented processors) are getting more important in practice of built-in embedded control systems realization. Function-oriented processors (controllers) (further – FOP, FOC) represent the specialized computations and control platforms containing architectural, algorithmic, circuitry and other concepts, directed on effective (in terms of minimization of labor costs of the target task developer, time of algorithm performance, memory expenses, etc.) solution of rather narrow (special) class of control tasks. Despite the long history of these terms, active interest to this area has been shown only in recent years. Firstly, thanks to new technological capabilities of microcircuitry design and production of chips with high integration extent.

Development relevance of this perspective is caused by a number of factors (including economic), in aggregate bringing to the needs of usage of the most optimized (in the meanings stated above) decisions in many technical applications, thus the functional variety of general purpose microcontrollers is often excessive and defiant the additional expenses not justified by real requirements (cost, operational and so forth), and program realization of special algorithms on such microcontrollers is inadmissible expensive from the point of view of the optimal criteria stated above.

Typical applications, in which the usage of FOP and FOC is expedient and demanded, include different onboard control systems, the autonomous communication systems, the distributed systems of data collection, personal communicators, etc.

Development of systems that belong to the mentioned class is characterized by growth of requirements to their reliability and to the accuracy of computations, growth of algorithms complexity, increase in number of various sensors and executive mechanisms, toughening of requirements to frequency characteristics, mass and dimensions parameters and power consumption.

Thus, it is desirable to have special, the most suitable microcontroller for each group of tasks (from their rather various circle).

II. Classification and examples of FOC realization

Several special applications mentioned above require function-oriented microcontrollers that are produced in some countries (as well as in Russia). Despite the variety of tasks in which FOC application is expedient FOC can be united in groups by using various criteria. In particular, criterion of the main direction of their specialization can be used (fig. 1). Let us review the characteristic examples of FOC development, ones representing scientific and practical interest, and ones that

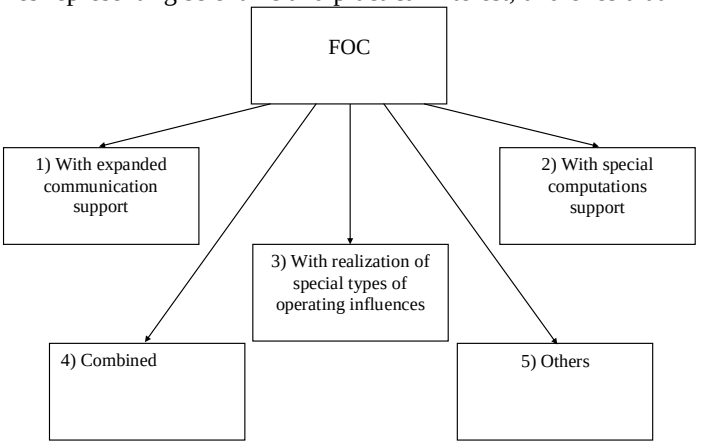

Fig. 1. Version of FOC classification

are successful in commercial sense – serially released products with a steady sales market.

The typical representative of the first classification branch is the FOC-microcontroller ATA5505 produced by firm Atmel [1], it contains built-in block of the RFID interface providing wireless radio-frequency data exchange with identification tags built into objects (RFID tags, or transponder) that is widely applied in systems of the warehouse account, conveyor production, systems of identification, access control, etc.

FOC ATA5505 has the QFN case of 5mm x 7mm size, it works in the low-frequency range of radio signals (100 KHz – 150 KHz) and is compatible to all existing standards of reading and programming of RFID tags with amplitude manipulation that allows to develop the systems for identification schemes with use of the minimum quantity of external components, thereby providing possible reduction of cost and terms of a new product development, and also providing its best reliability indicators and mass and dimensions parameters (fig. 2).

FOC ATA5505 has 512 bytes of static memory, 512 bytes

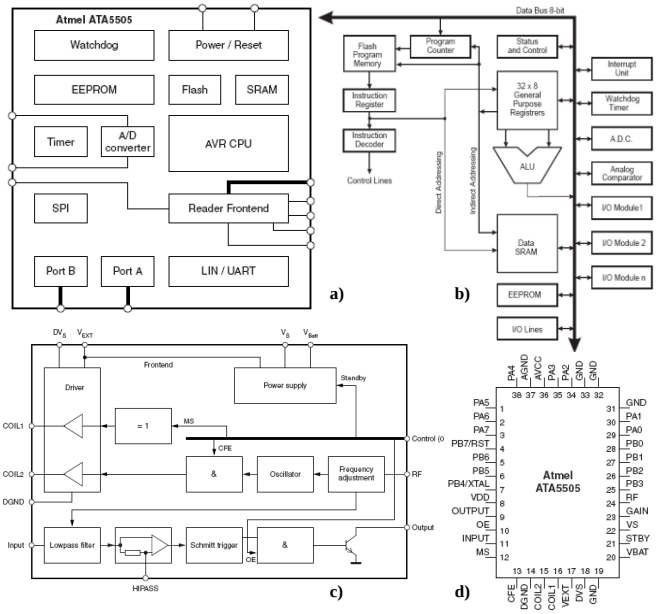

Fig. 2. Structure (a), kernel (b), RFID block (c) and assignments (d) of FOC ATA5505.

of EEPROM, 16 general purpose input-outputs, 32 general purpose registers, the 8-digit timer-counter with the comparison scheme, the 16-digit timer-counter with capture and comparison schemes, the universal serial interface, interrupt controller (internal and external sources), 11-channel 10-digit ADC, the programmable watchdog timer with the built-in generator and three programmatically adjusted power consumption modes. At the expense of execution of enough difficult instructions for one cycle, the microcontroller allows to reach performance of 1MIPS on MHz with possibility of power consumption control and calculations speed setup.

The representative of the second classification branch is the microcontroller MDR8F3 by firm Milandr (Zelenograd, Russia) [2] (fig. 3).

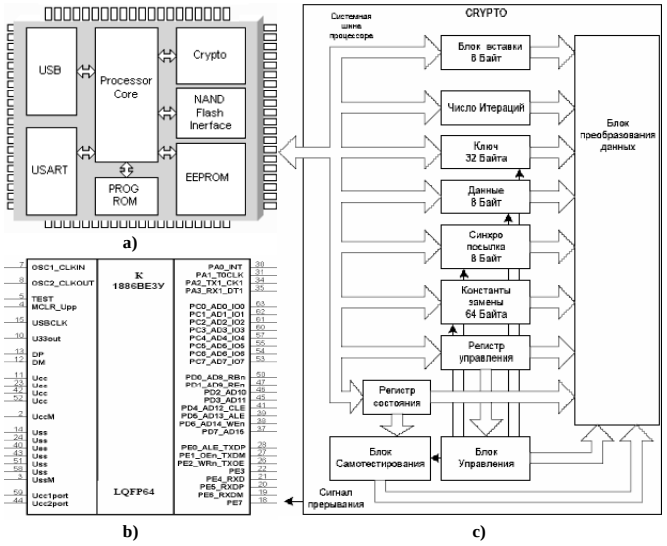

Fig. 3. Structure (a), assignments (b) and block of cryptographic information security (c) of MDR8F3.

This microcontroller contains the hardware block of cryptographic information security in accordance with Russian Federal standard 28147-89, the 16-digit timer-counter, communication USB and USART ports, 28 lines of input-output ports, built-in program memory of 32 K x 16 bytes, built-in data memory with a capacity of 902 bytes, the 4-vector interrupt controller, the watchdog timer. FOC is compatible to MCU PIC17 on instructions system and has the LQFP64 case.

The third classification branch of FOC is represented by the microcontrollers 1867BC5T [3] (fig. 4) released by research institute of electronic equipment of NIIET (Voronezh, Russia) and intended for systems of a digital control of electric motors.

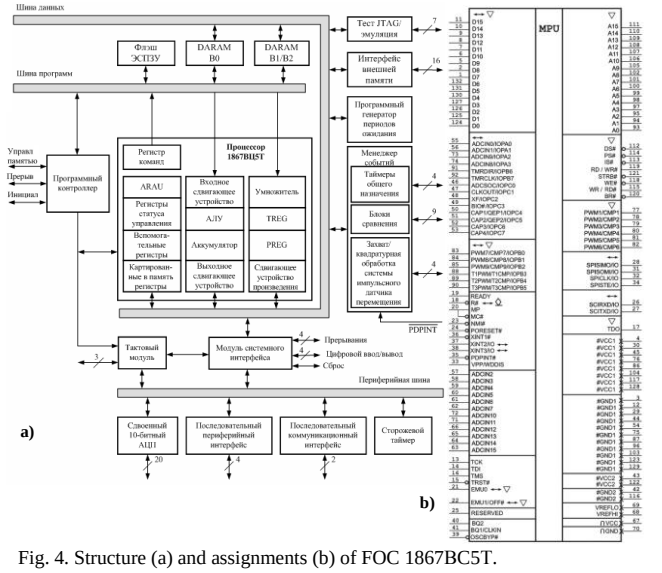

Fig. 4. Structure (a) and assignments (b) of FOC 1867BC5T.

The microcontroller 1867BC5T contains 16-digit digital signal processor, compatible to architecture of the processor 1867BM2, built-in flash memory of programs, event manager block, and also a number of serial interfaces (SCI and SPI).

The structure of the events manager includes the 12-channel PWM block, three timers, 6 blocks of comparison, 4 blocks of capture. The structure of FOC also includes two independent 10-digit 8-channel ADC that allows developing various control systems of the electric drive with significantly smaller labor costs, than at traditional approach to development – for example, to realize system of fluctuations damping in mechanical part of the drive, synchronization of shaft rotation, etc.

The diverse structure of the fourth group of combined FOC is characterized by family of the ZW0x0y [4] microcontrollers (fig. 5) produced by Zensys firm, having MCS51-compatible architecture and intended for development of the distributed measurement and control systems, on the basis of local wireless self-organizing radio-frequency communication networks of the Z-Wave standard.

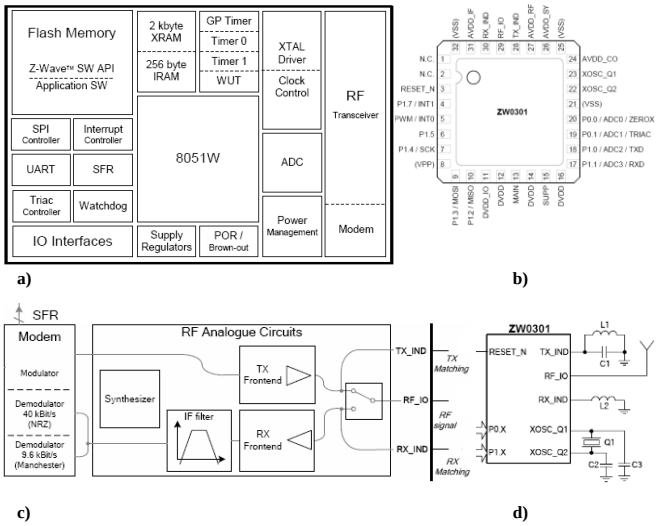

Fig. 5. Structure (a), assignment (b), radio channel block (c), Switching scheme (d) FOC ZW0301.

These FOCs have different specialized communication opportunities (a special radio channel), and also built-in library of applied programs (API) for service of difficult subscribers interaction protocols in self-organizing networks.

For example, FOC ZW0301 has 32 Kb of Flash-memory and 2 Kb of the static RAM, the PPM controller (for realization of thyristor management), 4-channel 12-digit ADC, PWM controller, the SPI and UART transceivers, three 16-bit timers, watchdog timer, 10 lines of input-output, and also the radio channel block with the original protocol of the exchange, allowing to develop the distributed applications with self-organizing structure. FOC is issued in the 32-output QFN case with 5mm x 5mm size.

The i.MX515 microcontroller produced by Freescale [5] with an ARM Cortex A8 kernel that contains the built-in coprocessor for hardware processing of images (scaling, imposing, rotation, etc.), and also has a P-ATA interface for direct work with external stores belongs to the fourth classification group.

The fifth FOC classification group contains alternatives to FOCs with the fixed hardware architecture – known as System on Chip, Programmable System on Chip (SoC, PSoC) – containing unit of the microcontroller and unit of the programmable logic device (PLD) in the case of one integrated chip.

Functioning of a such FOC microcontroller kernel of such FOC with variable structure is defined by the program written down in its memory, and PLD functioning – by a written down in its memory configuration of its elements hardware connections. Thereby the developer is given an opportunity to create and describe not only program, but also hardware set elements of information transformation.

The PSoC family by Cypress [6] can be an example of such FOC. This family includes PSoC with microcontrollers with popular architecture such as MCS-51 (fig. 6) and ARM.

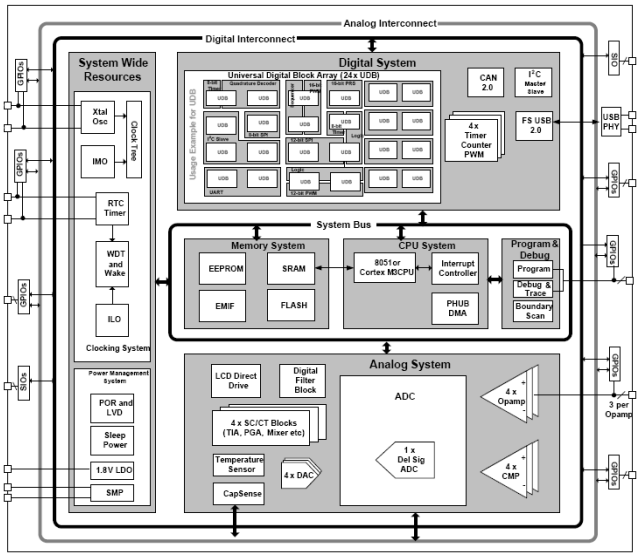

Fig. 6. Structure of FOC PSoC CY8C38.

Microcontrollers produced by EnergyMicro of Gecko family belong to the same fifth group, in particular, EFM32G210F128-QFN32 [7] developed for application in systems with extremely rigid restrictions on a components power consumption. So, specified FOC in a mode of the maximum functionality consumes current 150 μA/MHz, and in a sleep mode (change of a condition of input contacts) its current power consumption is 20 nA.

III. Problem definition

Despite the variety of FOC designed to satisfy of various conditions, shown to a developed microcontroller system, the problem of creation and use FOC cannot be guaranteed within existing approaches; due to the following circumstances:

- in the majority of FOC, cardinal optimization is performed by one criteria, so the problem of searching for FOC with several requirement (relating to classification group 4 in fig. 1), can be resolved only partially and therefore is non-optimal (for example, by a choice of obviously excess FOC), or at all insoluble that complicates process of a concrete new product development;

- the team of the developers who systematically use FOC in the development usually faces a migration problem between various FOC classes for the next development that leads to a dilemma: to use well-known to the developer, but obviously excessed FOC (i.e. to the non-optimal solution of a development problem), or to use professional hardware and software development of a new FOC that is in most cases fraught with increase in development duration, and in some cases – insufficient level of its quality.

Approach that favors a usage of FOC architectural concepts with PSoC, despite obvious advantages, has also a number of shortcomings:

- architectural opportunities of PLD applied in such FOC as a rule do not allow to realize difficult structures of data processing necessary, in particular, for the solution of problems concerned with hardware support of specific computations (the second classification group on fig. 1);
- problem of the developer's migration between the FOC models for the next development remains.

Due to the circumstances noted above, in authors' opinion, other approach to FOC development consisting in granting to the target built-in application developer of tools of various FOC creation is expedient.

Thereby the contradiction between existing idea of MCU (including FOC) as about computing systems, whose functional flexibility is provided only by a change of a program component at invariable architecture of hardware – on the one hand, and requirement to change this architecture depending on a solved task – on the other hand is overcome. The tool, allowing to create the most corresponding to a problem architecture of the FOC hardware platform has to be provided in the order of the developer then the necessary software for this platform has to be developed.

Thus, let us talk about creation of the specialized tool decisions providing support of the research and initial stages of developmental works in the field of the equipment and the function-oriented controllers' software design.

IV. Proposed architectural solutions for tools

The main idea of a tool complex creation is based on use of expanded parameterized libraries of the kernel description and FOC peripherals for programmable logic devices (PLD). With application of means of computer-aided design (CAD) for PLD developer, proceeding from requirements to architecture of created FOC, chooses the existing modules which are stored in library of ready decisions, creates new modules (if necessary filling up with them this library) and unites the existing and new modules for obtaining the description of new FOC. After debugging, translation of this description in a machine form and its loading into memory of PLD, the chip starts carrying out functions of hardware for developed FOC.

Further, using CAD tools for development of the software for FOC, the developer designs, debugs, translates into a machine form and loads the applied program into FOC's memory.

Authors offer the following structure of FOC's design tool complex (fig. 7):

- the PLD's CAD tools, allowing to develop and configure FOC hardware platform;
- expandable library of standard hardware components for FOC equipment;
- the CAD tools for FOC software;
- expandable library of standard program modules for FOC;
- the debugging board (allowing to carry out prototyping both realistic FOC modeling) including in the structure (at least) PLD configuration load facilities (the JTAG interface and memory of a configuration), FOC software load facilities, VLSI chip of PLD (carrying out after configuration FOC function) and interface devices for the interaction with objects;
- instrumentations and simulators of object of control for implementation of realistic modeling of FOC work.

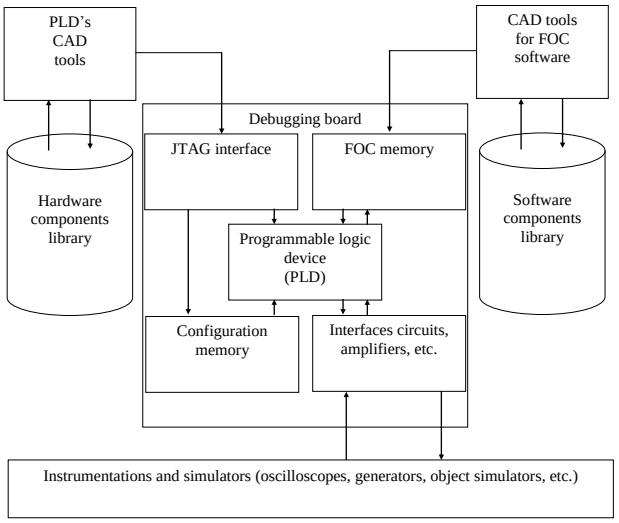

Рис. 7. FOC's design tool complex.

The using of offered structure would mean in, at a FOC architecture design stage the developer carries out the following actions:

- choice of a kernel of the microcontroller;
- definition of the nomenclature of the FOC's standard peripherals (library);
- definition of the FOC non-standard (specialized) units;
- interconnection of MCU kernel and FOC standard units;
- development and debugging of the FOC non-standard units;

- general FOC equipments interconnection, translation of description into a machine code and loading into PLD's memory of configuration.

At FOC software design stage the developer carries out the following actions:

- definition of the nomenclature of program modules;
- allocation and interconnection of standard (library) program modules;
- development and debugging of the FOC non-standard program modules;
- general interconnection of the FOC software, translation of description into a machine code and loading into FOC memory.

At a stage of complex debugging of hardware-software system the control and measuring equipment and imitating means is applied.

v. Example of the tools complex realization

As an example of tools CAD for FOC constructed with application of specified approaches, we will consider the FOX-51 complex developed by authors (fig. 8). The complex has the following distinctive features:

- used package of CAD for PLD – Quartus II (fig. 8, a);
- CAD package for MCU – Shell51 (fig. 8, b);
- PLD chip applied as a part of a debugging board– Cyclone III (fig. 8, c);
- microcontroller kernel of FOC – MCU-51 (development of the Californian university).

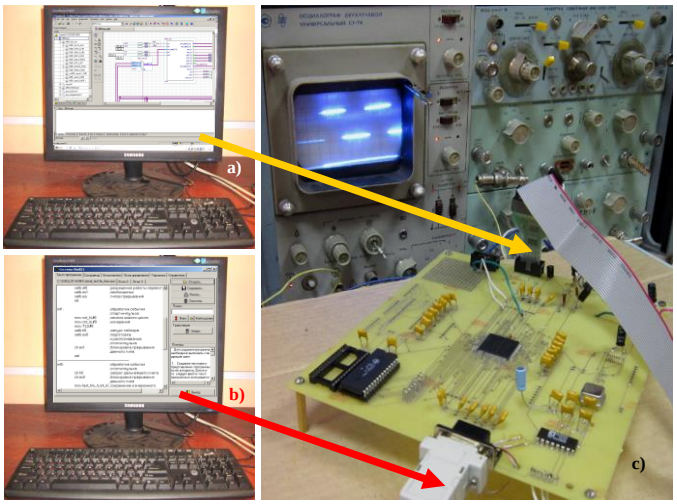

Fig. 8. Example of CAD tools for FOC: loading of FOC configuration (a), program loading (b), hardware debugging (c).

With usage of the FOX-51 in the experimental purposes the MCS-51-compatible FOC of the 4th classification group containing in the structure unit of PWM-signals hardware generation and a unit of alphanumeric LCD service (fig. 9) is developed. For definition of extent of decrease in development resource intensity and extent of increase of their accuracy with usage of offered expansions a number of the experiments consisting in realization of the PWM functions and an output on LCD both standard means of MCU, and with use of the developed FOC non-standard units is carried out.

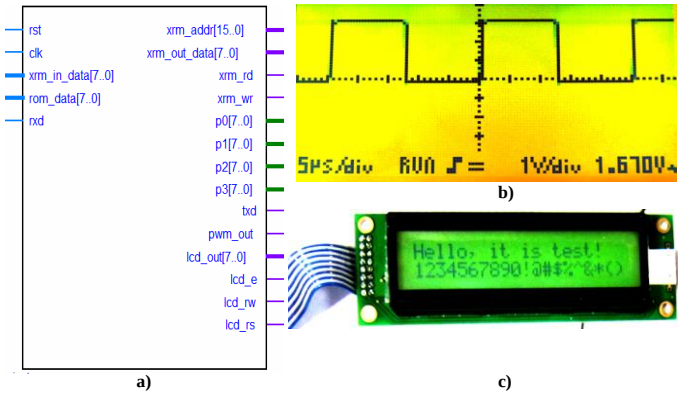

Fig. 9. Scheme (a), PWM generation (b) and interaction with LCD (c) of FOC.

So, fig. 10 shows the version of the scheme the PWM-signals program of generation accepting through the UART interface a two-byte code of the PWM-signal period and a single-byte code of pulse duration coefficient, and MCU using for PWM generation only the standard resources – two timers-counters and the line of input-output port.

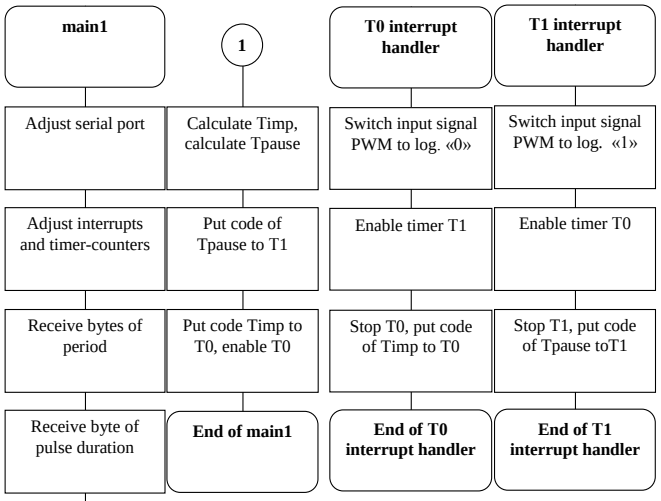

Fig. 10. System of PWM-signal generation: the standard software solution.

Realization of similar PWM-signal generation system with usage of the FOC non-standard unit is given in fig. 11 – the PWM hardware module (fig. 11, a, c). The FOC program (fig. 11, d) sets accepted through UART parameters by means of adjusting registers (fig. 11, b). Almost fivefold economy of the FOC program memory size and release of such critically significant resources, as timers-counters is thus reached. Precision characteristics of two versions of realization are given in fig. 12. It is visible, that pulse duration provided by hardware realization is more accurate compared with software

version. Besides, hardware realization allows keeping the PWM-signal period practically without errors on all range of pulse duration values.

Conclusion

At this stage of work the hardware-software CAD tools for design and research of function-oriented controllers is created, the demonstrational version of FOC with peripherals is developed; a number of experimental probes is carried out.

Openness and modularism of complex structure allow to make further experiments on development and use of new FOC, and also to make changes in complex structure.

The CAD FOX-51 allows projecting and analyzing a wide range of control algorithms, and is suitable for application in scientific experiments and educational and methodical work.

Additional information on IECS (Intelligent Embedded Control Systems) laboratory and activity of its collective is available in a network: http://aivt.ftk.spbstu.ru/education/labs/intelsys/ and http://www.famous-scientists.ru/12041. It is possible to contact authors via e-mail: avasil@aivt.ftk.spbstu.ru.

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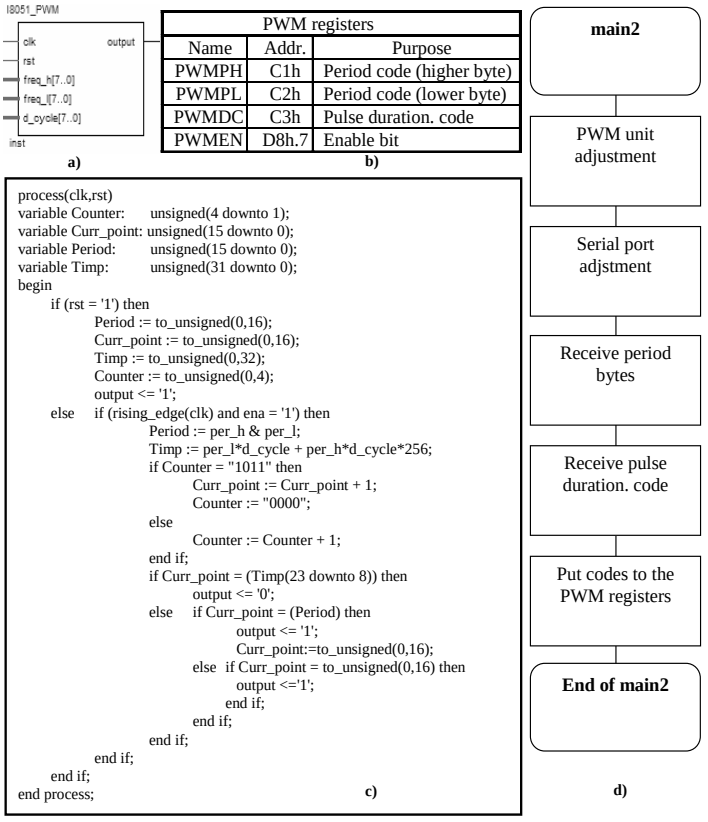

Fig. 11. System of PWM-signal generation: PWM unit (a), SFR of the unit (b), VHDL-description of the unit (c), usage of the unit in the program (d).

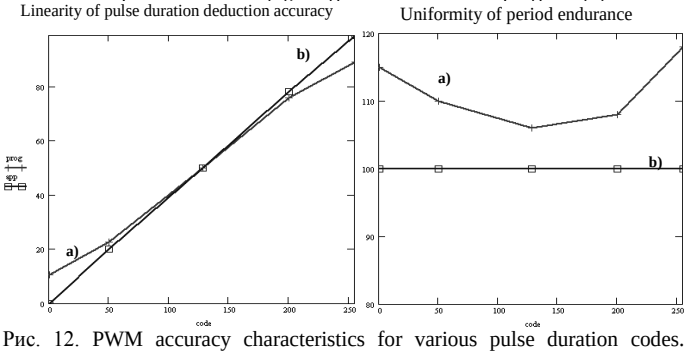

Рис. 12. PWM accuracy characteristics for various pulse duration codes. Tpwm=100 μs. Standard realization (a), realization with the usage of PWM unit (b).