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Impact of Radiation on MOSFET in Nano Regime

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***Abstract*. This paper present new simulation results on the effects produced by heavy-ion strikes on minimum-size (channel-length less than 32nm) MOSFET. The radiation-induced degradation of semiconductor device electrical parameters are reviewed. These results are related to the degradation of semiconductor-device performance on the variation of oxide thickness. Emphasis is placed on the effects of heavy-ion impact on MOS structures. The present degree of understanding of radiation effects in silicon devices is summarized.**

Keywords— heavy-ion, MOS, radiation effect, TCAD simulation

I. Introduction

When high-energy radiation is incident on a semiconductor device, energy is deposited in the semiconductor via two mechanisms; electronic ionization and atomic collisions [1]. The occurrence of these two mechanisms in a semiconductor structure depends both on the nature of radiation and the type of devices. For the exposure of heavy-ion on semiconductors, most of the deposited energy goes into ionization processes, i.e., excitation and then pair generation. The radiation-produced charges in a device mainly concentrate in insulator layer and semiconductor-insulator interface; name to trapped charges. In a MOS transistor the dominant effect of the trapped-oxide charge is to produce momentarily shifts in the I_{DS}-V_{GS} characteristics for the device, by altering the device threshold voltage. For both type of MOS devices there is negative shift in threshold voltage [2].

Moreover, with the technology scaling of standard CMOS process, the performance related to Total Ionizing Dose (TID) effects are naturally being improved due to the thinner gate/isolation oxides of new technologies, which reduces the charge trapping induced by ionizing radiation [3-6].

For radiation-hardened microelectronics, Moore's law tells us that we should fundamentally expect a technology gap to exist between state-of-the-art high-volume commercial microelectronics and radiation-hardened microelectronics that require specialized processing techniques and are produced in very small volumes by commercial standards. While the commercial marketplace has inserted 45-nm technologies into products today, the most advanced radiation-hardened integrated circuits on the market based on custom processes are at the 150-nm level, at least three technology generations behind [6].

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II. Overview

Figure 1, shows a simple schematic of a MOSFET, In this case an n-channel device using a p-type Si substrate. When a bias potential is applied to the gate contact, there will be an electric field across the gate oxide region and into the Si surface region immediately below the gate region. If the gate bias is sufficiently large and positive (for n-channel operation), the majority carriers (holes in p-type Si) will be repelled from or depleted in this surface region, and minority carriers (electrons) will be attracted to this region, forming what is called an inversion layer. If now also a potential difference is applied between the source and drain contacts (n+ doped region in fig. 1), the inversion layer provides a low-resistance current channel for electrons to flow from the sour9ce to the drain. The device is then said to be turned on [Fig. 1 (a)], and the control gate bias potential at which channel just begins to conduct appreciable current is called the turned-on voltage or threshold voltage of the device.

The total-dose ionization problem that occurs in this structure is then due to the radiation-induced charging (normally positive) of the thin gate oxide region, which generates additional space-charge fields at the Si surface. These additional induced fields result in voltage offsets or shifts in the turn on voltages of the devices, which lead to circuit degradation and failure. For example, for sufficiently large amounts of trapped positive charge for the device schematically shown in figure 1, the may be turned on even for zero applied gate bias [Fig. 1 (b)]. In this case, the device is said to have failed by "going depletion mode" [7].

As already mentioned several times, the part of an MOS structure most sensitive to ionizing radiation is the oxide insulating layer (SiO_2), which in present-day devices is generally less than 1 nm thick. When the radiation passes through the oxide, the energy deposited creates electron/hole pairs. In SiO_2, the radiation-generated electrons are much more mobile than the holes, and they are swept out of the oxide (collected at the gate electrode) in times on the order of picoseconds. However, in that first picosecond or two, some fraction of the electrons and holes will recombine. This fraction depends greatly on the applied field and on the energy and type of the incident particle [8].

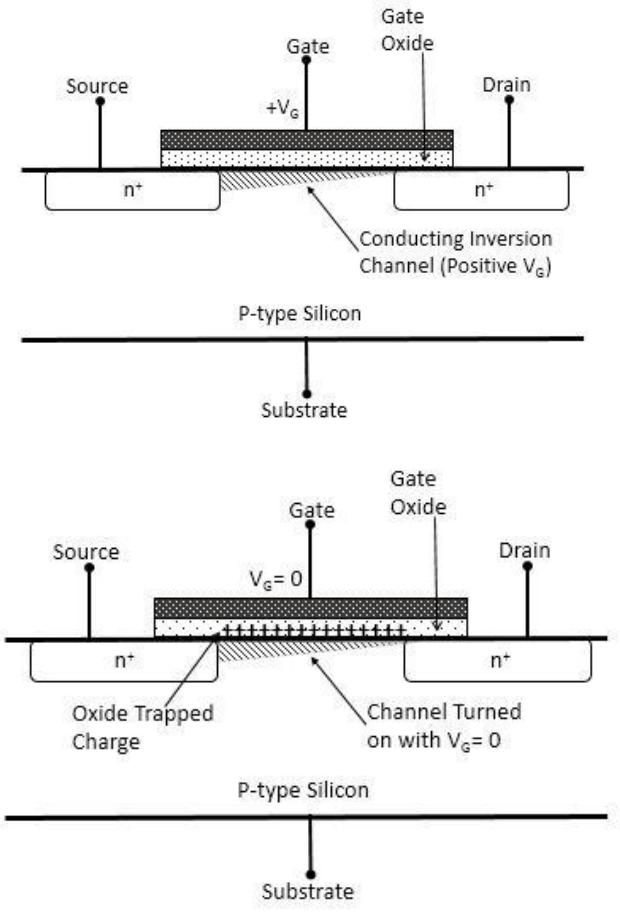

Fig. 1. Schematic of n-channel MOSFET Illustrating basic effect of total-dose-ionizatiton-induced charging of gate oxide: (a) normal operation and (b) post-irradiation.

The holes which escape Initial recombination are relatively immobile and remain behind near their points of generation, causing negative voltage shifts in the electrical characteristics of MOS devices, e.g., in threshold voltage (V_T) for MOS transistors (MOSFET's) or flat-band voltage (V_{fb}) for MOS capacitors. These initial processes of pair creation and prompt recombination-which determine the actual charge (hole) yield in the SiO_2 film and consequently the initial (maximum) voltage shift-constitute the first major factor of the MOS response.

III. Simulation Models

In this case, the ITRS 2008 road map will be followed. The following dimensions were chosen based on the ITRS; a gate length of 22nm, an effective oxide thickness of 3.5nm to 0.8nm (Si02), spacer width of 9nm, source/drain junction depth of 20nm, and a source/drain extension junction depth of 5nm. The doping levels of the drain/source doping are 1e+21 cm^{-3} (peak), 1e+18 cm^{-3} (junction) of Gaussian type, with a lateral diffusion factor of 0.8 [9].

Using a Silicon substrate, a 2-D MOSFET was modeled in Sentaurus TCAD. The structure's boundary and doping were defined using Sentaurus Structure Editor (SDE), a device modeling software. It was then meshed in SentaurusMesh (SNMESH) to create the appropriate files needed to properly simulate the device. Fig. 2 shows the meshed device and its doping concentrations.

With this meshed device, simulations have been performed on the device by running two SDevice (Sentaurus Device; a device simulator) command files. The first SDevice command

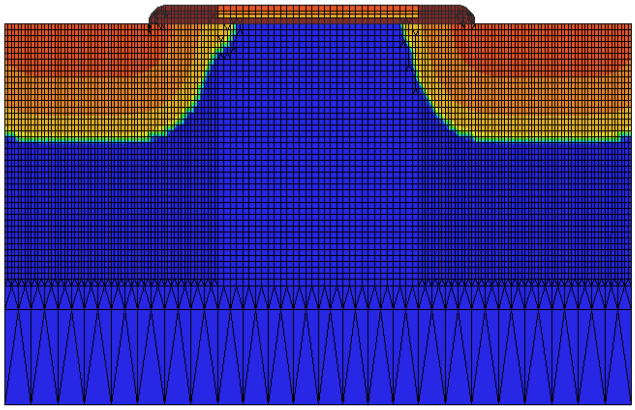

Fig. 2. Meshed view of minimum-size (approx. 22nm) MOSFET

file created Id vs Vgs curve without any introduction of radiation. The second SDevice command file created Id vs Vgs curve with the introduction of heavy-ions on the device. This introduction of heavy-ion is switched on with the command "HeavyIon" in the SDevice script [10]. These curves were then viewed in Inspect.

IV. Discussion of Results

Simulation of transfer characteristics have shown in Fig. 3. After irradiation the threshold voltage has shifted in negative by less than 10% from the pre-irradiated device [Fig 3(a)]. Simulations are performed on the nMOS structure with different oxide thickness ranging from 3.0nm to 0.8nm and corresponding results are enlisted in table 1. There is a large variation of threshold voltage in thicker oxide due to irradiation. While the oxide thickness further reduced the percentage change in device threshold voltage is diminish. These happens as the oxide thickness reduces as a result of scaling, the trapped charge densities in the dielectric remains very-very less and thus the Vth variation is very less in comparison to thicker oxide.

The The shift in the subthreshold region [Fig. 3 (c)] is between ±20mV. The subthreshold shifts in minimum-size devices are positive and negative, meaning that in some cases negative charge, while in some others positive charge builds up in the MOSFETs, because heavy-ion contain both type of charge particles.

TABLE I
THRESHOLD VOLTAGE VARIATION ON OXIDE THICKNESS

Oxide Thickness	Pre-irradiated Threshold Voltage	Post-irradiated Threshold Voltage	Percentage Variation
3.0 nm	0.823 V	0.746 V	9.35
2.4 nm	0.767 V	0.696 V	9.25
2.0 nm	0.712 V	0.648 V	8.98
1.8 nm	0.664 V	0.607 V	8.58
1.2 nm	0.415 V	0.382 V	7.95
1.0 nm	0.332 V	0.306 V	7.67
0.8 nm	0.220 V	0.204 V	7.27

Approx values are taken upto three decimal places.

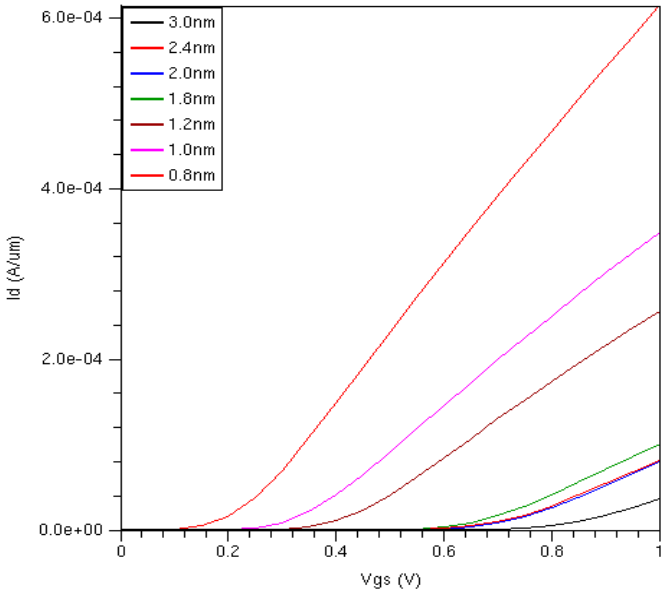

Fig. 3 (a). Transconductance (Id vs. Vgs) curve after irradiation. Legend indicates the oxide thickness.

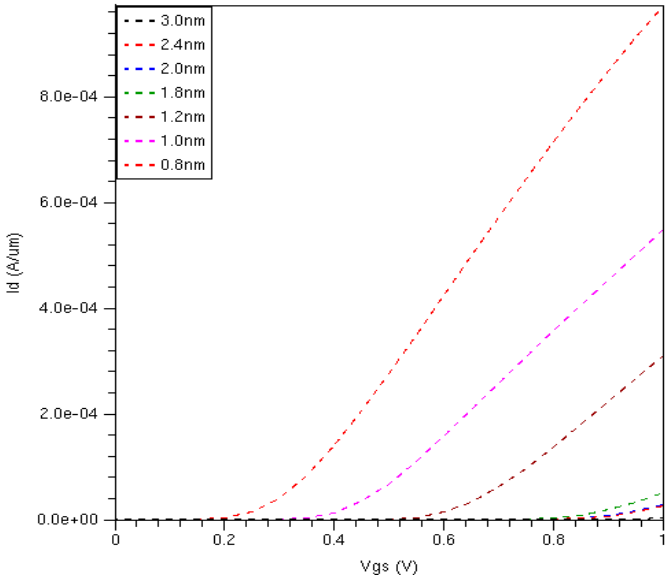

Fig. 3 (b). Transconductance (Id vs. Vgs) curve before irradiation. Legend indicates the oxide thickness.

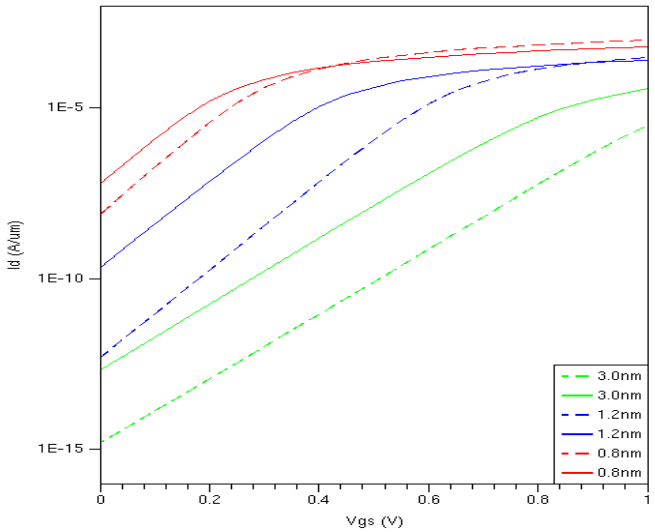

Fig. 3 (c). Subthreshold drain current. Solid curve shows the value after irradiation and dashed curve is for before irradiation. Legend indicates the oxide thickness.

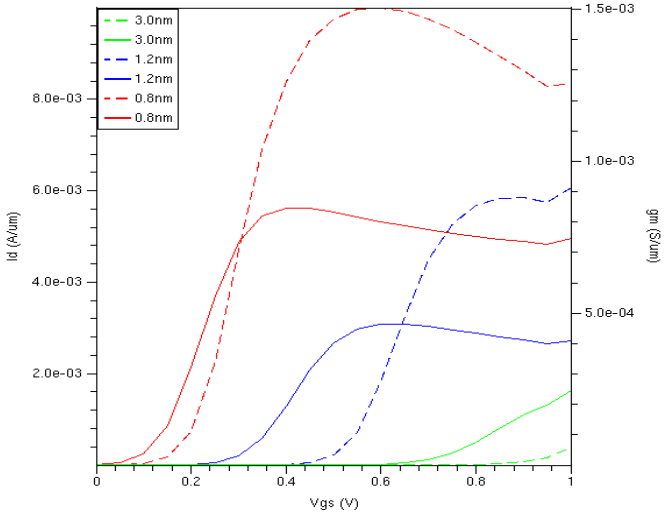

Fig. 3 (d). Transconductance (gm) variation after and before irradiation. Legend indicates the oxide thickness.

There is a drop in the maximum transconductance which can be as large as 10% [Fig. 3(d)] and a reduction in drain current. Furthermore, in case Fig. 3(b) the linear region shifts rightwards too (compare the dashed and solid line). Another interesting phenomenon have been observed after exposing some minimum-size MOSFETs to heavy ions is an increase in drain current accompanied by a reduction in the output resistance, i.e., the slope of the Id-Vds curve.

Finally, an increase in substrate leakage current is shown in Fig. 3(e) after a heavy-ion strike. The increase in substrate leakage are caused by how fast the heavy-ion swept out from the uppermost portion of the device. But oxide thickness reduction maintain these leakage as traps due to radiation are going to very less, also the charge bulid-up in the SiO_2 is swept out quickly, so a very short time leakage current flows in thin oxides.

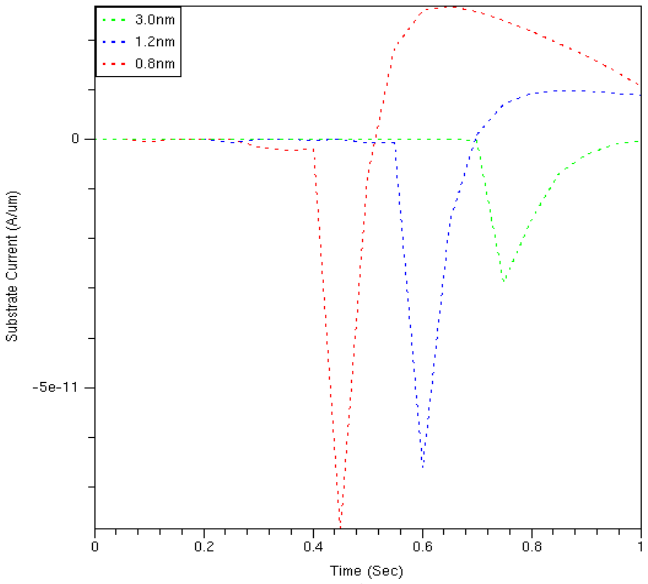

Fig. 3 (e). Body leakage current vs time of simulation. Here leakage is maximum when ion strikes and quickly swept out in thin oxide. Legen indicates the oxide thickness.

v. Conclusion

We demonstrate that charge trapping in oxides induces an unexpected shift in electrical parameter of MOSFET. As the scaling of semiconductor devices goes on progressing, the thickness of dielectric (here SiO_2) used in the device fabrication is also scaled down and thus, there is very less area for the radiation induced charge to trapped in the oxide. These devices feature an ultra-thin gate oxide (< 1nm) which does not trap any adequate fixed charge.

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