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A Low-Power Sample-and-Hold Amplifier using 0.05-µm CMOS Technology

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***Abstract*. This paper presents a sample-and-hold circuit based on a cascode-miller compensation technique, utilizing a class-AB operational amplifier as an output stage. Also using the techniques of pre-charging and output capacitor coupling can mitigate the requirements for the op-amp, resulting in low power dissipation. Power consumption is about 300µW from a single 1-V power supply. The performance of this SHA is not degraded even if input frequency approaching up to Nyquist frequency.**

Keywords— **Sampling, Sample and Hold (SHA), ADC (Analog to Digital Converter), Power Consumption.**

I. Introduction

Sample-and-hold amplifiers (SHA's) play a critical role in the design of data acquisition interfaces especially analog-to-digital converters [1]. A high speed high resolution S/H amplifier designed for analog to digital converter applications. Unfortunately, charge injection error is the main problem of S/H circuits resulting in accuracy reduction of these circuits and hence the creation of non-linearity distortion. A number of circuits were designed in order to improve either high-speed or high-accuracy [2-4]. They are usually the most power hungry blocks of ADC's since they should drive the largest capacitive load while maintaining the highest accuracy needed in the ADC equal to the total resolution of the converter. The power consumption will be even higher when the supply voltage is scaled down to small values such as 1-V. First, since the full-scale voltage swing of the ADC is shrunk, to save the same signal-to-noise ratio the capacitor values of the residue stages as well as the SHA are to be increased. Second, to achieve the same gain-speed-swing performance of the operational amplifiers single-stage configurations will be no more useful and two-stage structure consumes more power.

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The resolution of the conventional high speed open loop SHAs is usually limited to 8-10 bits due to the non-ideal effects of switches such as charge injection and clock feed through [5-7]. On the other hand speed of high-resolution closed loop SHAs is determined by the performance of the operational amplifiers. In this paper low-power design techniques for low-voltage fast-settling opamps have been merged in order to reduce the power consumption of a 1-V 8-bit 100M-Samples/s fully-differential SHA.

II. The Sample and Hold (SHA)Amplifier Configuration

The common configurations for the realization of a closed-loop switched capacitor SHA are shown in the Fig. 1 [8].

Since the feedback factor of the op-amp in the flip-around SHA of Fig. 1 is larger, the power consumption will be smaller. However, the common mode input and the output of the opamp should be similar for the structure of Fig. 1.

The associated clock waveforms that eliminates clock feed-through and charge injection to a first order is shown in the Fig. 2.The switches in this figure are closed when their cont. rolling clock signals are high. The basic operation can be understood by considering the state of the circuit at t 0. At this time the input signals charge the sampling capacitors. At this particular instance of time, prior to t1, the amplifier is said to be operating in the sample mode of operation. At t1, the φ1 switches turnoff. The resulting charge injection and clock feed through appear as common mode signals on the inputs of the op-amp are ideally rejected. Since the top plate of the hold capacitor are always at *VCM*, at this point in the time of charge injection and clock feed through are independent of the input signals. This produces increase the dynamic range of sample and hold. The voltage on the inputs of the op amp between t 1 and t2 is *VOFF1 + VCM*, a constant voltage. Note that the op amp is operating open loop at this time between t1 and t3 should be short.

At t2 the φ2, switches turn off. At this time point in time, the voltages on the bottom plates of the sampling capacitors are *vinp* and *vinm*. The voltages on the top plates of the capacitor are *VOFF1+VOFF2+VCM*. The term V_{OFF2} is ideally a constant that results from the charge injection

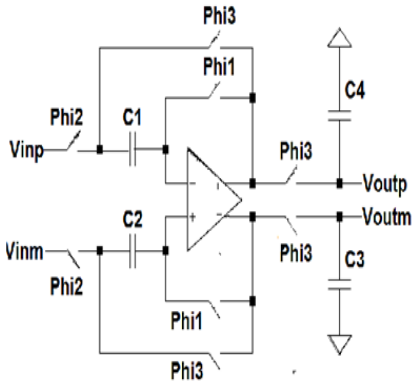

Figure 1: Flip-Around SHA Configuration

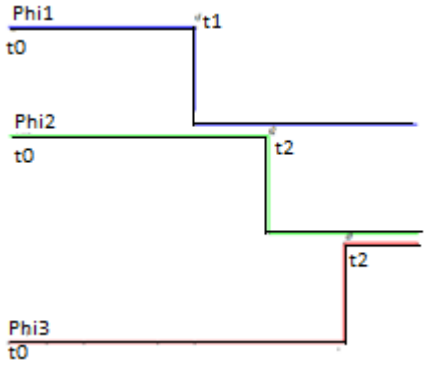

Figure 2: Sample and hold clocks and capacitive feed through from φ2 switches turn off. The tie between t1 and t2 should be short compared to variation in the input signals.

At the time t1, the φ3 switches turn on and the op amp behaves like a voltage follower; the circuit is said to be in the hold mode of operation. The charge injection and clock feed through resulting from the φ3 switches turning on causes the top plate of the capacitor to become *VOFF1+VOFF2+VOFF3+VCM*, again assuming that the storage capacitor are much larger than the input capacitance of the op amp. The output of the sample and hold are *Voutm* and *Voutp*.

Since the input referred noise of the front end SHA directly affects the ADC input-referred noise, this stage should have the smallest kT/C noise and therefore the largest capacitor values of the ADC. On the other hand, the load capacitance of this SHA in the hold phase is the sampling capacitors of the first residue stage of the ADC. Since the kT/C noise of the first residue stage is also directly transferred to the ADC input (with gain unity for the SHA) the size of these capacitors also needed to be large. The number of these capacitors might be usually chosen greater than 2^1 for a residue stage resolving more than 1 effective bit in a high resolution ADC [9]. Therefore the total load capacitance of the front-end SHA of a 1-V 8-bit ADC can be as large as 250fF. The accuracy of the SHA directly affects the accuracy of ADC. For an 8-bit ADC, the output settling error of the SHA should be less than $1/2^{12}$ of its final value.

Consequently the opamp required for this 1-V 100M-Samples/s 8-bit SHA must have a DC gain of less than 60dB and its output should be settle in less than 10ns. The entire static power of the SHA is dissipated in the opamp. Therefore, design technique should be employed to reduce the power consumption of the opamp.

III. Low Power Operational amplifier Design

To satisfy the high-gain and high-swing behavior of the opamp with a 1-V supply a two-stage configuration with a folded-cascode first stage and a class-A/AB second stage is chosen. The schematic of the two stage opamp is shown in the Fig. 4.

Figure 3 shows a cascode load op-amp. Seen in the Figure are typical values for the voltages in the circuit assuming gate-source voltages of 400mV and, for the bottom two rows of NMOS devices, drain-source voltage of 100mV. Notice that *Vbias* is used to bias the second row devices, which puts 200mV across the drain-source voltages of the PMOS devices. This results in larger gain and reduced voltage swing.

The circuit's limited output swing is not a major draw-back in this SHA application The continuous-time output common-mode feedback (CMFB) using two source-coupled pairs is suitable here due to reduced output voltage swing.

Figure 3 shows the two stage op-amp with a CMFB circuit. The second stage of the opamp operates class AB. We used 50fF capacitors for compensation in this op-amp.

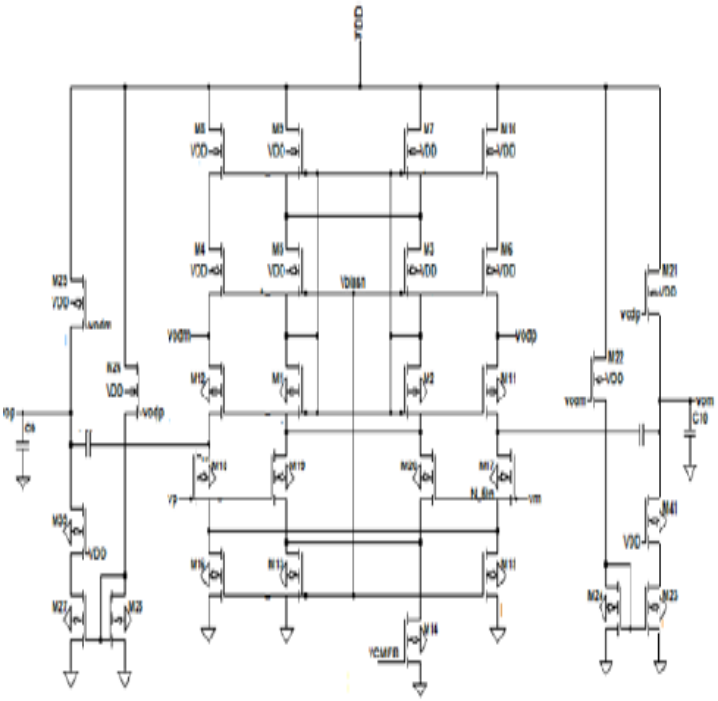

Figure 3: Two stage class A/AB op-amp

Slew rate limitations caused by the diff-amp

driving the compensation capacitor is

Slew rate = ISS/CL=dVout/dt……(1)

= 200µA/50fF = 400mV/ns

Figure 4 shows the DC characteristics of the op-amp shown in Figure 3. Where we've held the inverting op-amp input at the common-mode voltage and swept the voltage on the non-inverting input. The output voltage swing all the way from ground to V_{DD}. The op-amp's DC gain is approximately 550 without DC load.

The thermal noise in the input sampling network in the sample mode can be expressed as:

$$\overline{V_n^2} \approx \frac{kT}{C_S+C_0+C_L} \quad (2)$$

A total load capacitance of 250fF is used to achieve 8-bit resolution with $2V_{pp}$ differential signal.

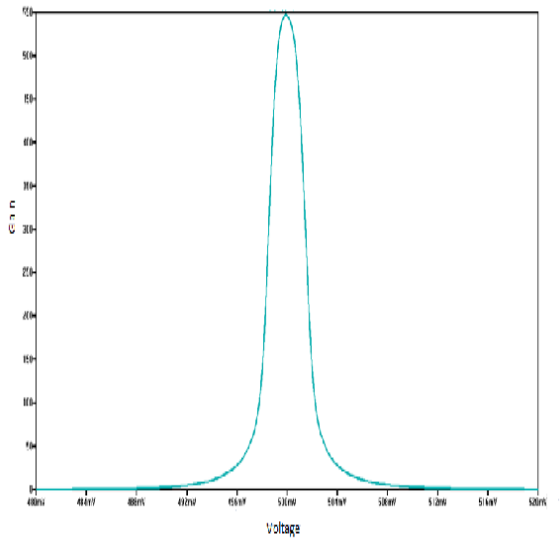

Figure 4: DC gain with class A/AB

This SHA is simulated with SPICE in all process/ temperature corners using BSIM3v3 models of a 0.05µm CMOS process.

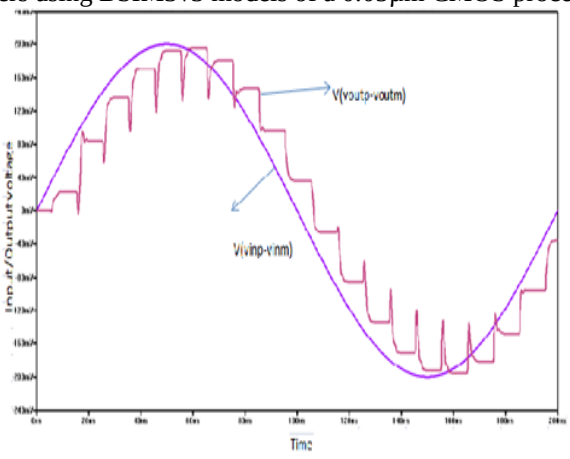

Figure 5: Input/output simulation of SHA

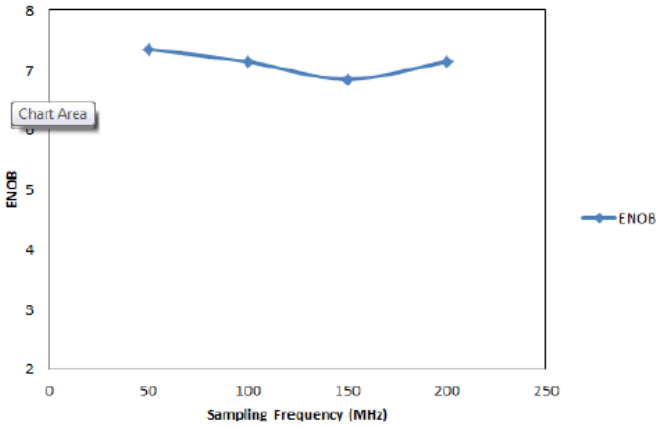

Figure 6: ENOB vs. Sampling Frequency

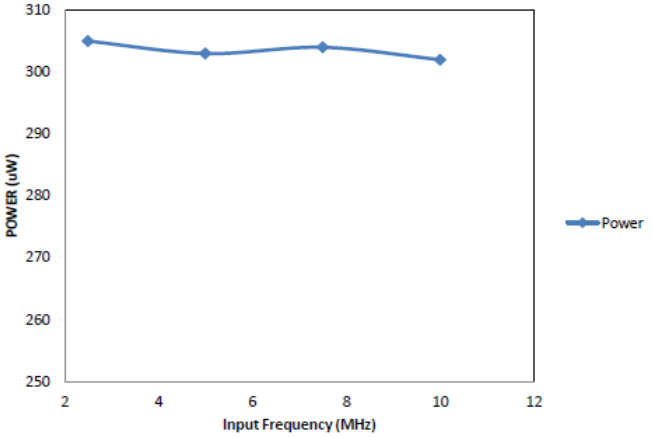

Figure 7: Power vs. Input frequency

The SHA is designed based on standard 0.05µm CMOS process. The complete SHA consumes only 303µW power. The operational amplifier has DC gain of 56 dB and a phase margin of 48^0 in closed loop configuration.

Figure 6 shows the simulated ENOB of the SHA versus the sampling frequency. The sampling frequency is 100MHz and the input has a 2Vpp differential voltage. The SHA achieves a minimum ENOB of 7.14 over entire frequency band.

Figure 7 shows the power consumption with the input frequencies it is about 300µW.

Table 1: Summary of measured performance

Technology	TSMC 0.05µm
Resolution	8-bit
Sampling Rate	100MHz
Supply	1-V
Input Range	Rail-to-Rail
Power consumption	303µW
ENOB	7.14@ F_S=100MHz & F_{in} =5MHZ

Table 2: Comparison with published SHAs

Sample rate	# bits	V_{DD} (V)	Swing (V_{pp})	P_{diss}	Tech
50MS/s	10	5	4.4	47mW	1.2µm
103MS/s	10	6	2.84	16mW	0.8µm
220MS/s	10	3	3.6	25mW	0.5µm
185MS/s	10	3.3	2	33mW	0.25µm
100MS/s	12	2.5	2	33mW	0.25µm
100MS/s	8	1.0	2	303µW	0.05µm (**Present work**)

IV. Conclusion

In this paper, a 1-V 100M-S/s 303µW 8-bit Sample-and-Hold amplifier was implemented and compared with 12 bit 100MS/s.It is observed that by using cascode miller compensation in new class-AB output operational amplifier there's considerable decrease in power consumption. . The LT-SPICE simulation results in a 0.05µm CMOS process were presented to confirm the effectiveness of the presented power reduction approaches in the designed SHA compared to few recent researches.

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