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A Design for Cyclic Time-to-Digital Converter

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Abstract*—The time-to-digital converter is a widely used device for measuring pulse width, jitter and timing characteristic of signal. In this paper, we present a cyclic time-to-digital converter based on the pulse-shrinking technique. Through utilizing the Schmitt trigger and design rules, the resolution of pulse-shrinking cell can be precisely adjusted by controlling the high and low threshold voltage of the transition. The proposed time-to-digital converter was implemented by TSMC 0.35μm 3.3V process and the simulation results show the resolution of circuit is very well that less than 20ps. In addition, within 4ns, the differential nonlinearity is less than 0.5LSB with respect to the resolution of 20ps.

***Keywords*—time-to-digital converter, pulse-shrinking element, Schmitt Trigger**

I. Introduction

Time-to-digital converter (TDC) is widely used in laser range-finder, all digital delay-locked loop (DLL), smart temperature sensor, built-in self-test circuit, automatic test equipment and so on [1-3]. There are various methods of designing TDC. These methods can be categorized into two major structures: analog and digital. Based on the time-to-voltage conversion and dual-slope method, the conventional analog structure for time interval measurement is charging or discharging a capacitor with a constant current to integrate an analog voltage and converting the voltage into a digital code by an analog-to-digital converter (ADC) [4-5]. However, these structures are vulnerable to system noise. Based on the delay element, the digital structures can be further classified into several kinds such as the vernier delay line based [6-7], and the pulse-shrinking based [8-11]. The vernier delay structure often utilizes two digital delay lines with different delay quantity respectively to produce multiphase clocks for a D flip-flop chain. The effective time resolution of vernier delay structure is determined by the difference between two digital delay lines. However, the mismatches between the delay cells cause resolution degradation. Even with careful layout, the mismatching effect cannot be eliminated completely.

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Conventional pulse-shrinking TDC allows that the pulse width under measurement is shrunk continuously by a pulse-shrinking chain. However, the calibration of the TDC must be done before performing measurement. The cyclic TDCs were therefore presented to simplify calibration process. In addition, the cyclic TDC with multi-stage pulse-shrinking delay line was presented to increase the speed of timing measurement [10].

In this work, we present a cyclic time-to-digital converter based on the multi-stage pulse-shrinking technique for rapidly converting pulse width into the corresponding digital code. The pulse-shrinking cell is utilizing Schmitt trigger instead of conventional inverter pairs. The resolution of pulse-shrinking cell can be precisely adjusted by controlling the high and low threshold voltage of the transition.

II. Overview of Pulse-Shrinking Cell

A. *Voltage-Controlled Pulse-Shrinking Cell*

The conventional voltage-controlled pulse-shrinking cell is shown in Fig. 1. It consists of a voltage-controlled current-starving inverter followed by a output buffer. The rising propagation delay T_r of the current starving inverter is controlled precisely by the analog bias voltage V_{bias} while the falling propagation delay T_f is controlled by aspect ratio of the transistor M_1. Thus, the resolution of the pulse-shrinking is the difference ($T_r - T_f$) between the rising and falling propagation delay time.

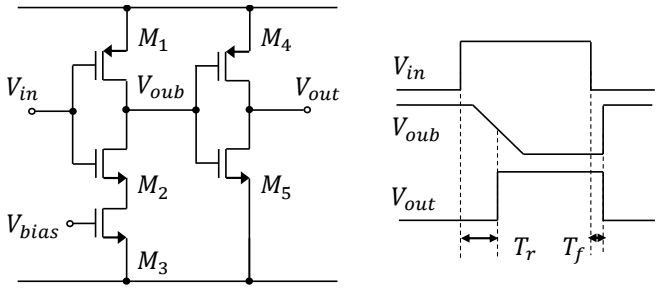
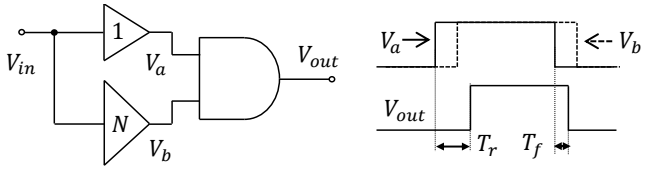


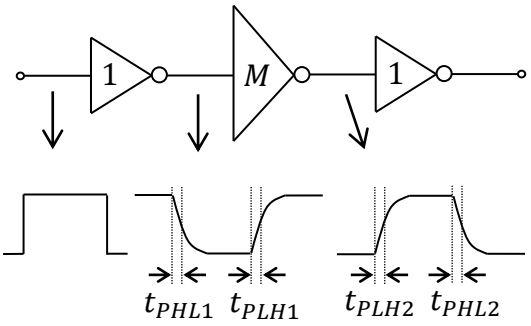
Figure 1. The conventional voltage-controlled pulse-shrinking cell.

B. *Dimension-Controlled Pulse-Shrinking Cell*

As mentioned above, since the resolution is determined by controlling the analog bias voltage. The analog bias voltage must be adjusted precisely through calibration process to make the resolution fine enough. Therefore, the pulse-shrinking cell without the need of adSditional analog bias voltage is more suitable in general TDC design. The dimension-controlled pulse-shrinking cell is shown in Fig. 2(a). The input pulse is simultaneously fed into the small and the large buffers to generate two pulses (V_a and V_b) with different delay time (T_r and T_f) respectively, then the output pulse is the result of the two pulses after passing an AND gate. The resolution ($T_r - T_f$) is completely depending on dimension of the two buffers. Another kind of dimension-controlled pulse-shrinking cell is shown in Fig. 2(b). Through controlling the propagation delay time of the small and the large inverters, the pulse width reduction can be found as $t_{PHL2} - t_{PLH2} + t_{PLH1} - t_{PHL1}$.



(a)



(b)

Figure 2. The conventional dimension-controlled pulse-shrinking cell.

III. Circuit Description

A. *Schmitt-Trigger-Based Pulse-Shrinking Cell*

Since cyclic TDC with dimension-controlled pulse-shrinking cell has the advantages of easier calibration process and small area overhead, we present a new cyclic TDC in which Schmitt triggers are used as dimension-controlled pulse-shrinking cell. The basic schematic of Schmitt trigger with output buffer is shown in Fig. 3. Through theoretical analysis, the high and low threshold voltage (V_{SPH} and V_{SPL}) of the transition can be expressed as:

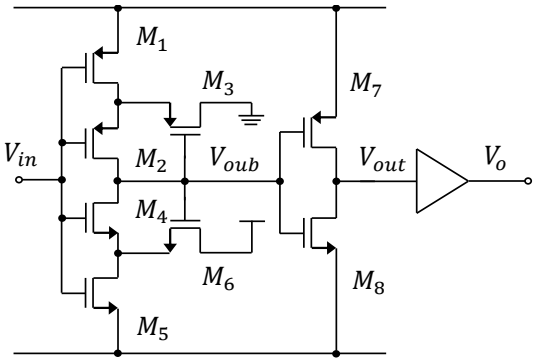


Figure 3. The Schmitt-trigger-based pulse-shrinking cell.

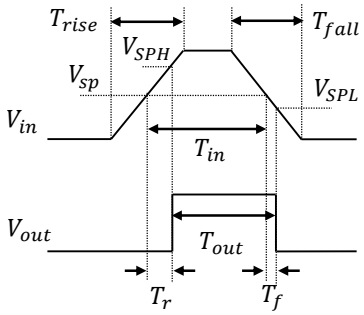


Figure 4. The concept of Schmitt-trigger-based pulse-shrinking cell.

$$V_{SPH} = \frac{V_{DD} + \sqrt{\frac{\beta_5}{\beta_6}} \cdot V_{th5}}{1 + \sqrt{\frac{\beta_5}{\beta_6}}} \quad (1)$$

$$V_{SPL} = \frac{\sqrt{\frac{\beta_1}{\beta_3}} \cdot (V_{DD} - V_{th1})}{1 + \sqrt{\frac{\beta_1}{\beta_3}}} \quad (2)$$

, where V_{th} is the threshold voltage of transistor and $\beta_n = \mu_0 \cdot C_{ox} \cdot (W_n / L_n)$. According to equations above, both high and low threshold voltage (V_{SPH} and V_{SPL}) of the transition are controllable through tuning the aspect ratio of transistors. The concept of Schmitt-trigger-based pulse-shrinking cell is shown in Fig. 4. For simplifying the derivation, we assume that both rise and fall time (T_{rise} and T_{fall}) of input pulse V_{in} are ideal and constant. Then the difference between input and output pulse width can be expressed as:

$$T_{in} - T_{out} = \frac{1}{V_{DD}} \left[T_{rise} \cdot (V_{SPH} - V_{SP}) - T_{fall} \cdot (V_{SP} - V_{SPL}) \right] \quad (3)$$

, where $V_{sp} = V_{DD} / 2$.

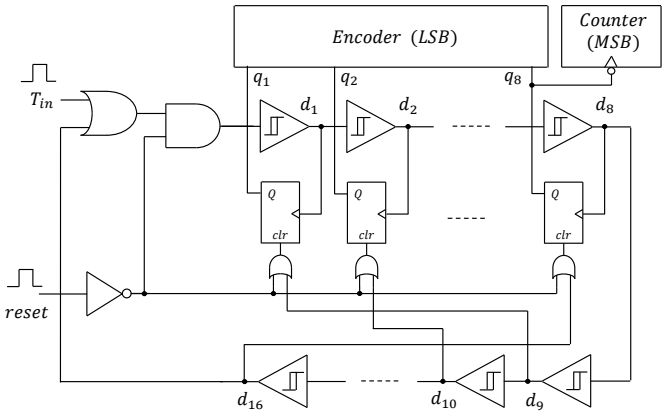


Figure 5. The proposed cyclic TDC.

B. *The Proposed Cyclic TDC*

The proposed cyclic TDC is shown in Fig. 5 which consists of a control unit (AND gate and OR gate), two pulse-shrinking delay lines, A D flip-flop chain, a digital counter and an output encoder. In Fig. 5, two 3-bit pulse-shrinking delay lines, A and B, are composed of $d_1 \sim d_8$ and $d_9 \sim d_{16}$ respectively. In measurement process, the outputs ($d_1 \sim d_8$) of delay-line A are used to trigger the D flip-flop chain while the outputs ($d_9 \sim d_{16}$) of delay-line B are connected to the same D flip-flop chain as the reset signal. The falling-edge-trigger counter is triggered once delay-line A and B finish shrinking both. Finally, A 8-bit Johnson code ($q_1 \sim q8$) is produced by the D flip-flop chain and then encoded into the corresponding 4-bit digital code at the end of the measurement process. According to the method mentioned above, the measured time interval T_{meas} can finally be calculated and expressed as:.

$$T_{meas} = (number_{counter} \cdot 2^4 + number_{encoder}) \cdot \Delta t \qquad (4)$$

, where Δt is the resolution of pulse-shrinking cell, $number_{counter}$ and $number_{encoder}$ are the count of counter and encoder respectively. Based on the multi-stage pulse-shrinking technique, the proposed cyclic TDC can rapidly measure long pulse width as well.

IV. Simulation Result

In this section, we demonstrate the practicability of proposed design through simulating both circuits of Fig. 3 and Fig. 5 in TSMC 0.35µm 3.3V process. According to the derived equation in (3), the transistor sizes used for M1, M3 and M5 are 3µm/0.35µm, 2µm/0.5µm and 1µm/0.35µm, respectively. Then, the simulation result for different resolution of Schmitt-Trigger-Based Pulse-Shrinking cell is shown in Fig. 6. The simulation result shows that the pulse-shrinking cell is able to reach very fine resolution even less than 20ps by well tuning the aspect ratio of transistors. To verify the linearity of proposed cyclic TDC, a series of pulses with different width were fed into the TDC for coding. The measured outputs are reported in Fig. 7. The average resolution is about 20ps. Fig. 8 shows that the differential nonlinearity (DNL) is less than 0.5LSB within the range of 1ns to 5.4ns. In addition, we compared our design with several published techniques and summarized into Table I. It shows the competitiveness of proposed design. Although average power of proposed cyclic TDC is slightly larger than others, the linearity of proposed design is almost comparable to that of other designs.

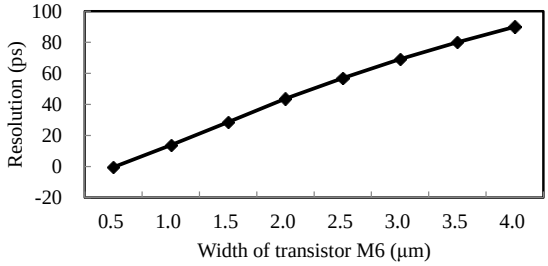


Figure 6. Influence of transistor size on the pulse-shrinking.

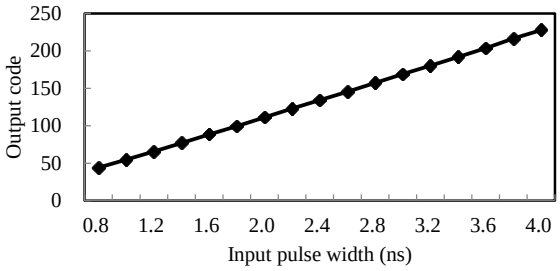


Figure 7. The digital output code of proposed cyclic TDC.

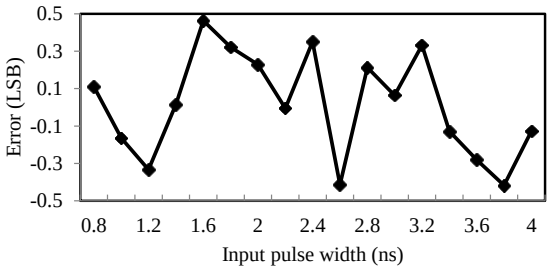


Figure 8. The measured error of proposed cyclic TDC.

TABLE I. COMPARISON OF SEVERAL TECHNIQUES

	[9]	[10]	This work
Technology	0.35µm	0.13µm	0.35µm
Resolution	68ps	20ps	20ps
Error (DNL)	0.8LSB	0.5 LSB	0.5LSB
Power	1.2mW	1.09mW	1.27mW

v. Conclusion

In this paper, we have presented a cyclic time-to-digital converter based on the pulse-shrinking technique. To alleviate the need of external analog bias voltage and calibration process, we utilize the Schmitt trigger as dimension-controlled pulse-shrinking cell instead of voltage-controlled pulse-shrinking cell. This advantage enables the pulse shrinking capability of the pulse-shrinking cell can be completely controlled by the dimension ratio of the transistors. In addition, based on the multi-stage pulse-shrinking technique, the proposed cyclic time-to-digital converter can be applied to rapidly convert long pulse width into the corresponding digital code. The simulation results show that the resolution of proposed design is 20ps and the maximum error is within 0.5LSB under the implement of TSMC 0.35μm CMOS process with 3.3V power supply.

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