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An Omni-Protection Scheme for Class-D Amplifiers

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Abstract*—Class-D amplifier has been a popular device because it features very high power efficiency. However, with increasing power demand, the over-current/-voltage/-temperature protections of amplifiers are necessary to prevent over-heated damage caused by consuming large power consumption over a long time. This paper thus presents the method to dynamically reduce the total power loss of class-D amplifier according to the feedback signal of temperature sensor. The proposed scheme simultaneously reduces the static and dynamic power loss by lowering current delivery progressively and enabling parts of segmented power stages that are in need of conduction. The simulation results show that the total power loss (i.e. excessive heat) and relative temperature difference on chip packages can be reduced to 5.8% of the maximum value that is 12% improvement than that of conventional design. Moreover, the corresponding improvement on power efficiency is over 19% for the cases of small modulation indexes which demonstrates the effectiveness of proposed scheme.

Keywords*—Power-loss control, over-temperature protection, class-D amplifier, multilevel technique, power efficiency.

I. Introduction

High-power class-D audio amplifier is gradually popular among TV and home theatre sets because of its high efficiency [1]-[4]. However, its ability of high power delivery may possibly over-heat itself because the power loss of amplifier is also increasing fast with the power demand, and therefore highlights the importance of system reliability. To prevent amplifier from damaging, the over-current (OC), over-voltage (OV) and over-temperature (OT) protections of high-power class-D amplifier (CDA) are in demand to reach the safe operating area (SOA) [5].

OC conditions are mainly arisen from loading variation or short circuit from output to power supply nodes, indeed, usually bring about the thermal runaway problem. This problem can be detected and lessened by restricting output current of amplifier within the acceptable limitation [5]-[9]. Moreover, OV is also called "clipping" because it happens when amplifier is over-driven. Under the OV situation, amplifier would be damaged because it is heated by maximum power loss for a long time. The influence can be mitigated by using automatic-gain-control (AGC) circuit to adjust the gain of pre-amplifier [10]-[15]. In addition, even in normal operation, This large power loss converts into excessive heat and raises the temperature of chip and PCB board, and hence seriously affects the system reliability. This problem is usually avoided by shutting amplifier down if the chip temperature is larger than the maximum limitations of chip packages. However, that will cause the audio holes problem [16]-[19]. In this work, a dynamic power-loss control scheme is presented to implement the protections of class-D amplifiers. Through dynamically adjusting the total power loss, the class-D amplifier could continue operating well without shutting itself down when OC, OV or OT conditions happen.

The paper is organized as follows. Section II introduces the thermal resistance of packages which defines the relationship between the junction temperature and power loss of chip. Section III presents the design of proposed protection scheme for class-D amplifier based on PWM and bridge-tied-load (BTL) configuration. The scheme comprises two control loops to reduce the static and dynamic power loss simultaneously. Moreover, the two control loops operate only when detecting the OT conditions. Finally, experimental results and conclusions are given in Section IV and Section V.

II. Thermal Resistance and Over-Temperature Problem

Figure 1 shows mechanisms of heat dissipation including conduction, convention and radiation. The relationship between the temperature of chip junction T_J and ambient T_A can be represented by the "Two-Resistor model" and further simplified as the thermal resistance θ_{JA} of packages as shown in Fig. 1 [20].

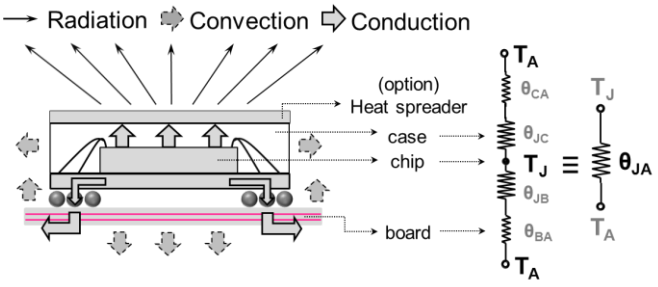

Figure 1. Mechanisms of heat dissipation and thermal resistance of chip packages.

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As seen in Fig. 1, the thermal resistance θ_{JA} of packages presents how the temperatures T_J and T_A and their difference relate to the power loss P_{Loss} (i.e. excessive heat) of chip and can be expressed as below:

$$\theta_{JA} = \frac{T_J - T_A}{P_{Loss}} \quad (1)$$

Therefore, it is usually used to estimate the power loss limitation of chip packages. For example, a thermal resistance 100°C/W of package with 90% power efficiency of amplifier delivering a 5V sine signal into a 4Ω speaker, the power loss and corresponding temperature difference on package can be calculated as below:

$$P_{Loss} = \left[\left(\frac{5/\sqrt{2}}{4}\right)^2 \cdot 4\right] \cdot (1-90\%) \approx 0.3W \quad (2)$$

$$\Delta T = T_J - T_A = P_{Loss} \cdot \theta_{JA} = 0.3 \cdot 100 \approx 30°C \quad (3)$$

Equation (3) means that the PCB temperature T_A will be larger than 70°C if the chip temperature T_J is over than 100°C, which seriously degrades the system reliability.

Moreover, with fixed power loss, the temperatures T_J, T_A and their difference ΔT are finally stabilized as shown in Fig. 2 and the thermal resistance θ_{JA} can be calculated by (1). The most important thing is that, according to (1), the temperatures T_J, T_A and their difference ΔT on package can be lowered by reducing the power loss P_{Loss} as shown in Fig. 2. In order to prevent amplifier from over-heated damaging, the protection scheme presented in this work is implemented by optimizing the control process of amplifier to reduce the total power loss instead of using complex package or extra devices outside chip to enhance the heat dissipation, and therefore reduces product cost [21]-[22].

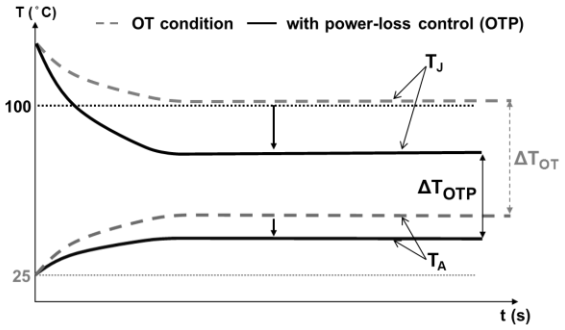

Figure 2. Over-temperature condition without and with power-loss control protection.

III. Proposed Omni-Protection Scheme

In this section, to protect the class-D amplifier against damaging, we consider the over-current (OC), over-voltage (OV) and over-temperature (OT) conditions which may possibly damage amplifier by raising chip temperature and present two control loops to prevent them by reducing the power losses. The static and dynamic power-loss are simultaneously reduced by lowering current delivery progressively, and by segmenting and enabling parts of power stages that are in need of conduction. Therefore, the total power loss of the amplifier is well controlled in order to prevent over-heating itself.

A. Over-Temperature Problems

The basic class-D amplifier, as depicted in Fig. 3, consists of a pulse-width modulator (PWM) and a bridge power stage which comprises two chains of gate drivers and two cascades of CMOS inverters. The CMOS inverters are mainly in charge to deliver required current into loudspeaker, therefore, its power loss is depended on output current i_{out} and expressed as below:

$$P_{OC,\lim} = \frac{1}{T_S}\int_0^{T_S} i_{out}^2 \cdot 2r_{on} \cdot dt \approx \frac{1}{2}(I_{\max} \cdot D)^2 \cdot 2r_{on} \quad (4)$$

,where T_S, r_{on} and D are period of input carrier, on-resistance of CMOS inverters and modulation index (the ratio between amplitude of input signal and carrier signal).

According to (4) and Fig. 3(b), under the OC condition, the power loss of OC will be four times of the maximum limit $P_{OC,\lim}$ if the output current ΔI_{out} is two times of the maximum value $I_{\max}$, which will raise unacceptable chip temperature.

Moreover, under the OV situation as shown in Fig. 3(c), the output voltage is clipped at supply voltage and its power loss can be calculated as product of maximum voltage and current and expressed as below:

$$P_{OV,\lim} = V_{Max} \cdot I_{Max} \quad (5)$$

This large power loss $P_{OV,\lim}$ will also cause OT problem if the duration Δt_{OV} of OV situation continues for a long time.

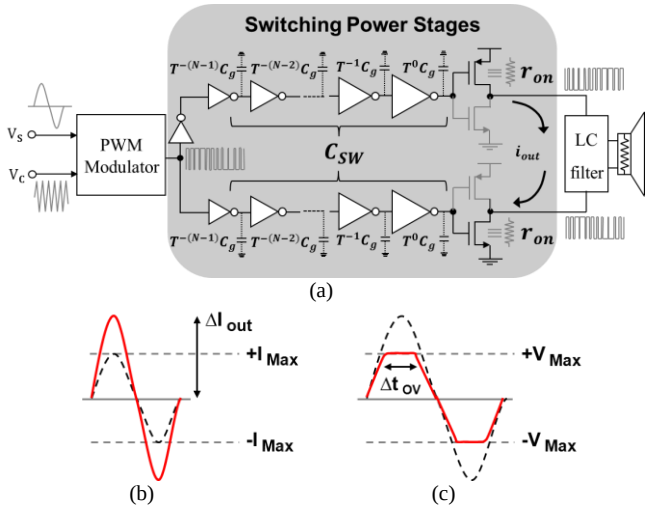

Figure 3. (a) Class-D amplifier with PWM modulator and bridge output stages, (b) over-current (OC) condition, and (c) over-voltage (OV) condition.

The general case is that, under normal operation, the switching power stages usually consumes the most of total power loss and should be designed carefully to prevent over-heating the amplifier. Its power consumption comprises the dynamic power loss $P_{D,GD}$ of gate driver chains and static power loss $P_{S,Tr}$ of cascaded CMOS inverters which are shown in Fig. 3 and expressed as below:

$$P_{D,GD} = \frac{1}{2} V_{DD}^2 \cdot f_{SW} \cdot 2\left[C_g \cdot \sum_{i=0}^{N-1} T^{-i} \right] = \frac{1}{2} V_{DD}^2 \cdot f_{SW} \cdot C_{SW} \quad (6)$$

$$P_{S,Tr} = \frac{1}{T_S} \int_0^{T_S} i_{out}^2 \cdot 2r_{on} \cdot dt \approx \frac{1}{2} (I_{out} \cdot D)^2 \cdot 2r_{on} \quad (7)$$

Figure 4 (a) shows the compromise between driving ability and power losses of switching power stages in case of different power demands (i.e. modulation index, D). For example, if we attempt to reduce the static power loss $P_{S,Tr}$ by enhancing its driving ability (i.e. larger transistor size) in large modulation index, the parasitic capacitance of larger inverter transistors would enlarge the dynamic power loss $P_{D,GD}$ that may be the prime loss in case of small modulation index. For this reason, in case of different modulation indexes, the sizes of gate driver chains and CMOS inverters should be dynamically adjusted to make less dynamic and static power loss as shown in Fig. 4(b).

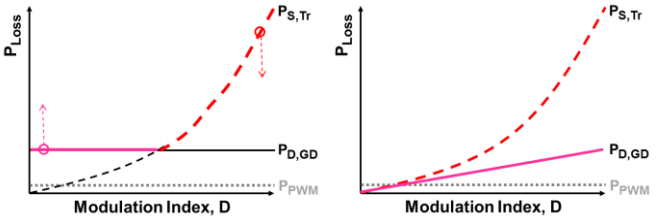

Figure 4. Power losses versus power demand in a class-D amplifier.

B. *Proposed Omni-Protection Scheme*

In this section, we present two control loops, as depicted in Fig. 5, to implement the controls of power-loss reduction and power loss minimization which are used to adjust the current delivery and driving ability of power stages, respectively. They are illustrated as following.

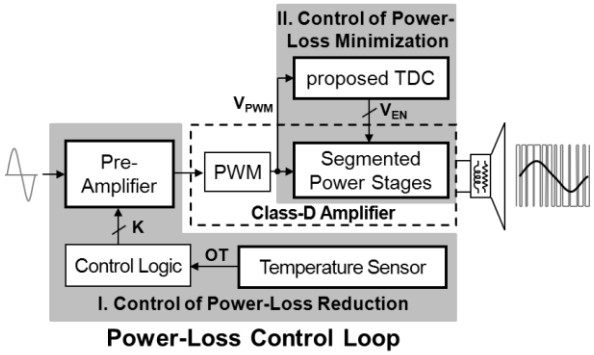

Figure 5. Block diagram of class-D amplifier with proposed over-temperature protection.

a) Control of power-loss reduction

The OC and OV conditions consume large static power-loss because the CMOS inverters are used to deliver heavy current, thus, we firstly attempt to reduce the current delivery step by step in order to lower the static power-loss and junction temperature as shown in Fig. 6. This can be achieved by applying pre-amplifier to audio or carrier input and adjusting their gain according to the value of integrated temperature sensor as shown in Fig. 5.

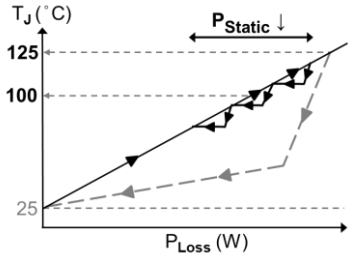

Figure 6. Progressive power-loss reduction versus junction temperature T_J.

b) Control of power-loss minimization

In addition to adjust the current delivery for power-loss reduction, the control of power-loss minimization is achieved in the meantime by adjusting the driving ability of power stages. The control of power-loss minimization consists of proposed time-to-digital converter (TDC) and segmented power stages as shown in Fig. 5. The input signal is processed by PWM modulator as usual and then the modulated signal is fed into the TDC and segmented power stages simultaneously. The TDC translates this modulated signal into digital binary codes representing the duty ratio of modulated signal and power demand of input signal. In order to obtain minimum power loss, the driving ability of power stages should be dynamically adjusted according to the power demand (i.e. modulation index, D). The output signal of proposed TDC is hence used to selectively enable parts of the segmented power stages that are in need of conduction.

The proposed TDC consists of a set of delay cell and an adder as shown in Fig. 7 [23]. The delay cell is a series of D flip-flop and each flip-flop provides propagation delay ΔT. The modulated PWM signal $V_{PWM}(t)$ is fed into delay cell and propagated to be $V_{PWM}(t - k \cdot \Delta T)$ consequently. If the number of D-flip-flop is M and carrier period of modulation is T_s, the delayed pulse signal of PWM can be further expressed as $V_{PWM}(t - k \cdot T_s / M)$. That is, the time slot of one period T_s is divided into M time slots and the PWM signal is arranged into each time slot. The adder then summarizes the value of signals in each time slot and results in a summation:

$$V_{EN}(t) = \sum_{k=1}^{M} V_{PWM}(t - k\frac{T_s}{M}) \quad (8)$$

Because the output signal of proposed TDC varies with the delayed pulse signal of PWM immediately, we have to describe the relationship between them by a macro point of view taking

its average value. The average value of output signal of proposed TDC within one period is then expressed as:

$$V_{EN}(t)_{avg} = \frac{1}{T_s}\int_0^{T_S} V_{EN}(t)\,dt = \frac{1}{T_s}\int_0^{T_S}\sum_{k=1}^{M} V_{PWM}(t - k\frac{T_s}{M})\,dt$$
$$= \frac{1}{T_s}\sum_{k=1}^{M} A\cdot t_n = (A\cdot M)\cdot\frac{t_n}{T_s} \quad (9)$$

,where A and t_n denote to amplitude and pulse width of PWM signal. According to (9), the average value of proposed TDC is proportional to the duty ratio (i.e. t_n / T_s) of PWM signal representing the power demand linearly in digital codes. Thus, we can adjust the driving ability of power stages directly by using the proposed TDC to enable the required segmented power stages.

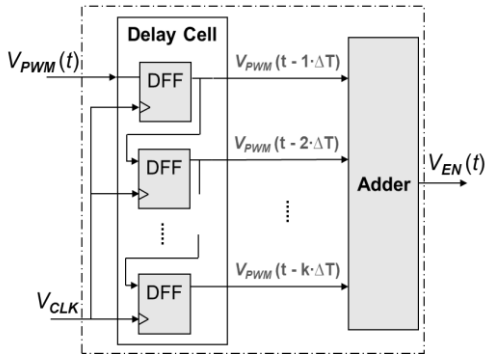

Figure 7. Block diagram of proposed time-to-digital converter (TDC).

For example, M =19 and $V_{EN}(t)$ varies between 18 and 19, means large duty ratio of PWM signal and great power demand from input signal. The 9 segmented gate drivers and CMOS inverters are all on duty in this situation. On the contrary, $V_{EN}(t)$ varies between 11 and 12, means smaller power demand that requires few segmented gate drivers and CMOS inverters. Through applying proposed method, the segmented gate drivers and CMOS inverters are selectively enabled on demand that gives substantial reduction in dynamic power loss. Thus, the total power loss is indeed minimized over a wide range of modulation indexes, especially for small modulation index.

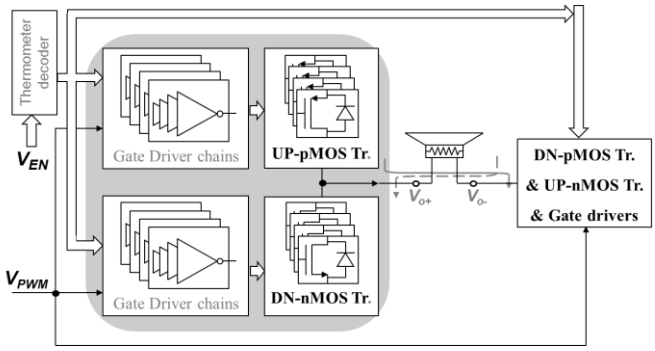

Figure 8. The segmented gate driver chains and CMOS inverters.

IV. Simulation Results

In this section, to demonstrate the improvement on reduction of total power loss and relative temperature difference on chip packages, TSMC 5V-0.35-um CMOS technology was used to implement two cases of PWM class-D amplifiers including (I) applying proposed method and (II) optimizing amplifier sizes for a range of modulation index D=0.1~0.9 [24]. With inductance L_o=45uH, capacitance C_o=1.5uF and resistance R_L=4Ω of the used low-pass filter and loudspeakers, both of two amplifiers delivered 2.7W of maximum power and consumed 0.2W of total power loss.

Fig. 9 shows the total power loss and relative temperature difference of two class-D amplifiers. With a 100°C/W thermal resistance of package, 0.2W of total power loss will cause 20°C difference on package meaning that excessive heat fails to be dissipated outside chip and the over-temperature would cause damage by overheating amplifier. Thus, the proposed scheme was applied to reduce total power loss and ΔT from 0.2W and 20°C (D=1.0) to 4.8mW and 0.48°C (D=0.1) step by step in order to prevent overheated damage. Moreover, that is 12% improvement in comparison with the other design.

Fig. 10 shows the power efficiency of two class-D amplifiers. It can be seen that there is 19% improvement at most on power efficiency in comparison with the other design when modulation index is below 30% of the maximum modulation index. The power efficiency is calculated as below:

$$\eta(\%) = \frac{P_{out}}{P_{out} + P_{Loss}}\cdot 100\% \quad (10)$$

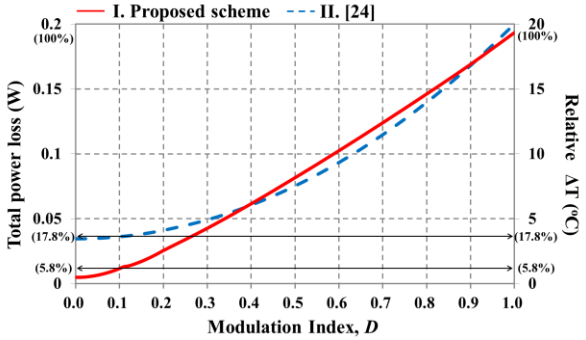

Figure 9. Power loss of amplifier and relative temperature difference on packages versus modulation index, D (i.e. the power demand).

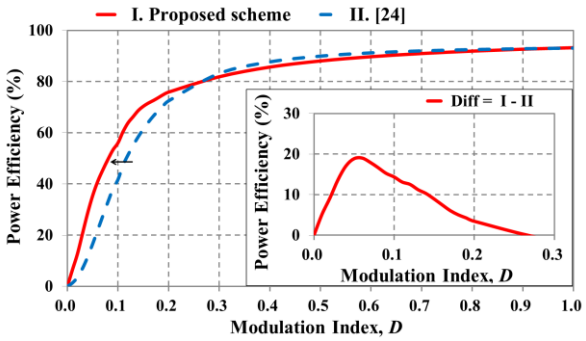

Figure 10. Power efficiency improvement of class-D amplifier power stages with and without proposed control.

v. Conclusions

The control scheme has presented to dynamically reduce total power loss and excessive heat for implementing the over-temperature protection of class-D amplifiers. By applying proposed protection scheme to amplifiers, the driving (static) power-loss is reduced by lowering output current delivery progressively. In the meantime, the switching (dynamic) power-loss is reduced by segmenting the CMOS inverters and their gate driver chains, and using the TDA output to enable parts of them that is in need of conduction. Thus, the total power loss of class-D amplifiers is well controlled and reduced in order to prevent over-heated damage caused by over-current/-voltage/-temperature problems which demonstrates the effectiveness of proposed scheme. Without using complex packages or extra devices outside chip to enhance the heat dissipation, the proposed scheme uses only simple digital circuits and hence reduces product costs.

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