International Journal of Advances in Electronics Engineering – IJAEE
Volume 4 : Issue 1 *[ISSN 2278 – 215X]*
Publication Date : 09 January 2014

A 0.35µm CMOS Pierce Oscillator for MEMS SAW Resonator

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Abstract— **This paper presents the pre and post layout simulation results for a pierce oscillator integrated with MEMS SAW resonator. The oscillator is designed to be interface with 1.78GHz MEMS SAW resonator. The pierce oscillator has achieved 18dB gain, 1.8GHz bandwidth and about 100° phase performance. The simulation is done using CMOS 0.35u technology. The pre layout simulation of MEMS oscillator is sustained at 1.775GHz, with 0.8V voltage swing. The post layout simulation is sustained at 1.766GHz and 0.35V voltage swing. The phase noise performance after post layout simulation is 97.94dBc/Hz at 100kHz cutoff frequency.**

***Keywords*— CMOS MEMS Oscillator, Pierce Oscillator, MEMS SAW resonator**

I. Introduction

Oscillators are the most important part in any electronic components. The accuracy and stability of the clock references will highly determine the performance of the electronic components. The electronic systems are considered best if they can lock and position them to the pseudorandom signal faster. The existing clock references are small but since they are based on piezoelectric material they cannot be fabricated on the same chip. Thus they consume more power. In this regards, MEMS based oscillators allow not only miniaturized system but also consume less power. MEMS based oscillator can also be integrated with other devices on the same die. Thus it is the best candidate to replace the traditional clock references.

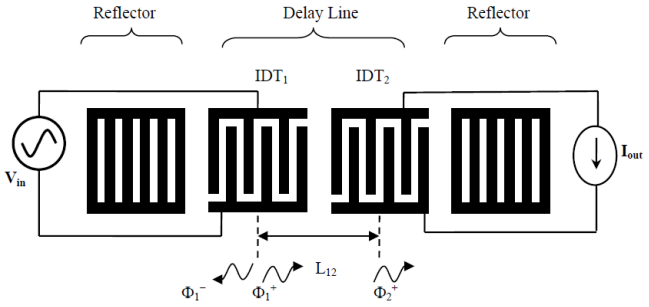
The research on MEMS resonator technology has begun as early as the year 1965[1]. Advancement in CMOS and MEMS technology has fueled much research on MEMS based oscillators [2-7]. The MEMS resonator used in the oscillator circuit generates frequency through either electrostatic or piezoelectric transduction [7]. The resonator will acquire the motional resistance during resonance. This motional resistance affects the insertion loss. To have good performance, the sustaining circuit should have the following characteristics: i. higher gain in order to overcome insertion loss of the resonator, ii. High bandwidth for optimal oscillation and iii. Small input and output impedance.

This paper presents the design of an oscillator for a MEMS SAW resonator. Section II presents the overview of MEMS SAW resonator and the sustaining circuit. Section III, shows the pre and post layout simulation result when both the resonator and the sustaining circuit are connected in closed loop connection. Section IV, summarizes the findings of this work.

II. Oscillator Circuit Implementation

A. *CMOS SAW Resonator*

The operating principle of SAW device is based on the piezoelectric effect. When a microwave voltage input is applied at the transmitting (input) IDT, it generates a propagating acoustic wave on the surface of the substrate [8]. This propagating acoustic wave in turn produces an electric field localized at the surface which can be detected and translated back into an electrical signal at the output IDT port. Thus with existence of reflectors, resonance is achieved. Figure 1, shows the two port and the equivalent circuit model of the SAW resonator. This circuit can be divided into two parts: acoustic and parasitic components. The acoustic component can be described electrically using circuit elements R_x, C_x, L_x, and C_f. The R_x is also known as the 'motional resistance", is a key factor in determining quality factor and insertion losses of the device. The existence of parasitic component which is represented by C_1 and C_2 in the circuit model can degraded the performance of the resonator.



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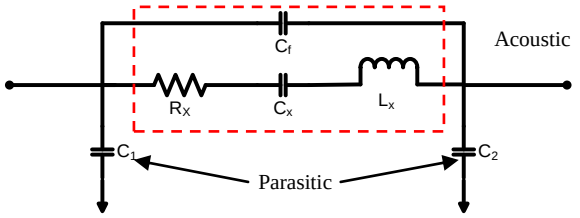


(b)

Figure 1: (a) Schematic of a two-port SAW resonator, (b) Electrical Equivalent circuit model for CMOS SAW Resonator

The Impedance of the resonator is given by:

$$Z_L = \frac{jX_{C_T}(R_x + jX_{C_x} + jX_{L_x})}{R_x + j(X_{C_T} + X_{C_x} + X_{L_x})} \quad (1)$$

The resonance frequency is given by:

$$f_r = \frac{1}{2\pi\sqrt{L_x C_x}} \quad (2)$$

The parameters extracted for CMOS SAW resonator based on measured S_{21} are as follows; $R_x = 185\Omega, L_x = 1.6uH, C_x = 5fF, C_f = 143.8fF, C_1 = C_2 = 300fF$. Consequently, equation 2 yield the resonant frequency at 1.779GHz. The simulated magnitude and phase of admittance result is shown in Figure 2.

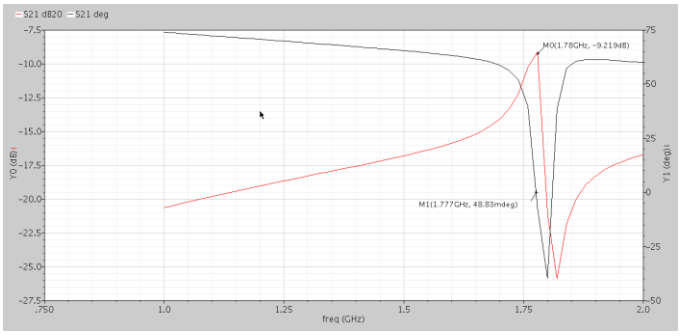


Figure 2: The simulated S_{21} magnitude and phase for CMOS SAW resonator.

From Figure 2, the insertion loss at series resonance is 8.65dB and for parallel resonance is 27.02dB. The series Q-factor of this SAW resonator at series resonance is 96. The value was obtained from equation 3[9].

$$Q_s = \frac{\omega_o L_x}{R_x} \quad (3)$$

The parallel Q factor is calculated using equation 4[9]; Q_p= 54.6.

$$Q_p = \frac{\omega_o L_x}{(R_x + R_{cap})} \quad (4)$$

Where, ω_o is centre frequency, R_{cap} is parasitic resistance.

B. *Sustaining Circuit Design*

The sustaining circuit to be integrated with CMOS MEMS SAW resonator must be able to overcome the insertion losses of the resonator and provide a unity loop gain and zero phase shift, as a consequence the oscillation is started up and sustained.

$$|\beta A_v| \geq 1$$

$$\angle \beta A_v = 0°, \pm 360°$$

For excellent phase noise characteristics, pierce oscillator circuit topology was chosen in this work. The circuit was adopted from [3]. Figure 3 shows the transistor level design of the pierce oscillator circuit topology. The design was implemented using the MIMOS 0.35um technology.

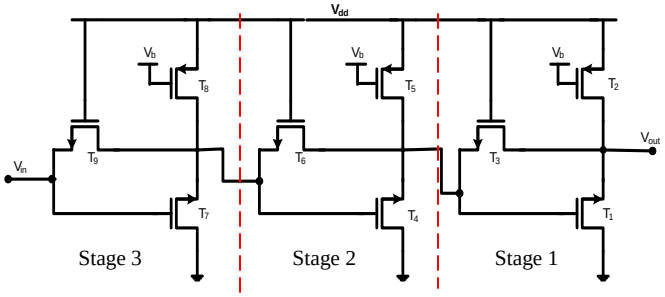
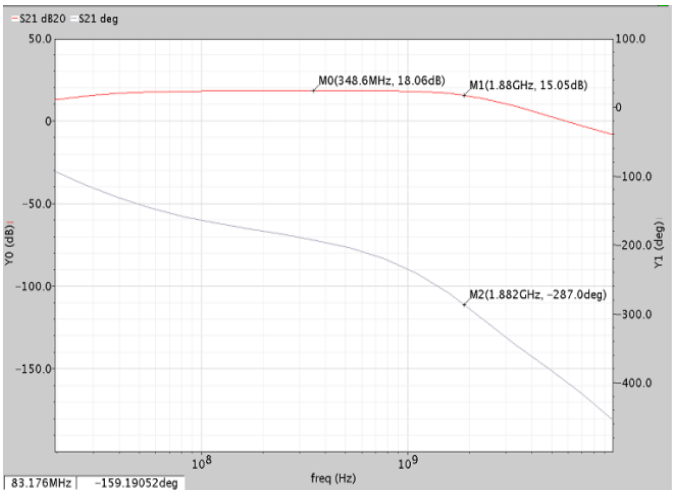


Figure 3: Schematic circuit of Pierce Oscillator Circuit Topology

T_1-T_3, is the single stage pierce circuit topology with T_1 as the main transistor provide the critical transconductance for oscillation. T_1 is biased by transistor T_2. Besides providing the bias resistance to the gate of T_1, T_3 also provided enough resistance to ensure the oscillation is sustained. Transistors T_4 through T_9 are added and become the second and third stages in order to ensure that the oscillation is started and sustained.

The gain and phase of the amplifier circuit shown in Figure 4,is obtained when V_{dd}=3V and V_b=820mV. The bias current I_{dT2}=1.06mA. The circuit has maximum gain of 15dB at 1.88GHz, 1.8GHz bandwidth and -100° phase response.



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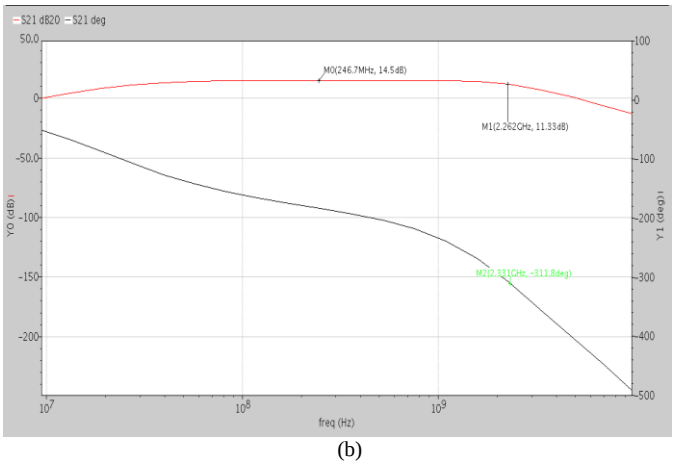


(b)

Figure 4: (a) Pre layout and (b) Post layout simulation for the Pierce oscillator Circuit design.

Figure 4(b) shows the maximum gain obtained after post layout simulation is 14.5dB and -40 phase response. Even though the maximum gain is lower, this gain is adequate enough to overcome the insertion loss of the resonator.

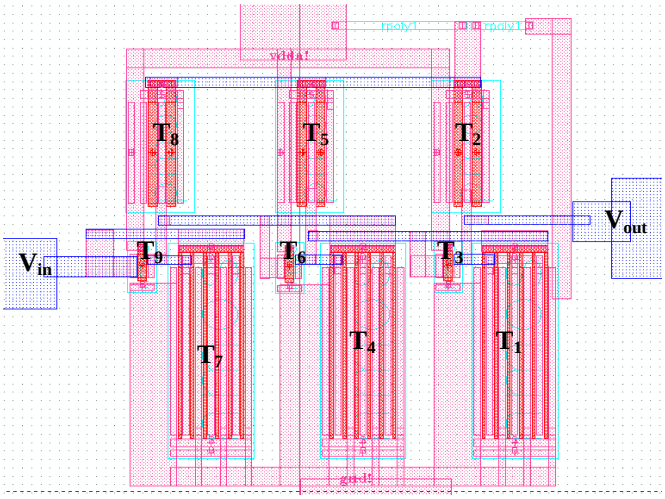


Figure 5: The layout design

The layout of the amplifier is shown in Figure 5.

III. Close Loop Simulation Output

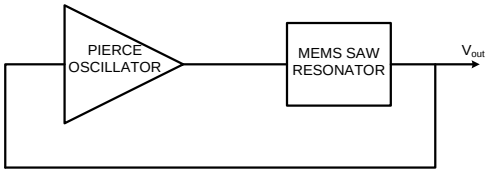
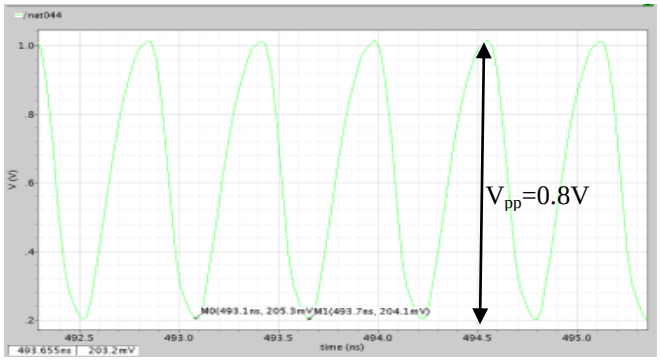


Figure 6: The block diagram of the Close loop system of Oscillator

Block diagram in Figure 6 shows the connection setup between the sustaining circuit and the resonator. For the oscillation to occur, no external input is required. The simulated transient output is shown in Figure 7. The amplitude of the oscillation is 0.8V for pre layout simulation and decrease to 0.3V for post layout simulation. Refer to equation 5, as the amplitude decrease, the signal power will decrease Figure 8 shows the PSS output power. Pre layout simulation shows that the highest power spectrum is 2.23dBm at 1.775GHz, and the highest power spectrum after the post layout simulation is -5.118dBm at 1.766GHz..

$$P_{sig} = \frac{1}{2}\frac{V^2}{R_L} \quad (5)$$



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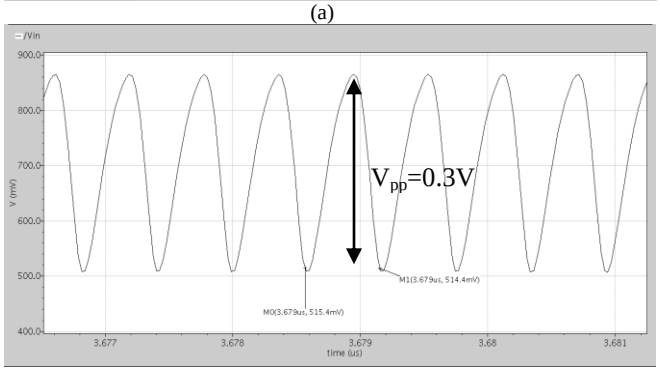
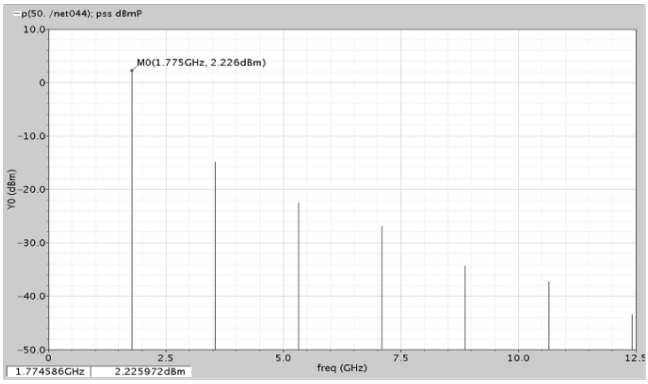


(b)

Figure 7: Transient output (a) pre layout and (b) post layout simulation



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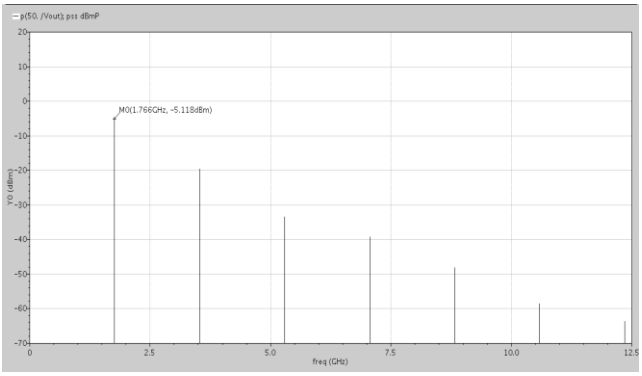
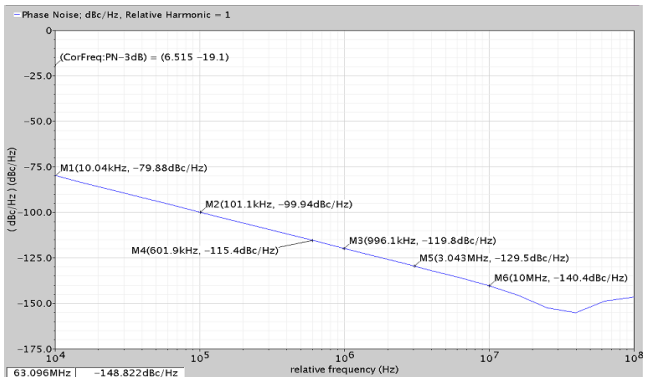
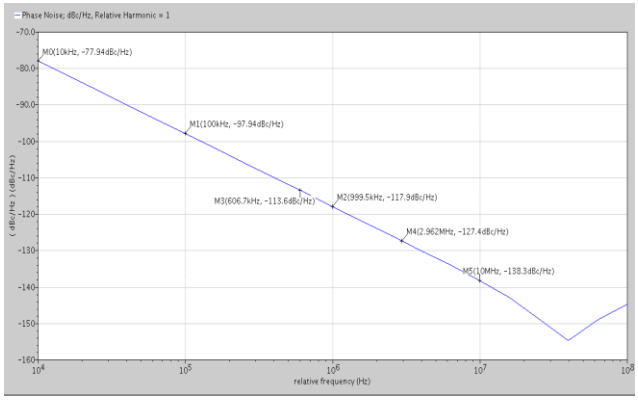


(b)

Figure 7: The PSS output (a) pre layout and (b) post layout simulation



(a)



(b)

Figure 8: Phase noise performance (a) pre layout and (b) post layout simulation

Phase noise performance for pre layout simulation and after post layout simulation did not have much different. Referring to figure 8, at cutoff frequency 100kHz, pre layout phase noise is 99.94dBc/Hz and the post layout phase noise is 97.94dBc/Hz. According to Leeson phase noise in equation 6, as the signal power is decrease the phase noise will increase.

$$L(\Delta\omega) = 10log\left[\frac{2FkT}{P_{sig}} * \frac{\omega_o}{2Q_L\Delta\omega}\right] \quad (6)$$

The phase noise performance obtained in this work is better than the authors' previous work in [10].

IV. Conclusion

The pre and post layout simulation of 1.78GHz oscillator based on MEMS SAW resonator has been carried out. Only slight differences were found for the pre and post layout result. The calculated Q factor for this MEMS SAW resonator is 96 at series resonance frequency. The phase noise performance for pre and post layout simulation is 99.94dBc/Hz and 97.94dBc/Hz respectively at 100kHz offset frequency. The highest power spectrum obtained for pre and post layout is 2.226dBm at 1.775GHz and -5.118dBm at 1.766GHz.

Acknowledgment

The authors wish to thank MIMOS BERHAD for fabricating the chips used in this work.

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