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Design Of Multimode Interleaver using OFDM in WLAN Application

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***Abstract*— Wireless technology is expected to be the dominant mode of access technology in the future, a new data range of services such as multimedia and high speed data are being offered for delivery over wireless network. The IEEE 802.11 is known as Wireless LAN, to obtain higher data rates it is used with OFDM, which is defined a speed upto 54 Mbps in 5-GHz band. In this paper we present a technique to model the interleaver used in IEEE 802.11a and IEEE 802.11g based WLAN in verilog HDL using Quartus 9.0 web edition. Our technique is comprises of OFDM which provide higher operating frequency in addition to reducing the effects like intersymbol and interchannel interferences.**

Keywords-WLAN; OFDM; memory; Multimode interleaver

I. Introduction

Communication system have three fundamental resources signal power , time and bandwidth. The general objective of these resources is to achieve maximum data transfer in minimum bandwidth, maintaining the quality of service.

In digital communication the quality depends upon the probability of bit error at the receiver. Data communications often require BERs on the order of $10^{-6} - 10^{-9}$. Such low values can only be achieved by employing coding of the data, i.e., introducing redundancy into the transmission. The use of error-correcting codes1 leads to a reduction of the BER. Shannon showed that it is possible to transmit data without errors as long as the bit rate is smaller than the channel capacity. Hamming also introduce the error correcting codes.

The use of Internet makes the quest of Broadband Wireless Access (BWA) as an alternative solution to Digital Subscriber Line (DSL) or cable modem for Internet access. BWA is the most challenging segment of the wireless communication. High processing speed, design flexibility and fast design Turn around Time (TAT) are the important requirements of BWA.

Wireless local area network (WLAN) links two or more devices using some wireless distribution method and usually providing a connection through an access point to the wider Internet. This gives users the mobility to move around within a local coverage area and still be connected to the network. An access point (AP) is installed to act as bridge between wireless and wired network. The AP is connected to wired network and is equipped with antenna to provide wireless connectivity. IEEE 802.11a and IEEE 802.11g based WLAN use orthogonal frequency division multiplexing (OFDM) that increases the overall throughput at access point. The IEEE 802.11 specification is a wireless LAN (WLAN) standard that defines a set of requirements for the physical layer (PHY) and a medium access control (MAC) layer. For high data rates, the standard provides two PHYs - IEEE 802.11b for 2.4-GHz operation and IEEE 802.11a for 5-GHz operation. The IEEE 802.11a standard is designed to serve applications that require data rates higher than 11 Mbps in the 5-GHz frequency band.

Orthogonal frequency-division multiplexing (OFDM) is a method of encoding digital data on multiple carrier frequencies. OFDM is popular due to its multi-path interference, and mitigate inter-symbol interference (ISI) causing bit error rates in frequency selective fading environments .OFDM has attained the high data rate by splitting the data stream into a number of low-rate sub-carriers (SC) instead of utilizing one carrier at a high rate. This increases symbol duration and improves system robustness. OFDM is achieved by providing multiplexing on users data streams on both uplink and downlink transmissions.

Digital communications are prone to random burst errors. Interleaving is used for error correction in block codes to make them effective in a burst noise environment. The interleaver spreads out adjacent data over multiple blocks of data. The primary role of interleaver is to disperse the sequences in a bit-stream so as to minimize the effect of burst errors introduced in transmission. An interleaver is usually used in conjunction with some type of error correcting code. By spreading the source bits over time, it becomes possible to make use of error control coding which protects the source data from corruption by the channel. Since error control codes are designed to protect against channel errors that may occur randomly or in a bursty manner, interleavers scramble the time order of source bits before they are channel coded. The transmitted bits are same

but ordered in some special way. This reordering of bits is called permutation of data. There are two categories named as block and convolution al interleaver.
A multimode interleaver employs hardware multiplexing
For implementation of the various specifications of the interleaver, The main challenges include real time low latency computation for different permutation function, higher throughput and low cost for different standards. The multimode functionality is then achieved by fast switching between different standards.

In this paper we propose a multimode interleaver using OFDM in WLAN. As per IEEE 802.11a and IEEE 802.11g standard, ½, ⅔ and ¾ are the allowed code rates where as BPSK, QPSK, 16-QAM and 64-QAM are the permitted modulation schemes. The interleaver comprises of two blocks namely address generator and interleaver memory. The address generator operates at higher frequency and provides better resource utilization.
The paper is organized into five sections. Section 2 discusses the interleaving in OFDM based WLAN. In section 3, describes proposed hardware model of the interleaver, while section 4 represents the simulation of hardware model. Finally, the paper is concluded in section 5.

II. Interleaver in OFDM based WLAN

IEEE 802.11a and IEEE 802.11g based WLAN uses identical interleaving technique in which a special type of block interleaver is used. The channel interleaving in WLAN is based on a block interleaver, which is expressed in the form of a set of two equations for two steps of permutations. The first step ensures that adjacent coded bits are mapped on to non-adjacent subcarriers, while the second step ensures that adjacent coded bits are mapped alternately on to less or more significant bits of constellation, thus avoiding long runs of lowly reliable bits. The first permutation m_k *for* index k is defined by:

$$m_k=(\ N_{cbps}/d).(k\ \%\ d) + \lfloor k/d \rfloor \quad (1)$$

Here N_{cbps} is the block size corresponding to number of coded bits per allocated sub-channels per OFDM. and typical value for *d* used in WLAN is 16. The operator % is defined as the modulo function, computing the remainder, and the operator *x* is the floor function i.e. rounding towards zero. The second permutation j_k for index k is given by:

$$j_k = s.\left\lfloor \frac{m_k}{s} \right\rfloor + \left(\left(m_k + N_{cbps} - \left\lfloor d.\frac{m_k}{N_{cbps}} \right\rfloor \right) \right) \quad (2)$$

The parameter s is defined as s= *max* (1, N_{bpsc} / 2), where N_{bpsc} is number of coded bits per sub-carrier, i.e., 1, 2, 4 or 6 For BPSK, QPSK, 16-QAM or 64-QAM respectively and *ceil* operation is the rounding towards infinity.

III. Hardware Architecture

The proposed hardware model of OFDM based WLAN interleaver consists of two sections: address generator and interleaver memory as shown in Fig. 1.

Table 1. Important parameters of 802.11a PHY layer

Information data rate	6, 9, 12, 18, 24, 36, 48, 54 Mbit/s
Modulation	BPSK, OPSK, 16-QAM, 64-QAM
FEC	*K* = 7 convolutional code
Coding rate	1/2, 2/3, 3/4
Number of subcarriers	52
OFDM symbol duration	4 µs
Guard interval	0.8 µs
Occupied bandwidth	16.6MHz

A. Address Generator

Address generation is the main concern for any kind of interleaving.

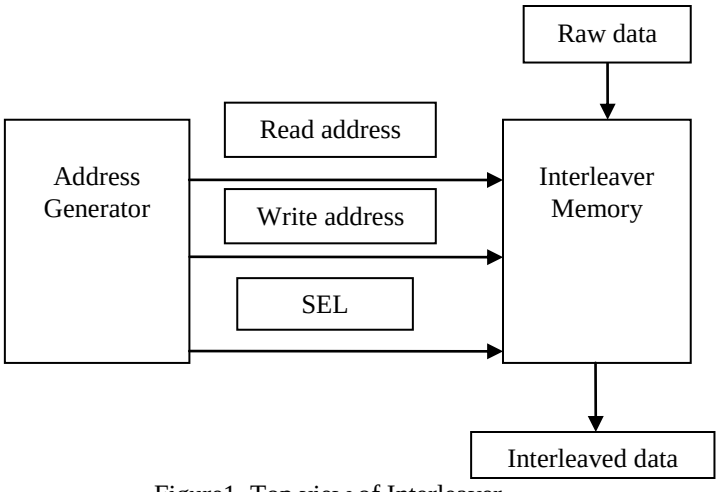

Figure1. Top view of Interleaver

The address generation block generates the interleaved address based on all the permutations involved in

implementing a block interleaver, whereas, it generates memory read and write addresses concurrently while implementing a convolutional interleaver. The role of address generation block to be used as an interleaver or de-interleaver is mainly controlled by the controller after employing an addressing combination for writes and reads from the memory. The Address Generation circuit of the block interleaver for WLAN system is basically the simultaneous implementation of eqn. (1) and eqn. (2).
Evaluating these equations with relevant Ncbps for different modulations we find all the values of jk, the address of interleaver memory out of which first 32 of each category are only listed in Table II.

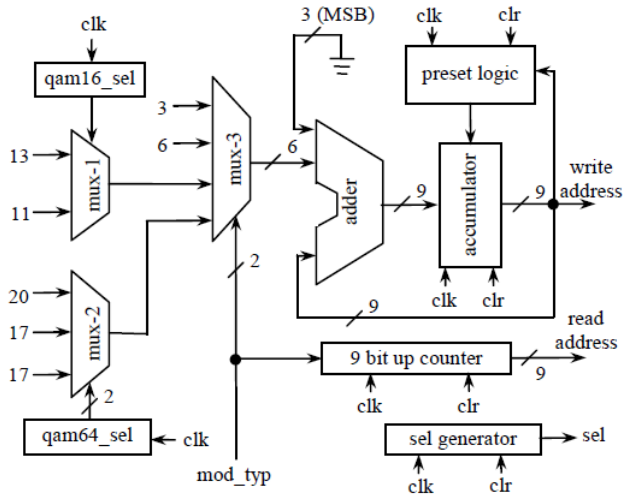

Figure 2. Block Diagram of Address Generator

Our proposed design of address generator block is described in the form of schematic diagram in Fig. 2. The circuitry is used for generation of write address. It contains three multiplexers: mux-1 and mux-2 implements the unequal increments required in 16-QAM and 64-QAM whereas mux-3 routes the outputs received from mux-1 and mux-2 along with equal increments of BPSK and QPSK. The select input of mux-1 is driven by a T-flip-flop named qam16_sel whereas that of mux-2 is controlled by a counter, qam64_sel. The two lines of mod_typ are used as select input of mux-3. The 6-bit output from the mux-3 acts as one input of the 9-bit adder after zero padding. The other input of the adder comes from accumulator, which holds the previous address. After addition a new address is written in the accumulator. The read addresses are linear in nature and are generated using a nine bit up counter as shown in Fig. 2. The counter is reset whenever it reaches to the terminal count for a desired modulation scheme. For example, in case of 16-QAM, the counter counts from 0 to 191 and then repeats. The sel generator is basically a T- flip-flop used to generate the select signal and is initialized to zero using clr input.

Table 2. First 32-permutation sample addresses for three code rates and modulation schemes

N_{cbps}=48 bits, BPSK (mod_typ =00)	0	3	6	9	12	15	18	21
	24	27	30	33	36	39	42	45
	1	4	7	10	13	16	19	22
	25	28	31	34	37	40	43	46
N_{cbps}=96 bits, QPSK (mod_typ =01)	0	6	12	18	24	30	36	42
	48	54	60	66	72	78	84	90
	1	7	13	19	25	31	37	43
	49	55	61	67	73	79	85	91
N_{cbps}=192 bits, 16-QAM (mod_typ =10)	0	13	24	37	48	61	72	85
	96	109	120	133	144	157	168	181
	1	12	25	36	49	60	73	84
	97	108	121	132	145	156	169	180
N_{cbps}=288 bits, 64-QAM (mod_typ =11)	0	20	37	54	74	91	108	128
	145	162	182	199	216	236	253	270
	1	18	38	55	72	92	109	126
	146	163	180	200	217	234	254	271

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Table 3. Data rates in 802.11a

Data rate (Mbit/s)	Modulation	Coding rate	Coded bits per subcarrier	Coded bits per OFDM symbol	Data bits per OFDM symbol
6	BPSK	1/2	1	48	24
9	BPSK	3/4	1	48	36
12	QPSK	1/2	2	96	48
18	QPSK	3/4	2	96	72
24	16-QAM	1/2	4	192	96
36	16-QAM	3/4	4	192	144
48	64-QAM	2/3	6	288	192
54	64-QAM	3/4	6	288	216

B. Interleaver Memory

Interleaver memory use two kind of memories: one is dedicated internal memory other is distributed memory. In block interleaving when one memory block is being written the other one is read and vice-versa.F.ig 3 is the RTL view of RAM used for interleaves the data. The memory input and output bit widths is generally constrained based on the requirements of the neighboring blocks. In the proposed design of memory clk, rst, wren, rden are acts as input and bout acts as output and a mux which provide many inputs to one output. One flip-flop which produce clock at the input of ram. Here memory is act as interleaver which disperses the sequence of bits. After a particular memory block is read / written up to the desired location, the status of sel changes and the operation is reversed. The mux at the output of the memory modules routes the interleaved data stream from the read memory block to the output. The data rates used in IEEE 802.11a is shown in table 3. Data rate is up to 54 Mbits/sec in 802.11a and g and the coded bits per OFDM symbol is 288.The maximum memory required for OFDM based WLAN interleaver is 288 bits.

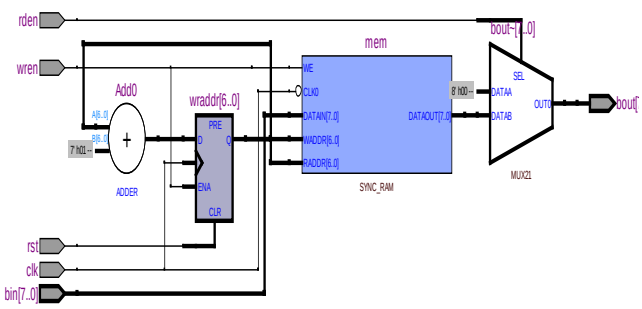

Figure 3. RTL view of Memory block.

Two identical memory blocks each of capacity 288 bits are required for implementation of block interleaver. In an interleaved memory, the memory is divided into a set of banks. An interleaved memory with n banks is said to be n-way interleaved. One way of allocating virtual addresses to memory modules is to divide the memory space into contiguous blocks.

IV. Simulation Result

Simulation result is in the form of timing diagram. It is obtained using Quartus II 9.0 edition using Verilog HDL language. In fig 4, we use 21 registers and 347 pins. In this simulation we select a MOD-TYP BPSK modulation scheme (mod_typ=00) have been chosen where first 16bits of raw data input (data_in) are held high. The effect of interleaver is visible as the consecutive 1's are dispersed by 3 bits position in the data output (data_out) line. This is because the write address sequence in BPSK modulation scheme is 0, 3, 6, 9… 47. Similar results are also obtained for other modulation schemes. Initially we make CLR = 1 to ensure that the counter in preset logic and accumulator are reset.

V. Conclusion

In this paper a technique to model the multimode interleaver using WLAN application is proposed. The proposed model is successfully simulated in Quartus-II 9.0. It consumes low power.

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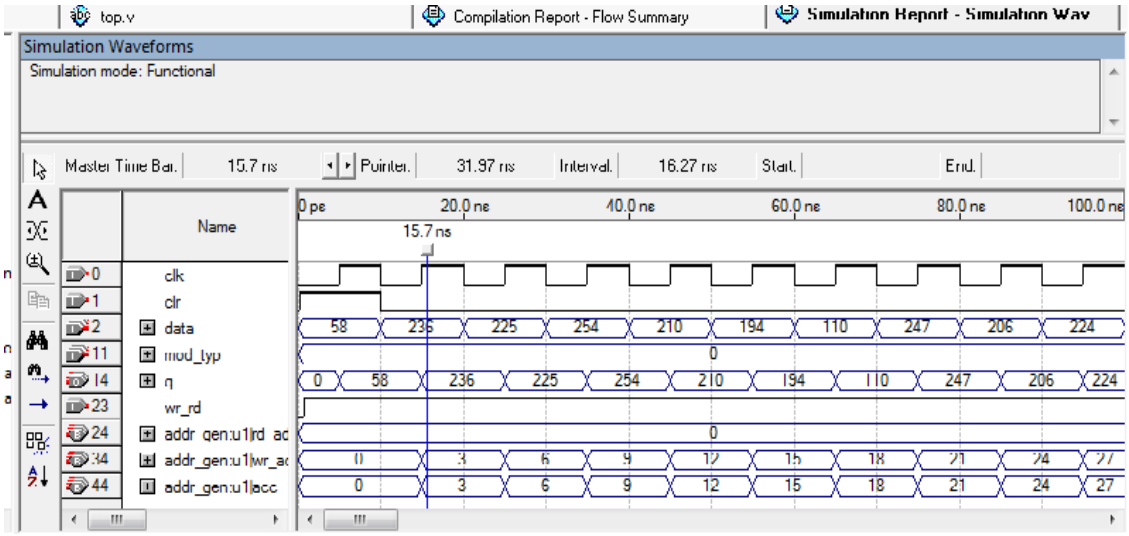

Figure 4: Simulation result of Interleaver