UACEE International Journal of Advancements in Electronics and Electrical Engineering – IJAEEE
Volume 2 : Issue 3 [ISSN 2319 – 7498]
Publication Date : 09 September 2013

Delay Analysis in Carbon Nanotube Bundle Interconnect For VLSI Design

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***Abstract*: This paper proposes to study the performance of carbon nanotube bundle in terms of delay as a VLSI interconnect at 32nm technology node. Output waveform and 90% propagation delay are analytically determined and compared with SPICE simulation result. Alpha power law model is used for representing the transistors of CMOS driver. SPICE simulation result reveals that delay increases with increase in length of interconnect.**

***Keywords*: Carbon Nanotubes, Interconnect, Propagation Delay, L-segment RLC**

I. Introduction

The integrated chips are mostly made of conducting wires, that are called VLSI interconnects. Until 180nm technology node aluminum wires were used as interconnects but as technology scales down aluminum interconnect suffers from electro migration because its current density is very low [1]. Later copper interconnects were preferred over aluminum interconnect because of its high conductivity and high current density. Due to continuous reduction in feature size copper interconnect faced problems of grain boundary effect and electro migration [1-2]. To overcome these problems Carbon Nanotube (CNT) based interconnects are found to be better alternative for copper interconnects at lower technologies [3].

CNTs are formed by rolling up the graphite sheets in the form of cylinder with diameter in the order of a nanometer. Due to its long electron mean free path (in the order of micrometer), CNT has high current density and lower resistivity than copper [4]. CNTs can be either metallic or semiconductor. Metallic CNTs are more attractive interconnects due to their high thermal conductivity [5].

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CNTs are of two types-Single walled Carbon Nanotubes (SWCNT) and Multiwalled Carbon Nanotubes (MWCNT). SWCNT consists of a single graphite sheet in cylindrical form and MWCNT consists of multiple concentric cylinders [6]. SWCNT has large resistance, so it is not a good choice for interconnect. So, a parallel connection of a large number of SWCNTs can be used in which four conducting channels are in parallel. Such SWCNT bundle has lower resistance than Copper interconnect[7].

Interconnect delay is the key factor to determine the performance of a chip. In the past, generally RC delay models were used. Dartu et al. [8] startred with a RC π-model for the timing analysis of RC interconnect. Elmore delay model [9] was used to estimate the signal delay through RC. But at higher frequencies, wire inductance starts to play a role on the chip. So RC model was no longer being adequate and RLC model was proposed. Friedman et al. [10] analyzed the inductance effect on RLC interconnect. An analytical solution for the output waveform for CMOS gate driving RLC line was presented [10]. K Banerjee et al. [11-12] proposed an optimization technique for Lumped RLC interconnect to analyze the effect of line inductance on circuit performance. J A Davis and J D Meindl [13-16] described the transient response of distributed RLC line in which CMOS inverter was replaced by resistor. In this paper simple output voltage models in four different regions are presented to extract output waveform for L segment RLC.

The rest of this paper is given as follows: Section II presents the piecewise transient model while in section III, transient results in all four regions are compared to the SPICE simulation result. The impedance analysis and effect of interconnect length on delay are also observed in section III. Finally section IV draws necessarily conclusion.

II. Piecewise Transient Analysis

A CMOS inverter with L segment RLC circuit of 1mm length of interconnect is shown in fig.1. The alpha-power law model [17] is used to represent the transistor current. The drain current is given in following equation for different regions of operations-

$$I_d = \begin{cases} 0; & V_{GS} \le V_{To}: \text{cut} - \text{off region} \\ k_l(V_{GS} - V_{TO})^{\alpha/2} V_{DS}; & V_{DS} < V_{DSAT}: \text{linear region} \\ k_s(V_{GS} - V_{TO})^{\alpha}; & V_{DS} \ge V_{DSAT}: \text{saturation region} \end{cases}$$

Here α is called velocity saturation index; k_l, k_s are the transconductance parameters in linear and saturation region of the transistor respectively, V_{DSAT} is drain-saturation voltage and V_{To} is threshold voltage at zero bias.

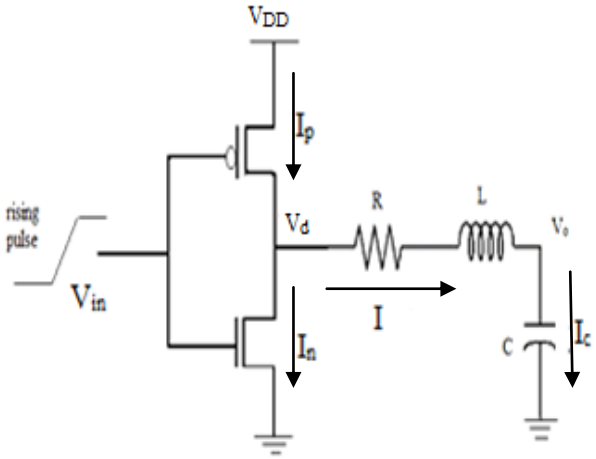

Figure 1. An equivalent model of CMOS gate driving L segment RLC circuit of interconnect.

In this case the analytical expression for output voltage is obtained in different four regions of operations of the transistor for fast input ramp [18].

Applying KCL at drain of nmos-

$$I_n + I - I_p = 0 \qquad (1)$$

An analytical expression for output voltage is calculated for rising input ramp. During rising input ramp, output node is discharged that means nmos transistor will be conducting. So during rising transition, the effect of pmos transistor can be neglected due to short circuit current [17] ($I_p = 0$).

So from equation (1)-

$$I_n + I = 0 \qquad (2)$$

Region 1 ($0<t<t_1$): The nmos transistor is in cut off during this region. This region extends until time t_1, when $V_{GS} = V_{To}$. So putting $I_n = 0$, equation (2) reduces to-

$$I = 0,\ I_c = 0, C\frac{dV_o}{dt} = 0$$

Here initial condition is- $V_o(0) = V_{DD}$

The output V_o remains V_{DD} upto time t_1.

Region 2 ($t_1<t<\tau$): During this region nmos operates in saturation region. Here τ is the rise time of input pulse. The current through nmos transistor during saturation region is given as-

$$I_n = k_s(V_{GS} - V_{To})^{\alpha}$$
$$I_n = k_s\left(\frac{V_{DD}}{\tau}t - V_{To}\right)^{\alpha}$$

From equation (2)-

$$k_s\left(\frac{V_{DD}}{\tau}t - V_{To}\right)^{\alpha} + I = 0$$

$$k_s\left(\frac{V_{DD}}{\tau}t - V_{To}\right)^{\alpha} + C\frac{dV_o}{dt} = 0 \qquad (3)$$

$$\text{here } k_s = \frac{I_{DD}}{(V_{DD} - V_{TH})^{\alpha}}$$

To solve equation (3), the term including α is solved using second order taylor series expansion at $t=\tau/2$ (here $V_{in}=V_{DD}/2$) as-

$$\frac{k_s\left(\frac{V_{DD}}{\tau}t - V_{To}\right)^{\alpha}}{C} = a_o + a_1 t + a_2 t^2$$

So the solution of differential equation (3) is as -

$$V_o(t) = K - a_o t - \frac{a_1}{2}t^2 - \frac{a_2}{3}t^3$$

Here K is integration constant and value of K is calculated using initial condition $V_o(0)=V_{DD}$

Region 3 ($\tau<t<t_2$): At this region the input ramp has reached its final value and nmos transistor is still operates in saturation region. The current through nmos transistor is given as [17]-

$$I_n = k_s(V_{DD} - V_{To})^{\alpha}$$

Now differential equation becomes-

$$C\frac{dV_o}{dt} + k_s(V_{DD} - V_{To})^{\alpha} = 0 \qquad (4)$$

The solution of above differential equation is-

$$V_o(t) = K_1 - K_2 t$$

Here K_1 is integration constant and

$$K_2 = \frac{k_s}{c}(V_{DD} - V_{To})^{\alpha}$$

The nmos transistor exits saturation at time t_2. Time t_2 is calculated by equating drain-source voltage and drain-saturation voltage of nmos transistor [17].

$$V_d(t_2) = V_{DSAT}$$

$$RI + L\frac{dI}{dt} + V_o = V_{DSAT} \quad (5)$$

Here $I = C\frac{dV_o}{dt}$ and $V_{DSAT} = \frac{k_s}{k_l}(V_{GS} - V_{TN})^{\alpha/2}$

Region 4 ($t>t_2$): During this region nmos transistor operates in linear region and current through the transistor is given as-

$$I_n = k_l(V_{DD} - V_{To})^{\alpha/2}V_d$$

Now differential equation becomes-

$$C\frac{dV_o}{dt} + k_l(V_{DD} - V_{To})^{\alpha/2}V_d = 0 \quad (6)$$

Here $V_d = RI + L\frac{dI}{dt} + V_o$

k_l is calculated by $I_{DS} - V_{DS}$ characteristics of transistor and is given as [17]-

$$k_l = \frac{I_{Do}}{V_{Do}(V_{DD} - V_{TH})^{\alpha/2}}$$

Equation (6) becomes-

$$\frac{d^2V_0}{dt^2}\left(LCk_l(V_{DD} - V_{To})^{\alpha/2}\right) + \frac{dV_0}{dt}\left(C + RCk_l(V_{DD} - V_{To})^{\alpha/2}\right) + k_l(V_{DD} - V_{To})^{\alpha/2}V_o = 0$$

So the solution of differential equation (6) is-

$$V_o(t) = 0.45 * \frac{(-K_2*\sqrt{M} - K_2^2 + 4*K_3*K_1)}{-M} e^{-(K_2 - \sqrt{M})t/2*K_1} + 0.45 * \frac{(K_2*\sqrt{M} - K_2^2 + 4*K_3*K_1)}{-M} e^{-(K_2 + \sqrt{M})t/2*K_1}$$

Here

$$K_1 = LCk_l(V_{DD} - V_{To})^{\alpha/2}, K_2 = \left(C + RCk_l(V_{DD} - V_{To})^{\alpha/2}\right)$$
$$K_3 = k_l(V_{DD} - V_{To})^{\alpha/2} \text{ And } M = K_2^2 - 4 * K_3 * K_1$$

III. Results and Discussions

A. *Comparison Of Analytical and Simulation Result*

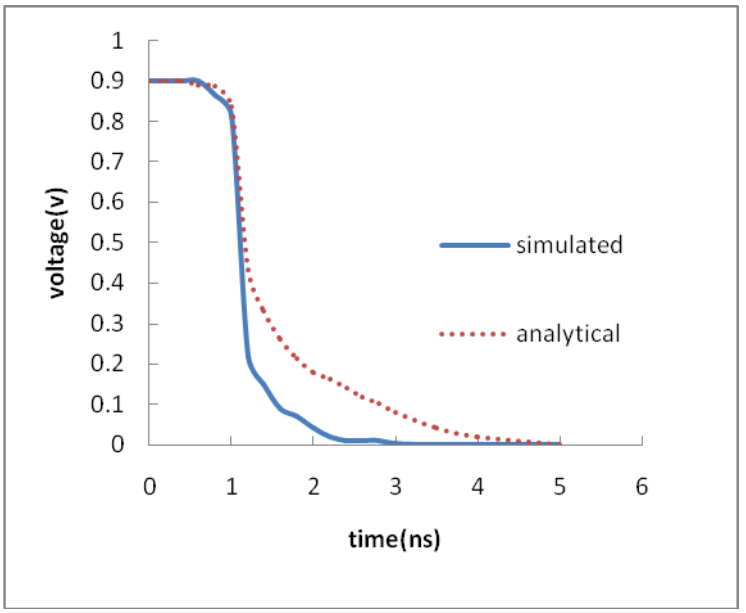

Figure 2. Comparison of analytical and simulated result of L segment RLC line for rising input pulse.

Figure 2 shows the transient response of CNT bundle for 1mm length of interconnect. The above graph reflect the difference between analytical and simulation result of L segment RLC circuit of 1mm length of interconnect.. It is observed that for fast ramp input signal analytical result in terms of output voltage accurately matched with simulation in saturation and some deviation is found in linear region.

B. *Impedance Analysis Of SWCNT Bundle Interconnect*

The effect of impedance parameters (R, L, C) on interconnect length are shown in Fig.3.The circuit impedance parameters are calculated from the models available in [6-7]. Result shows that the value of impedance parameters R, L, C increases with increase in interconnect length as shown in Fig. 3(a), 3(b) and 3(c).

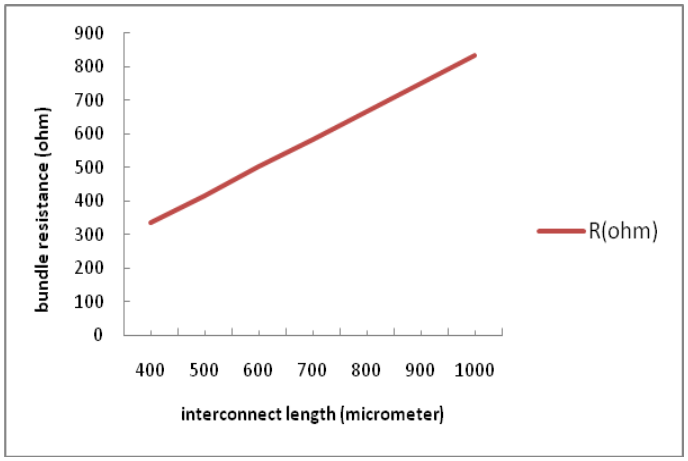

Figure 3 (a). Variation of bundle resistance as a function of interconnect length at 32 nm technology node.

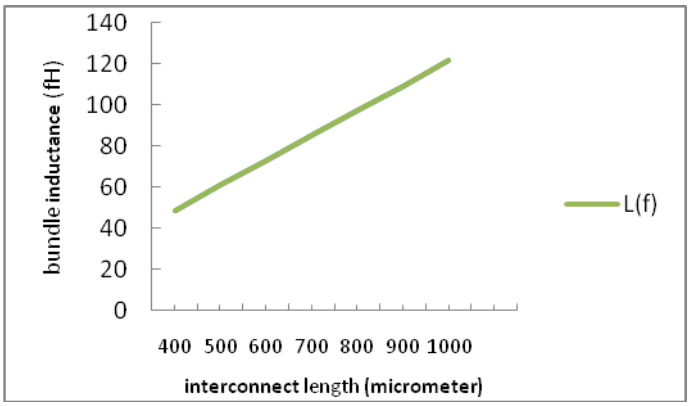

Figure 3 (b). Variation of bundle inductance as a function of interconnect length at 32 nm technology node.

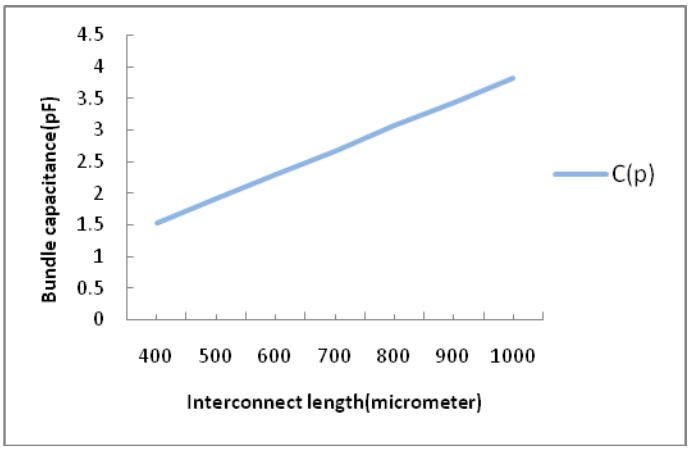

Figure 3 (c). Variation of bundle capacitance as a function of interconnect length at 32 nm technology node.

C. *Effect of interconnect length on bundle SWCNT delay*

The circuit considered for analysis [2,5-7] comprise a CMOS-inverter driving a distributed RLC model of interconnect. A load capacitance of 10fF terminates the interconnect and 0.1Ghz pulse of 1ns rise time provides input to the CMOS inverter. The performance of this setup is studied by SPICE simulation in 32nm technology node with Predictive technology model (PTM)[19] and optimum number of repeaters are used. 90% average delay is illustrated in fig.4 as a function of interconnect length. Result shows that 90% average delay increases with length of interconnect. The variations are simply reflections of the effects of interconnect impedance parameters as shown in figure 3. The increase of normalized delay indicates dominance of CNT resistance over its capacitance. Fig.5 shows the delay as a function of number of repeaters. This result reveals that delay decreases with increase in number of repeaters due to smaller value of RC product in each equal distributed segment of interconnect length.

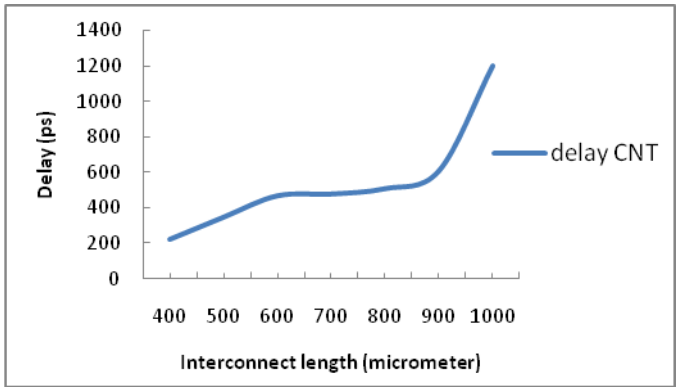

Figure 4. Variation of 90% average delay of SWCNT bundle as a function of interconnect length.

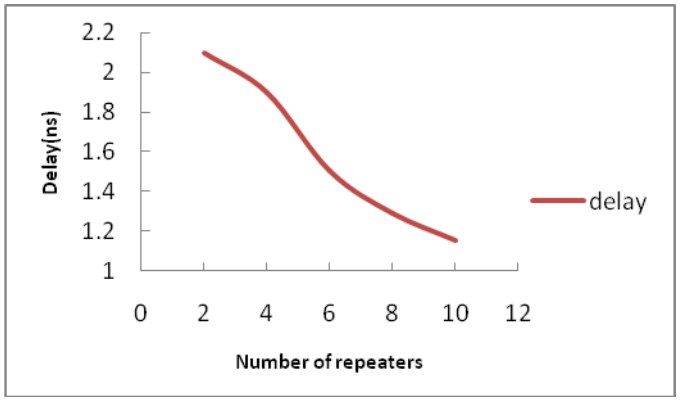

Figure 5.Variation of 90% average delay of SWCNT bundle as a function of number of repeaters.

IV. Conclusion

An analytical model for the calculation of output voltage of an L segment RLC equivalent circuit is presented. Good agreement between analytical and SPICE simulation results is achieved in saturation region. Applying the concept of L-equivalent distributed circuit to SWCNT bundle interconnect the influence of interconnect length and number of repeaters on propagation delay is also analyzed. The analysis shows that 90% delay of SWCNT- bundle interconnect increases with increase in length of interconnect due to the dominance of interconnect impedance parameters. Whereas opposite is true for the repeaters insertion in long interconnects.

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