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Design and Analysis of Domino Logic Circuit for Subthreshold Operation

[Hemant Sharma, Mayank Kumar Rai & Sankar Sarkar]

***Abstract*—This paper presents an equivalent RC delay approach to study the subthreshold operation for inverter and OR logic circuits. The inverter is designed for subthreshold current model, which is exponential in nature instead of using square law model. Based on the inverter the other Domino circuits are designed and various bulk biasing techniques are used. Taking the effect of Miller capacitance, equivalent capacitance is calculated and results of RC delay are compared with SPICE simulation in 32nm technology.**

***Keywords*—Low power, Subthreshold, Dynamic logic circuit.**

I. Introduction

With the reduction in the MOS technology and the growing demand for system portability, the number of devices per chip increase which results in high power consumption. A lot of research has been done on optimizing delay but power reduction is the major design constraint now. One of the approach to reduce power is lowering supply voltages which degrades circuit speed due to reduced transistor currents. So, there is a need of optimizing both delay and power.

With the scaling of devices, the threshold voltage of device is also scaled down so subthreshold operation is now major challenge to designer. Subthreshold currents increase exponentially and many models had been developed which calculate subthreshold current and swing [1].Delay variations are studied and analytically derived for PVT(Process, Voltage and Temperature) variations in subthreshold circuits[2]. Delay models are also being developed for subthreshold regime [3] but these delay modelsare complicated. In [4], the model is derived from direct use of Gaussian law rather than using poison equation. To reduce delay various biasing schemes are used as in [5]. Recent work published in subthreshold design to calculate delay are complicated.

In this paper, a simple model is presented for delay calculation. The effect of all the capacitances of each transistor in domino logic and their equivalent contribution to delay are considered. The rest of paper is organized as follows: Section II presents the design of various bulk biasing techniques. In particular, Section III shows the equivalent output capacitance models in each biasing technique and resistance calculation under subthreshold condition. While in Section IV, results of different biasing circuits are analyzed and compared to the SPICE simulation. Finally, Section V draws necessary conclusion.

Hemant Sharma
ECED, Thapar University,
Patiala, India.
hemant.spray@gmail.com

Mayank Kumar Rai
Asst. professor, ECED , Thapar University,
Patiala, India.
mkrai@thapar.edu

Sankar Sarkar
Ret. Professor,
Department of Electronics & Computer Engineering,
IIT Roorkee, India.
sankarsarkar@gmail.com

II. Design of Bulk Biasing Techniques

Here, domino logic is used and various bulk biasing techniques are applied. The different bulk biasing techniques have effect on the value of threshold voltage and hence provide more flexibility in subthreshold region. The bulk bias is related to threshold voltage by relation

$$V_T = V_{T0} + \gamma\left[\sqrt{|2\varphi + V_{SB}|} - \sqrt{|2\varphi|}\right] \quad (1)$$

The subthreshold operation is analyzed under six bulk biasing techniques [5] viz.
Type1. Bulk of NMOS connected to Gnd and bulk of PMOS connected to supply voltage.
Type2. Bulk of NMOS connected to clock and bulk of PMOS connected to supply voltage.
Type3. Bulk of NMOS connected to Gnd and bulk of PMOS connected to clock.
Type4. Bulk of NMOS and PMOS connected to supply voltage.
Type5. Bulk of NMOS and PMOS connected to Gnd.
Type6. Bulk of NMOS connected to supply voltage and Bulk of PMOS connected to Gnd.

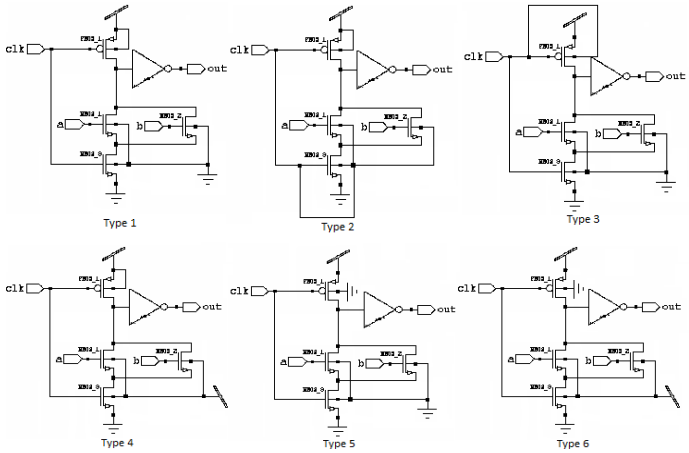

Figure1. Various Bulk Biasing techniques for Domino OR [5].

Based on these biasing Techniques the theoretical model is formed and the equivalent capacitance is calculated.

When the input voltage is below the threshold voltage, the MOS enters into subthreshold region. Subthreshold region is the small region between the point where weak inversion and strong inversion occurs. In this region the current through the drain terminal is exponential function of voltages given by following relation

$$I_{ds} = I_0\left[1 - e^{-V_{ds}/V_t}\right]e^{((V_{gs}-V_{th}-V'_{off})/nV_t)} \quad (2)$$

$$\text{Where, } I_0 = \mu\frac{W}{L}\sqrt{\frac{q\epsilon_{si}(NDEP)}{2\varphi_s}}V_t^{\,2} \quad (3)$$

In the above equation, V_t is the thermal equivalent of voltage, n is DIBL coefficient and V'_{off} is offset voltage. Based on this equation, we design a symmetric inverter and we get following equation.

$$\frac{\mu_n\left(\frac{W}{L}\right)_n}{\mu_p\left(\frac{W}{L}\right)_p}\sqrt{\frac{NDEP_n}{NDEP_p}}e^{(|V_{Tp}|-V_{Tn})/nV_t} = 1 \quad (4)$$

Putting typical values of these parameters, we find$(W/L)_n = 2.1\,(W/L)_p$. On the basis of this inverter the various circuits (static AND, static OR, domino AND and domino OR) for worst case are designed. For static circuits, the symmetric AND gate has $(W/L)_n = 4.2\,(W/L)_p$ and OR gate has $(W/L)_n = 1.905\,(W/L)_p$. Similarly for domino AND (with keeper) has $(W/L)_n = 12.6\,(W/L)_p$ and domino OR (with keeper) has$(W/L)_n = 8.4\,(W/L)_p$. These aspect ratios are used in simulation and result is verified.

III. Parasitic Extractions

A. *Output Capacitance*

In this section the internal capacitances which are charged or discharged during each input are analyzed. Here, inverter circuit is shown in figure 2 and its equivalent output capacitances have been shown in table-1 for various input conditions.

TABLE I. OUTPUT CAPACITANCES OF A INVERTER

V_{in}	C_{out}
0	$C_{gd1} + C_{bd2} + C_{gd2}$
1	$C_{gd1} + C_{bd1} + C_{gd2}$

During a rise time transition the input of a inverter must change from 1 to 0 (as output changes from 0 to 1). In this phase, the output capacitance of both the cases are to be considered as in rising transition. But during discharging or falling input, only those capacitors will be discharged which are charged during previous case (Out=1). The effect of miller capacitance which will be further added to output load capacitance is also taken into account.

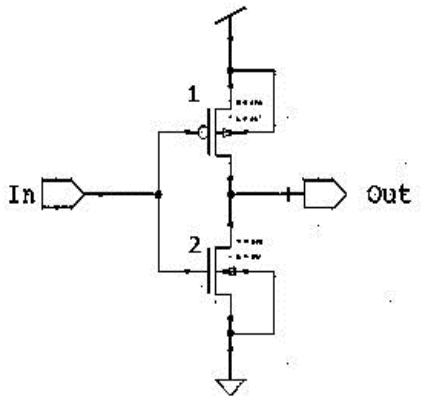

Figure 2. Schematic of an inverter.

B. *Capacitance In Subthreshold Region*

The capacitances strongly influence the gate delay. These parasitic capacitances are even more important in subthreshold. So they have to be considered carefully [6]. The parasitic capacitances are of three types namely junction capacitance C_j , overlap capacitanceC_{ov} , fringing capacitances (inner fringing capacitance $C_{if}$and outer fringing capacitances C_{ofside} ,C_{oftop} ,C_{ofdif}). From [6-7], the capacitances per unit width are modeled by

$$C_{ov} = \frac{\epsilon_{ox}L_{ov}}{t_{ox}} \quad (5)$$

$$C_{if} = 2\epsilon_{si}\ln\left(1 + \frac{X_j}{2t_{ox}}\right) \quad (6)$$

$$C_{ofside} = \epsilon_{ox}\left(\frac{t_{ox}+t_{gate}}{L_{gsd}} - 0.55\right) \quad (7)$$

$$C_{oftop} = \frac{2*0.8\epsilon_{ox}}{\pi}ln\left(1 + \frac{L_g}{2L_{gsd}}\right) \quad (8)$$

$$C_{ofdif} = \frac{0.8\,\epsilon_{ox}}{\pi}ln\left((M^2 - 1)\left(\frac{M^2}{M^2-1}\right)^{M^2}\right) \quad (9)$$

$$C_{BX} = \frac{C_{j*}AX}{\left[1-\frac{v_{BX}}{PB}\right]^{MJ}} + \frac{C_{jsw*}PX}{\left[1-\frac{v_{BX}}{PB}\right]^{MJSW}} \quad (10)$$

$$C_{gdox} = 0.4\,WL_{eff}C_{ox} \quad (11)$$

$$C_{gsox} = 0.6\,WL_{eff}C_{ox} \quad (12)$$

Where, t_{gate} is gate electrode height, X_j is source/drain diffusion depth and L_{gsd} is distance between gate and the source/drain metal electrodes. From the design Rule, we see that$L_g = 2L_{gsd}$. In eqs.(11)and(12), capacitance partition is assumed 40/60. Other parameters are extracted from BSIM 4.0model level 54[8] like, $C_{ov} = 69.576\,pF/m$, $C_{if} = 122.143\,pF/m$, $C_{ofside} = 15.750\,pF/m$, $C_{oftop} = 12.189\,pF/m$, $C_{ofdif} = 50.184\,pF/m$, $C_{gdox} = 590pF/m$

and $C_{gsox} = 896.58pF/m$. The value of the gate to source The available expressions of output capacitance in Table 1are considered for two cases(In=0 and In=1) in the operation of CMOS inverter. Similarly, for domino OR, the output capacitances up till intermediate node(out1) are given in table 2 for specific input transitions.

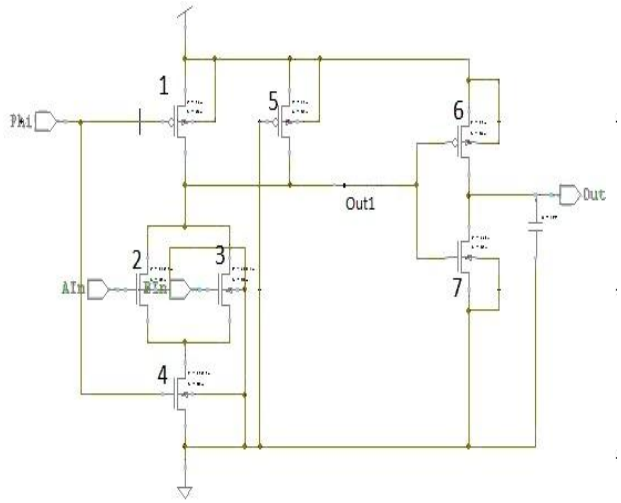

Figure 3. Domino OR type 1.

Out1 is input to inverter, so the Input capacitance (C_{gs}) of inverter is also added to load capacitance at Out1 whose practical value is very small as compared to other capacitance. Here, some of capacitances are connected to nodes which do not give full output swing, so equivalent capacitance on that node will be lesser than these values. Let us assume V_n is the node voltage of a node n and capacitances connected with this node n are C_{n1}, C_{n2} and C_{n3}. So $C_{Total_n} = \frac{V_n}{V_{DD}}(C_{n1} + C_{n2} + C_{n3})$. Moreover, Taking Miller effect into consideration, there is a coupling between input and output (C_{gd}) so net output capacitance will be twice that of coupling capacitance ($2C_{gd}$).

capacitance, $C_{gs} = 1.167\ nF/m$ and $C_{gd} = 0.860nF/m$.

C. *Calculation Of Resistance*

The subthreshold current is of exponential nature so resistance offered by NMOS or PMOS during discharging and charging is very critical. Small change in voltage may change current by many folds. So, here we calculate average resistance offered by the weakly inverted channel which is defined as change in V_{DS}(0 to V_{DD}) by change in current at that V_{DS}.

$$R = \frac{V_{DS}}{\mu\frac{W}{L}\sqrt{\frac{q\epsilon_{si}(NDEP)}{2\varphi_s}}V_t{}^2\left[1-e^{-V_{ds}/V_t}\right]e^{\left((V_{gs}-V_{th}-V'_{off})/nV_t\right)}} \quad (13)$$

By putting values from BSIM model 4.0 [8], the practical value of Average resistance comes out to be $1.388 * 10^5\Omega$ for NMOS of 101nm/32nm and PMOS of 48nm/32nm. This value is very obvious as the $V_{DS}$is of order of a few milli volts and the current is of order of a few nano Amperes.

IV. Results and Discussions

For simulation at 32nm technology node, predictive technology model (PTM)[8] is used and a 0.1GHz pulse of 0.5ns rise time provides input to CMOS inverter with load 1fF. 10 to 90% of rising and falling transition approach of input and output signal is used to calculate average delay. During rise time, all the capacitances (both Out1=0 & 1) are to be considered and during fall time calculations, only capacitances which were charged during previous case and also connected to output are to be considered. These observations are quiet obvious as during transition of output, neither it is complete logic 1 nor logic 0 so we have to take the effect of both the cases during rise time. But when output node is falling, the capacitances charged during previous case(when out=1) are to be discharged.

TABLE II. OUTPUT CAPACITANCE AT OUT1 FOR OR

GATE		A=0, B=1, Out1=0	A=0, B=0, Out1=1
Domino OR	Type 1	$C_{gd1}, C_{bd1}, C_{bd5}, C_{gs3}, C_{gd4}, C_{gd3}$	$C_{gd5}, C_{gd2}, C_{bd2}, C_{bd3}, C_{gd3}$
	Type 2	$C_{gd1}, C_{bd1}, C_{bd5}, C_{bd2}, C_{bd3}, C_{bs3}, C_{gs3}, C_{gd4}$ C_{bd4}, C_{gd3}	$C_{gd5}, C_{gd2}, C_{gd3}$
	Type 3	$C_{gd3}, C_{gd1}, C_{bd1}, C_{bd5}, C_{gs3}, C_{gd4}$	$C_{gd5}, C_{gd2}, C_{bd2}, C_{gd3}, C_{bd3}$
	Type 4	$C_{gd1}, C_{bd1}, C_{bd5}, C_{bd2}, C_{bd3}, C_{gs3}, C_{bs3}, C_{gd4}$, C_{bd4}, C_{gd3}	$C_{gd5}, C_{gd2}, C_{gd3}$
	Type 5	$C_{gd1}, C_{bd5}, C_{gs3}, C_{gd4}, C_{gd3}$	$C_{bd1}, C_{gd5}, C_{gd2}, C_{bd2}, C_{bd3}, C_{gd3}$,
	Type 6	$C_{gd1}, C_{bd5}, C_{bd2}, C_{bd3}, C_{gs3}, C_{bs3}, C_{gd4}$, C_{bd4}, C_{gd3}	$C_{bd1}, C_{gd5}, C_{gd2}, C_{gd3}$
Static OR		$C_{bd2}, C_{gd4}, C_{gd2}$	$C_{gs2}, C_{gd1}, C_{gd2}, C_{gd3}, C_{bd3}, C_{bd4}$, C_{gd4}

The RC delay is calculated and the 90% average delay is given by 2.2RC. OR logic gate circuit (Both domino and static) contains a NOR gate followed by an inverter. So, average delayfor NOR (at out1) is shown in table-3. Table-3 shows that domino OR type 4 has lower value of 90% average delay as compared to other cases. It is due to the fact that net output capacitance during fall time is lowest in Type 4 as shown in table-2.

TABLE III. CALCULATED 90% AVERAGE DELAY AT OUT1

GATE		Average Delay(ps)
Static OR		204.59
Domino OR	Type 1	338.74
	Type 2	327.64
	Type 3	338.65
	Type 4	327.63
	Type 5	411.40
	Type 6	328.64

90% calculated average delay for an inverter is shown in table-4.

TABLE IV. CALCULATED DELAY OF INVERTER WITH LOAD OF 1fF

GATE	Average Delay(ps)
Inverter	397.83

The intermediate output node (Out1) of circuit domino OR type 1 as shown in figure-3 is input to the inverter. Therefore the 90% average delay at Out node is given by

$$TotalRCDelay = \sqrt{(Avg.Inverterdelay)^2 + (Avg.DelayuptoOut1)^2} \quad (14)$$

Analytical and simulated values of 90% average delay and power dissipation are shown in table-5 for different logic circuits. Table 5 reflects simulated delay is minimum for domino OR type 4 which is accurately matched with theoretical value with minimum error. This circuit gives better performance in terms of delay due to smaller value of total output capacitance. In type 4 circuit only gate to drain capacitances are present during fall time of output transition. The type 2 has lower value of power delay product due to less power dissipation as compared to type 4.

Figure 4 shows the analytical and simulated normalized delay for six different OR biased circuits. The average delay is normalized by their respective value of static average delay of OR circuit. Similar approach is used to calculate 90% average delay for other types of biasing circuits as values mentioned in table-5. Results reveal that type 4 circuit gives better performance in terms of delay whereas type 2 has lower power delay product.

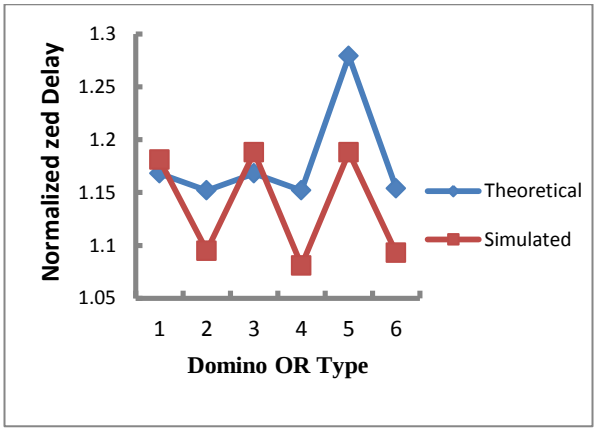

Figure 4. Theoretical & simulated normalized Delay for different Domino OR types.

V. Conclusion

A New RC delay approach for high speed domino OR circuit using six different bulk biasing techniques for subthreshold operation are analyzed. Analytical results are verified by

TABLE V. SIMULATED AND CALCULATED VALUES OF DELAY

GATE		Theoretical RC delay (ps)	Simulated RC delay (ps)	Theoretical normalized delay	Simulated normalized delay	Total power (nW)	Simulated PDP (power delay product) (10^{-18}Ws)
Inverter		397.83	436.59	1	1	10.75	4.691
Static OR		447.35	460.65	1	1	14.81	6.822
Domino OR	Type 1	522.51	544.04	1.168	1.181	113.49	61.743
	Type 2	515.37	504.61	1.152	1.095	114.92	57.989
	Type 3	522.45	547.32	1.168	1.188	112.92	61.803
	Type 4	515.36	498.05	1.152	1.081	119.62	59.577
	Type 5	572.29	547.03	1.279	1.188	113.65	62.169
	Type 6	516.02	503.57	1.154	1.093	119.80	60.328

SPICE simulations. The analytical results are accurately matched with simulated results with minimum error for all circuits. It is found that type 4 circuit has smaller delay as compared to type 2 OR circuit. In terms of power delay product consideration in subthreshold operation, domino OR type 2 is more efficient due to lower value of power delay product.

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About Authors:

Hemant Sharma He received his B-Tech degree in ECE from Jaypee University of Information Technology, Solan, H.P., India. He is currently doing M-Tech in VLSI Design & Auto CAD from Thapar University, Patiala, India. His research interests include Subthreshold logic design & Image processing.

Mayank Kumar Rai He received the B.E degree from M. J. P. Rohilkhan University, Bareilly, India in 2003 and the M.Tech degree from G. G. S. I. P. University, New Delhi, India in 2007. He is currently working towards the Ph.D degree in the department of Electronics and communication engineering, Thapar University, Patiala, India. He has over 11 publications in International referred journals, conferences and one book chapter on VLSI interconnects. He is also working as Assistant professor in the department of Electronics and Communication Engineering, Thapar university, Patiala, India. From 2007 to 2009, he was a faculty with FET, MITS, Lakshmangarh, Rajasthan India. His research interest includes the modeling and design of future VLSI interconnects.

Sankar Sarkar He received his B.Tech. degree in Radio Physics and Electronics and M.Tech. degree in Radio Wave Propagation from Calcutta University in 1968 and 1969, respectively. In 1971, he received the M.Sc. degree in Electrical Engineering from Loughborough University of Technology, UK. He did his Ph.D. from University of Roorkee (now *Indian Institute of Technology, Roorkee*), India. He joined *Indian Institute of Technology, Roorkee* as a Lecturer in 1972, where later he served as Professor. He has over 150 publications in International referred journals(*IEEE, Microelectronics Journal, IET, Physica Status Solidi A etc.*), conferences and two book chapters on VLSI interconnects. He has been Investigator in-charge of several sponsored projects. His present research interests are in the areas of modeling field effect devices, and nanometer-scale issues in high-performance/low-power VLSI design.