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An FPGA implementation of DS-SS communication system using pseudo chaotic sequence generator

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***Abstract*--- Chaotic system are unstable and a-periodic ,making them naturally difficult to identify and to predict .This nonlinear , unstable and a-periodic characteristics of chaotic signals has numerous features that make it attractive for communication use. This field of communication is termed as chaotic communication. Chaotic communication signals have large bandwidth and have low power spectrum density. In chaotic communication, the digital information to be transmitted is placed directly onto a wide band chaotic signal. Spread spectrum is a means of transmission, in which signal occupies bandwidth much more than the one necessary to send the information, the band spread is accomplished by utilizing a code which is independent of data. In this paper an attempt has been made to proposed and analysed the spread spectrum along with the performance analysed of pseudo chaotic code generator implemented in spread spectrum communication system. The sequence generator and the DS-SS for single user are implemented in FPGA as a prototype. The Bit error rate (BER) Performance of the system is evaluated in multi-user environment and reveal that the DS-SS system using pseudo-chaotic sequences as spreading sequences significantly the conventional PN sequences.**

***Keywords*— digital communication, spread spectrum communication, chaotic spreading sequence, chaos**

I. INTRODUCTION

Data security has been a topic of increasing importance in communication as the internet and personal communication system are being made accessible worldwide. In recent years using chaotic signals to address the secure communication problem has received a great deal attenuation. Direct sequence spread spectrum is one of the spread spectrum techniques. Reliability and availability of real time communication are imperative in the context of wireless communication services. A popular techniques used in this is spread spectrum (SS).In SS, the spreading process is accomplished using an spreading code. Conventionally, it is used a pseudo- noise (PN) sequence. These sequences are periodic with a long period and they have properties similar to noise .these properties are interesting when the safety of communication is a requirement of the system [1]. Besides the conventional method of PN periodic sequence generation, others methods can be used in SS system. A promising use of chaotic sequences as spreading codes. A chaotic signal is deterministic, a periodic and presents sensitivity dependence on initial condition and these properties have increased the interest in using chaos in many fields spread Spectrum (SS) has been termed as a means of transmission in which the signal occupies bandwidth much in excess of the minimum necessary to send the information, the band spread is accomplished by utilizing a code which is independent of the data and a synchronized reception with the code at the receiver is used for de-spreading and subsequent data recovery.

The SS Communications are mostly used today for Military, Industrial, Avionics, Scientific, and Civil uses. Spread spectrum techniques for digital communication were originally developed for military applications because of their high security and their susceptibility to interference from other interceptors [4] . Now a day spread spectrum techniques are being used in variety of commercial applications such as mobile and wireless communication. . In order to spread the bandwidth of the transmitting signals, the binary pseudo-noise (PN) sequences have been used extensively in spread spectrum (SS) communication systems. One of the most commonly used PN sequences in DS-SS is maximal length sequences (m-sequences)[5] . The length of m-sequences depends on the number of shift registers. Good correlation properties can be achieved with m-sequences. The ability to predict future sequence is nevertheless possible though difficult. Therefore transmission is not completely secured [7]. The number of sequences generated by Linear Feedback Shift Registers (LFSR) may not be sufficient for wideband DS-SS with a very large number of users. In addition, LFSR techniques provide limited flexibility in incorporating security into multiple user systems [6].The use of chaotic sequences as spreading sequences has been proposed in the literature because of its sensitivity to initial conditions and has characteristics similar to random noise. The pseudo-chaotic sequence generator presented in this paper is the modified version of the generator presented in[6]. The pseudo-chaotic sequence generators presented in and are in the class of Non Linear Feedback Shift Registers (NLFSR). Many authors have

shown that chaotic spreading sequence can be used as an inexpensive alternative to the LFSR sequences such as m-sequences and Gold sequences [10]. The remaining sections of this paper are organized as follows. In section 4 the generation of pseudo- chaotic sequences and their suitability in multiple accesses is described. The FPGA implementation of DS-SS system along with PCS generator is presented in section 5. In section 6 a detailed discussion of the performance of the proposed scheme and some experimental results are presented. The paper is concluded with some remarks in section 7.

II. SPREAD SPECTRUM COMMUNICATION

As a simple, expansion of the bandwidth is insufficient to be termed as the spread spectrum, but the bandwidth expansion must be accomplished with the separate signature. or called as spreading sequence. Both transmitter and receiver know this spreading sequence. It is also independent of the data bits[15]. All the sequences are randomly distributed, and there is no correlation between any two sequences. Let the sequence of data bits x (n) have the period T_{bit} and the spreading sequence of length M. generally called chips to distinguish them from the data bits have the frequency f_{chip} where $f_{chip} >> (1/T_{bit})$. In other words it is assumed that $f_{chip} >> f_{bit}$. From the above assumption that the transmitted data is random and independent, the power spectral density of the original unspread signal is given by [14]

$$S_D(f) = T_{bit}\left(\frac{\sin \pi f T_{bit}}{\pi f T_{bit}}\right)^2$$

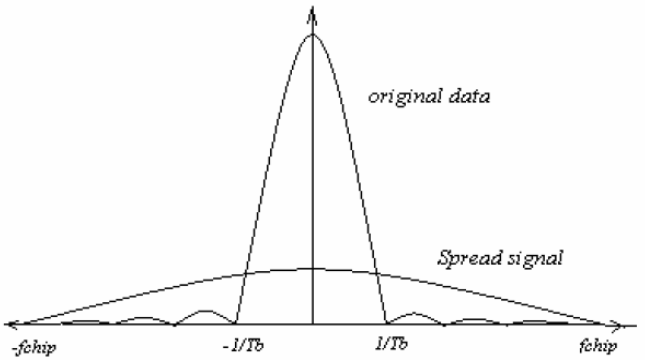

Fig 1. Spread spectrum concept in frequency domain

And assuming that spreading sequence is pseudorandom in nature, and is given by

$$S_{SS}(f) = \frac{1}{f_{chip}}\left(\frac{\sin \pi f/f_{chip}}{\pi f/f_{chip}}\right)^2$$

The relationship between the above spectral densities is sketched in the above Figure. The increased in performance due to the bandwidth expansion and contraction process is known as processing gain g_p .This processing gain can be represented as the ratio of bandwidth associated with the spread signal W_{SS} and that of the data signal W_D .

$$g_p = \frac{W_{ss}}{W_D} = \frac{T_{bit}}{T_{chip}}$$

The processing gain (PG) is normally expressed in decibel form as

$$G_P = 10\ log_{10}(g_p)$$

The SS signal is largely tolerant to external interfering factors, there will be degradation in performance as the number of SS signals in the same cell increases.

To make a good comparison, the background noise is expressed in terms of a modified form of signal to noise ratio (SNR), it takes account the processing gain.

$$\frac{E_b}{N_o} = 10\ log_{10}\left(\frac{g_P}{2\sigma^2}\right)$$

Where E_b/N_0 is the signal to Gaussian noise ratio, and σ^2 is the Gaussian noise variance.

III. DIRECT SEQUENCE SPREAD SPECTRUM TECHNIQUE.

In this paper we will relate only with direct sequence spread spectrum method. In Direct Sequence-Spread Spectrum the base-band waveform is XOR by the PCS sequence in order to spread the signal. After spreading, the signal is modulated and transmitted.

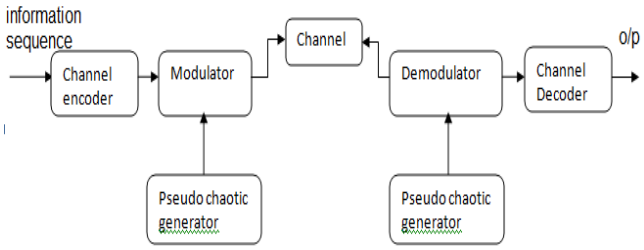

Fig.2.DS-SS block diagram

The bandwidth expansion factor - also known as the Processing Gain (*K*) -, can be defined as the ratio between the transmitted spread spectrum signal bandwidth (*B*) and the bandwidth of the original data sequence (*B message*) where the Processing Gain is the ratio of the spread bandwidth to the information rate *R* (bits/s) and it is much greater than unity.

$$K = \frac{B}{B_{message}} \approx \frac{B}{R}$$

Spread Spectrum transmitters use similar transmits power levels to narrow band transmitters. Because Spread Spectrum signals are so wide, they transmit at a much lower spectral power density, than narrowband transmitters. Spread and narrow band signals can occupy the same band, with little or no interference. Interference rejection capability arises from

low mutual correlation between the desired signal and the interfering signal conformed by the codes. This capability is the main reason for all the interest in Spread Spectrum today. The equation that represents this DS-SS signal is shown in equation.

$$Sss = \sqrt{}(2\ Es/Ts)\ [m(t) \otimes p(t)] \cos(2\ \pi\ fc\ t + \theta)$$

Where:
m(t) - The data sequence,
Ts –The duration of data symbol.
p(t) - The PCS spreading sequence,
fc -The carrier frequency,
θ - The carrier phase angle at t=0.

IV. GENERATION OF PSEUDO-CHAOTIC SEQUENCES.

Pseudo noise (PN) is termed as a coded sequence of 1's and 0's with certain auto-correlation properties [4]. The systems of sequences used in spread spectrum communication are usually periodic in that a sequence of 1's and 0's repeats itself exactly with a known period. The m-sequence represents a commonly used periodic PN sequence. The generated m-sequence is always periodic with a period of $N=2^m-1$ where m indicates is the length of the shift register.

The main focus of this paper is the PCS Generator, which generates a pseudo-chaotic PN sequence with good cross-correlation and auto-correlation properties that is well suitable for DS-SS system. Because of long periodicity, it provides very high security and is capable of handling number of users. It consists of a cascade of four basic cells with two 8-bit programmable registers each. The output of the last cell i.e. each bit of the last cell output are XORed together to obtain pseudo-chaotic sequence and also this bit is feedback to the system to maintain nonlinearity that's we known as(NLFSR). By increasing number of cells and size of the registers, we can increase the number of users and period of the sequence. Since the number of implementation possibilities are very high due to just changing only initial condition programmability, this new method of sequence is inherently more difficult to intercept [6]. each cell consists of two 8-bit registers and a XOR function block. Initial conditions are set to both the registers. The contents of the two registers are XORed (modulo-2 addition) to obtain 8- bit output Cell out, which is used as input to the upper register of the next NLFSR cell. The contents of the two registers are altered for the next iterations by shifting the contents of the lower register towards left. The most significant bit that shifts out of the register is loaded into the least significant bit place of the feedback register of the previous cell. Similarly, the shifted bit from the next cell is moved into most significant bit place of the lower (feedback) register. The contents of the upper register are replaced by the 8-bit output of the previous cell. The PCS generator used in this paper consists of four such cells connected in series as shown in Fig.3.[16]

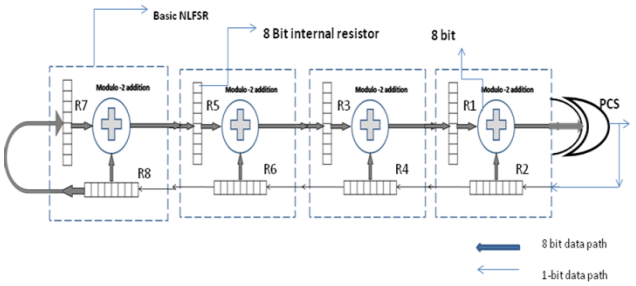

Fig.3.pseudo chaotic sequence generator[16]

The PCS generator contains eight 8-bit registers. These registers provide a total of 64 binary memory elements. Therefore, the PCS generator can be viewed as a sequential state machine with at most 264 possible states. The initial values of these registers can be initialized individually.

V. FPGA IMPLEMENTATION OF DS-SS SYSTEM ALONG WITH PCS GENERATOR.

In this paper, we have replaced the conventional PN sequence by PCS (pseudo-chaotic sequence) for a DS-SS system. The block diagram of the implemented DS-SS system with transmitter and receiver, and inter connection between them is shown in Fig 2. In this fig. shows that channel is the only connection between transmitter and receiver.

A. TRANSMITTER SECTION

In this DS-SS system, we spread the input data bits using Pseudo chaotic sequences which are generated by using PCS generator as mentioned in section 4. To generate PCS sequence, we need to set the 8 bit registers R1 to R8 of PCS generator. To load eight registers of the PCS generator set *load* = 1 and using 3 pins of *sel reg* the corresponding registers R1 to R8 are selected. The 8 bit initial values to each of these 8 registers are loaded using 8 pin *Reg init.* After loading the initial values to all the 8 registers, *Ready out* pin gives an signal to the user. At the same time a signal *ready* is set to high which gives an indication to the control circuit that it can start its operation. Initially before loading the initial values to the registers R1 to R8, the control circuit signals *busy* and *done* are not enabled i.e., *busy* = 1 & *done* = 0. As soon as *ready* = 1, then the signal *busy* = 0.
The tracking and synchronization of the receiver can be done easily by sending first 8 bit data as "00110011". During this condition, the massage source sends a signal in the form of *reload* signal to the control circuit to indicate that it is prepare to send the data. Once this happens the 8 bit data is sent parallel and stored in a buffer register of control circuit in the next clock cycle. After receiving the 8 bit data, the control circuit enables the PCS generator by setting the signal *run = 1*, also enables the multiplier by setting *enable = 1* and indicates the buffer that it is busy by setting the signal *busy = 1.[16]*

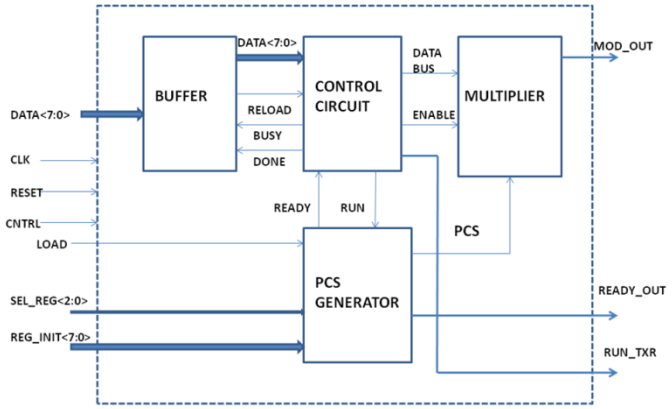

Fig. 4. Block diagram of transmitter[16]

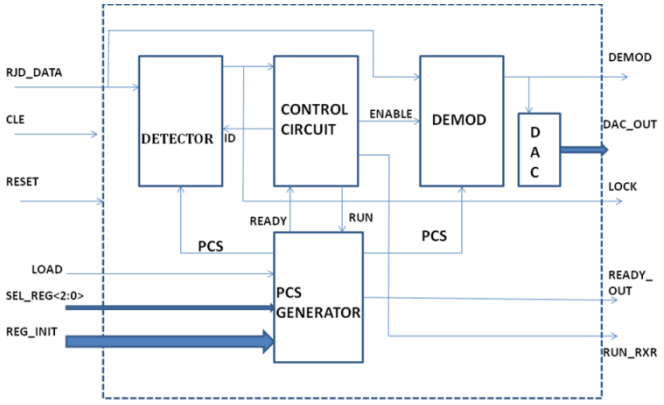

Fig.5. Block diagram of receiver[16]

During this particular time the PCS generator starts generating the 32-bits of PCS sequence. The control circuit then transfers one bit at a time serially to the multiplier where it is multiplied by the 32-bits of generated PCS sequence resulting in a 32-bits of spread sequence and the same is transmitted. After the first data bit is spread by 32-bits of PCS sequence, the second data bit is received in the multiplier and is multiplied by the next 32-bits of the PCS sequence.

Hence the PCS generator generates a total of 256 bits to spread all the 8-bits of data. After transmitting all the 256 bits with respect to one frame of data i.e., 8-bits of data, the control circuit makes signal *done = 1* and *busy = 0*. At that time the control circuit is ready to accept next frame of 8-bits of data. In this way the operation of the transmitter again repeats and maintains the specific gap between the two frames.

B. RECEIVER SECTION

The internal structural block diagram of the receiver is shown in Fig(4)[16] . It consists of detector, control circuit, PCS generator and demodulator. The receiver mainly works in 3 phases: the training phase, the detection phase, and the dispreading phase. Before the training phase, the 8 bit registers R1 to R8 are again set with the same initial values used in the transmitter. This is indicated by setting *ready = 1* by the PCS generator to the control circuit. In the training phase the control circuit keeps the signal *ld = 1* and *enable = 0* and *run = 1*. Now the detector is initialized with a training sequence i.e., the first 256 bits of the PCS sequence are loaded into the 8 lower registers, each with 32-bits of the detector.

In the detection phase, the control circuit resets *ld = 0* and *run = 0*. During this phase the received data of 256 bits are loaded into the upper 8 registers of detector, each register with 32-bits and is compared with the bits which are already stored in the lower 8 registers of the detector.

Upon reaching a certain threshold value, the detector sends a signal *lock = 1* which is sent to the control circuit. The occurrence of the *lock = 1* indicates the end of the detection phase and start of the dispreading phase. The control circuit now sets the signal *enable = 1* and *run = 1* for maintaining the frame gap durations previously considered during the transmission. The control therefore shifts from the detector to the despreader where the incoming wide band data stream is multiplied by the sequence from the local PCS generator; the original narrow band data is obtained at the *demod* data pin and transfer to the DAC (digital to analog convertor).

VI. PERFORMANCE OF THE PROPOSED SCHEME AND EXPERIMENTAL RESULTS.

In this paper the prototype was designed and implemented for a spreading sequence of length 32 bits because of hardware limitations. For practical applications the spreading sequence length can be increased to 1024 bits. Hence the performance of the system can be enhanced by increasing the length of the spreading sequence.

Hence increasing the spreading sequence length from 32 bits to 1024 bits naturally achieves better performance. The BER performance of the PCS system will compared with the PN system and apply error correction method in spread spectrum communication system then later on the autocorrelation properties and cross correlation properties of PCS will compared with the m-sequences and FPGA implementation.

VII. RESULTS.

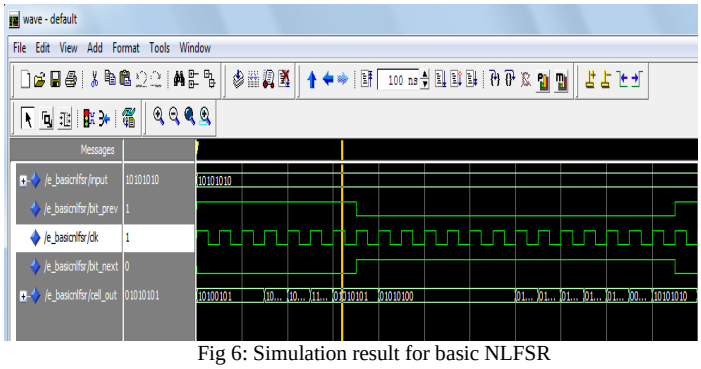

Fig 6: Simulation result for basic NLFSR

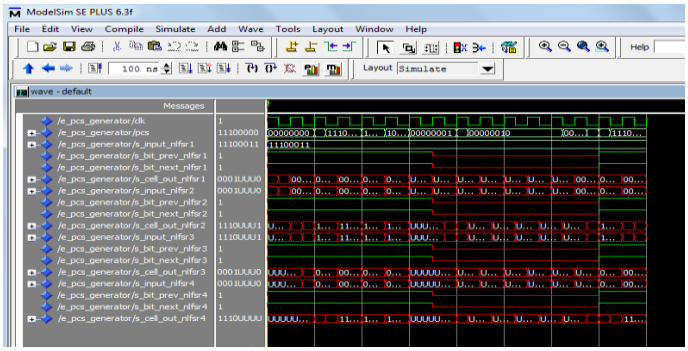

Fig 7: Waveform of PCS sequence generator

Fig 7 shows that at every clock cycle pcs sequence will randomly change.

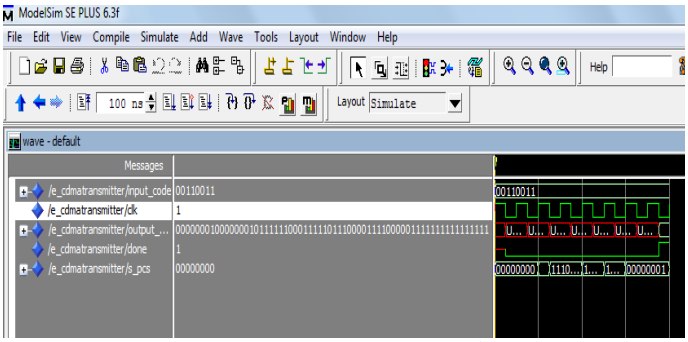

Fig 8: DS-SS Transmitter output waveform.

fig 8 shows that transmitter section of DS-SS communication system ,if consider 8 bit input then first bit of input will xored with pcs sequence then 2nd bit of input will xored with next randomly changed pcs sequence and same procedure will repeat upto 8th bit input then the done signal=1 and we will get 64 bit output.

Fig 9 shows the receiver section of DS-SS communication system under that here we will take 64 bit input which is output of transmitter section.then first eight bit of input of receiver will xored with pcs sequence then we will get first bit of input bit of the tramsmitter then same procedure will followed upto last eight bit input of the receiver and we will get the same origional input of transmitter .

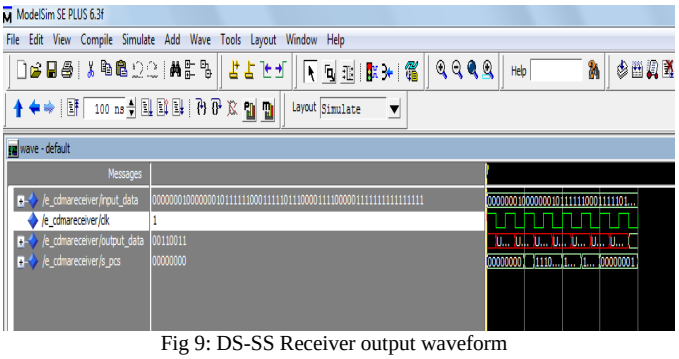

Fig 9: DS-SS Receiver output waveform

VIII. CONCLUSION.

Tests will have shown that simply using random selections of initial conditions can provide pseudo-chaotic sequences that are relatively long with good correlation properties.. And at receiver's side, it has been shown that noise reduction can considerably improves the performance of DS-SS communication. This flexibility provides an additional way of security on top of the inherent low-probability of intercept characteristics of PN sequences due to the difficulty of identify the underlying structure. Therefore the number of implementation possibilities is very high due to changing the initial condition, can be made software controlled and this new system of sequences is more difficult to detect.

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