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Design Of A Delay Block For Low Frequency Switch-capacitor Circuits

[Sandeep Kumar Dash, Bollipelli Srikanth, Ashis Kumar Mal, Rishi Todani]

***Abstract*—Switch-capacitor (SC) circuits are one of the most popular methods for implementing signal processing blocks such as Integrator, Filters, ADC in CMOS technology. This is primarily due to accurate time constant realization over a wide temperature and process corners. Beside good voltage linearity SC circuits occupies less area than continuous time circuits. Non-overlapping clock (NOC) generator is one of the important blocks of any SC circuit. In standard NOC design, simple CMOS inverters are connected in cascade to implement delay blocks. As technology scales, number of inverter increases affecting the area and power budget of the design. In this work, it is proposed to use two numbers of inverted CMOS inverters and one current starved inverter in cascade as a delay block, to achieve a larger delay for a given area. The proposed delay block is used to realize a ring oscillator and a voltage controlled NOC generator. Simulation result shows that proposed delay block exhibits a larger delay than existing standard delay blocks. As frequency of operation is decreased, the proposed delay block is seen to be more and more advantageous in terms of area and power. The designed NOC generator is used to implement a first order SC integrator. The entire work is carried out using GPDK 90 nm technology with 1.2 V supply.**

***Keywords*—Switch-capacitor circuits, delay block, ring oscillator, NOC generator, Switch-capacitor Integrator, GPDK 90nm, Inverted inverter.**

I. Introduction

In analog and mixed signal environment, switch capacitor circuits are one of the popular method for realizing different circuits in CMOS VLSI technology [1]–[3]. Switch-capacitor circuits are extensively used in mixed signal application such as Analog to Digital converters(ADC), Sampled analog architectures, Sigma delta modulators and in analog signal processing block such as Integrator, Comparator and Filters [4]–[8] due to its several advantage over others. The main advantages of switch capacitor circuits are lesser area, better temperature characteristics, higher accuracy of time constants and lower power consumption. In switch capacitor circuits, resistors are replaced by switch-capacitor block consisting of switches and capacitor. This capacitor is charged and discharged by means of a non-overlapping clock. Resistors can be emulated using formula (R =T/C), where R= Resistance, C= capacitance, T= Time period of non-overlapping clock.

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Several techniques are available to realize non-overlapping clock [9]–[11]. One of the standard ways is by using cascade delay blocks with two NAND or NOR gate [3], where delay blocks are implemented using standard CMOS inverters. For low frequency applications such as biomedical signal processing, the number of delay blocks becomes large increasing the area and power requirement. To reduce the number of stages of delay blocks for a given delay, use of transmission gates (TG) between two inverters are also proposed [10]. In this kind of design, the delay of combined block (Inverter + TG) is found to be more than that of two inverters of same size, mainly due to the larger input capacitance seen by the inverter. But the main disadvantage of this delay block is that due to two parallel charging (discharging) paths through NMOS and PMOS combination reduces the delay very much. Another delay block is also proposed to increase the delay using inverted CMOS inverter [12], [13].

In this work it is proposed to use a combination of two inverted CMOS inverters (by changing the position of NMOS and PMOS in CMOS inverter) and a current starved inverter in cascade as a unit delay element. The proposed delay block offers more delay mainly due to cascading inverted inverters. The output signal of inverted inverter is reduced $2V_T$ on both sides. Therefore, the output swing of the Cascaded inverted inverter is nearly equal to V_{DD} - $2V_{Tn}$ to $2V_{Tp}$, assuming input to the inverted inverter is rail to rail. Switching delay of proposed inverter circuit increases, because transistors are not allowed to be in cut off state during input excursion. When input to proposed delay block is high (let V_{DD}), then input to the current starved inverter is V_{DD} - $2V_{Tn}$. So all NMOS transistors are active and experience reduced gate voltage. This reduces the discharging current and thus delay is more than other inverters. Similar logic can be applied for increased delay during charging, that is when input to proposed delay block is logic low.

II. Theory & Analytical Analysis

Proposed delay block is shown in Fig.1. The input is applied to inverted inverter and output is taken from output of current starved inverter. In proposed delay block, inverted inverter is designed by exchanging position of NMOS & PMOS in CMOS inverter. Drain of NMOS in inverted inverter is connected to power supply V_{DD} and only logic high signal can activate this NMOS. Similarly drain of PMOS is connected to ground (gnd) and only logic low signal can activate this PMOS. Inverted inverter can be considered as a pass transistor circuit. In this proposed delay block two number of inverted inverter is cascaded. Hence it will act as a pass transistor in series. So, when input to this cascaded inverted inverter is high, logic 1, then NMOS is active and nearly (V_{DD} - 2V_{Tn}) will be transferred, where V_{Tn} is threshold voltage of NMOS in inverted inverter. Similarly when input to inverted inverter is logic low, then PMOS will be on and nearly (2V_{Tp}) will be transferred to output, where V_{Tp} is threshold voltage of PMOS in inverted inverter. It can be noted that output of cascaded inverted inverter is not rail to rail. This output is fed to input of current starved inverter. Although input to current starved inverter is not rail to rail, but its output will not be affected. It is due to fact that current starved inverter has very good gain (-dVo / dt) > 1 in between input voltage V_{IL} and V_{IH}, where V_{IL} is the maximum input voltage that can be considered as logic low and V_{IH} is minimum input voltage that can be considered as logic high. If input to current starved inverter is in the region, where voltage transfer characteristics (VTC) curve is flat, that is less than V_{IL} and greater than $V_{IH,}$ inverter offers no gain. Hence inverter is capable of restoring input (2V_{Tp}) to (V_{DD} - 2V_{Tn}) to nearly rail to rail output. In proposed delay block current starved inverter is used due to its control voltage. Its control voltage is used to set in such a manner that, input voltage will lie within flat portion of voltage transfer characteristics curve. In proposed delay block Vp is 0.75 V and Vn is 0.275 V. But it is not possible to use more than two inverted inverter in series, because then output of inverted inverter will exceed the region in which output signal can be restored. For GPDK 90nm technology, output of inverted inverter varies from 0.43 V to 0.96 V. For current starved inverter V_{IL} > 0.43 V and V_{IH} < 0.96 V can work perfectly. In proposed delay block, gain region varies from 0.45 V to 0.83 V. It is not possible to cascade more than two inverted inverter, because then V_{IL} and V_{IH} go beyond accepted limit. For GPDK 90 nm technology V_{Tp} and V_{Tn} is approximately 0.15 V.

A. *Cascaded Inverted Inverter Delay*

Generally propagation delay of an inverter is of two types, input to output signal delay during high to low (τ_{iPHL}) and low to high (τ_{iPLH}) transitions of output. By definition, τ_{iPHL} is the time delay between $V_{50\%}$ transition of rising input voltage and $V_{50\%}$ transition of falling output voltage, where $V_{50\%}$ is equal to 0.5 (V_{OH} +V_{OL}). Similarly τ_{iPLH} is defined as the time delay between $V_{50\%}$ transition of falling input voltage and $V_{50\%}$ transition of rising output voltage. So total propagation delay is equals to

$$\tau_{iP} = 0.5(\tau_{iPHL} + \tau_{iPLH}) \tag{1}$$

Principles of pass transistor [14], [15] are used to find-out the behavior of cascaded inverted inverter. So when input to the cascaded inverted inverter is logic high, the NMOS transistor is on and PMOS transistor is off and passes the logic high to output. Thus in logic high transfer, charging of capacitor is done through NMOS. To reduce the complexity of analysis, we neglect the substrate bias effect. So

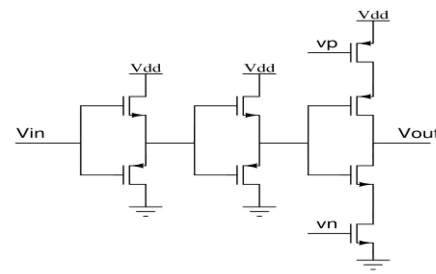

Figure 1. Block diagram of proposed delay block.

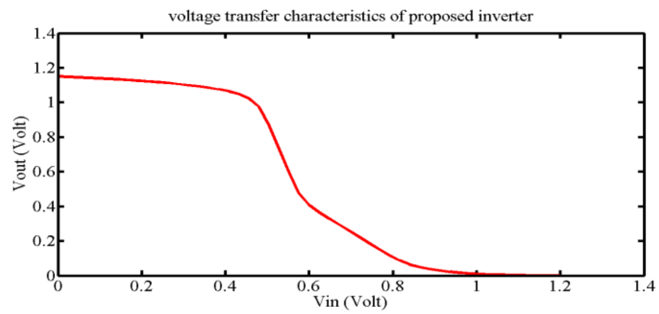

Figure 2. VTC of proposed inverter.

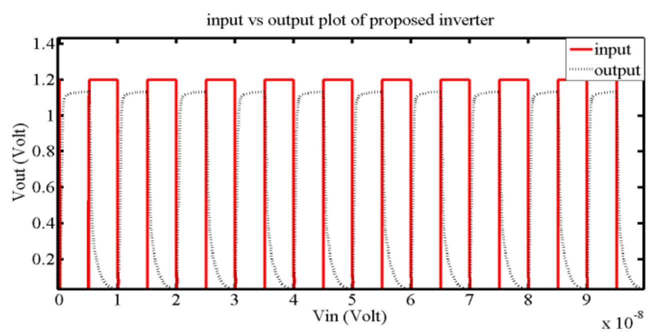

Figure 3. input vs. output plot of proposed delay block.

$$\tau_{iPLH} = \frac{2C_{load}}{K_n}\int_{2V_{Tp}}^{0.5V_{DD}} \frac{dV}{(V_{DD}-V-V_{Tn})^2} \tag{2}$$

$$= \frac{2C_{load}}{K_n}[(\frac{1}{0.5V_{DD}-V_{Tn}}) - (\frac{1}{V_{DD}-2|V_{Tp}|-V_{Tn}})] \tag{3}$$

Similarly during logic 0 transfer PMOS is on and NMOS transistor is off and passes logic low input to output. So high to low delay can be calculated as

$$\tau_{iPHL} = \frac{2C_{load}}{K_p}\int_{V_{DD}-2V_{Tn}}^{0.5V_{DD}} \frac{dV}{(V-|V_{Tp}|)^2} \tag{4}$$

$$= \frac{2C_{load}}{K_p}[(\frac{1}{0.5V_{DD}-|V_{Tp}|}) - (\frac{1}{V_{DD}-|V_{Tp}|-2V_{Tn}})] \tag{5}$$

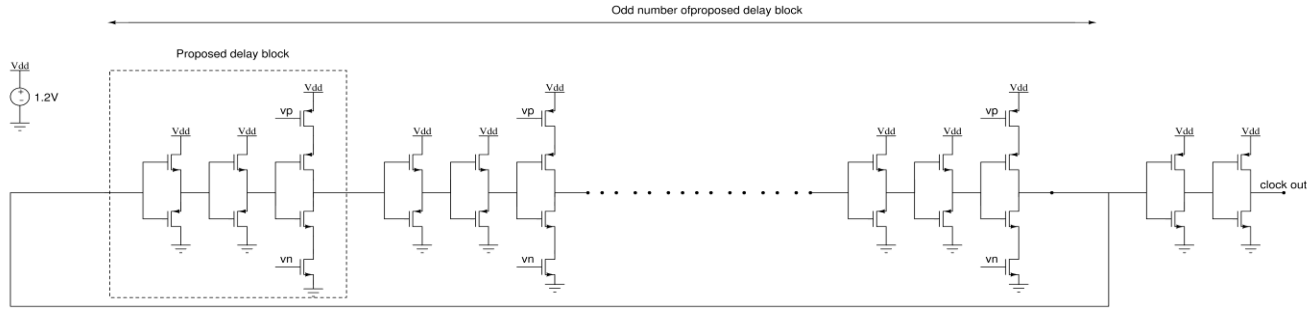

Figure 4: Block diagram of ring oscillator using proposed delay

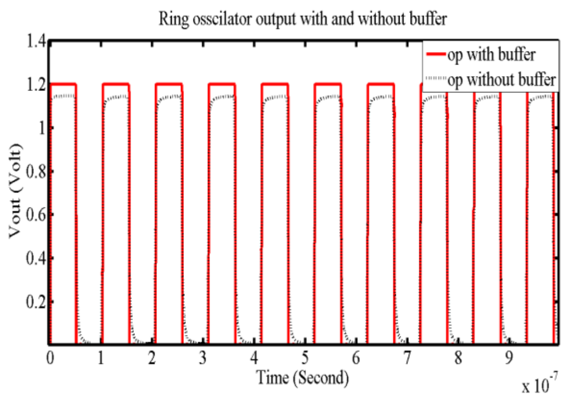

Figure 5. Output of ring oscillator with and without buffer

Using GPDK 90nm technology process parameters with 1.2 V power supply, the delay of inverted inverter is calculated. It is found that τ_{iPHL} = 0.15 ns and τ_{iPLH} = 0.11 ns. Hence average propagation delay becomes 0.13 ns, which is higher as compared to other inverters.

B. *Current Starved Inverter Delay*

Current Starved inverter (CSI) is the modified version of CMOS inverter. In this, middle two transistors act as CMOS inverter and remaining two transistors act as current source/sink. A control voltage is used to appropriately set its VTC such that the input voltage lies in its flat region. The input to CSI is from $2V_{Tp}$ to (V_{DD} - $2V_{Tn}$). When input to CSI is (V_{DD} - $2V_{Tn}$), V_{GS} of top NMOS is equal to ($0.5V_{DD}$ - $2V_{Tn}$) and load discharges through bottom two NMOS transistors in saturation region.

Time period to discharge through load from V_{DD} to V_{DD} - $3V_{Tn}$ is given by t_1.

$$t_1 = -C_{load}\int_{V_{DD}}^{V_{DD}-3V_{Tn}} \frac{1}{i_{Dn}} dV_{out} \quad (6)$$

$$= \frac{8C_{load}V_{Tn}}{K_n(V_{DD}-6V_{Tn})^2} \quad (7)$$

Discharging will continue using above equation, when V_{out} varies from V_{DD} to V_{DD} - $3V_{Tn}$. After that, top NMOS transistor enters linear region. Time period to discharge through load from V_{DD} - $3V_{Tn}$ to $0.5V_{DD}$ is given by t_2.

$$t_2 = -C_{load}\int_{V_{DD}-3V_{Tn}}^{0.5V_{DD}} \frac{1}{i_{Dn}} dV_{out} \quad (8)$$

$$= \frac{2C_{load}}{K_n(V_{DD}-3V_{Tn})} \ln \frac{3V_{DD}}{(7V_{DD}-8V_{Tn})} \quad (9)$$

Total high to low delay can be calculated by adding t_1 and t_2, that is $\tau_{CPLH} = t_1 + t_2$.

$$\tau_{CPHL} = \frac{8C_{load}}{K_n}[\frac{V_{Tn}}{(V_{DD}-6V_{Tn})^2} + \frac{1}{4(V_{DD}-3V_{Tn})} \ln\frac{3V_{DD}}{(7V_{DD}-8V_{Tn})}] \quad (10)$$

Similarly low to high delay is calculated as

$$\tau_{CPLH} = \frac{8C_{load}}{K_p}[\frac{|V_{Tp}|}{(V_{DD}-6|V_{Tp}|)^2} + \frac{1}{4(V_{DD}-3|V_{Tp}|)} \ln\frac{3V_{DD}}{(7V_{DD}-8|V_{Tp}|)}] \quad (11)$$

So total propagation delay of current starved inverter is calculated by adding τ_{CPHL} to τ_{CPLH}. This is given by

$$\tau_{CP} = 0.5(\tau_{CPHL} + \tau_{CPLH}) \quad (12)$$

Using GPDK 90 nm process technology, it is found that τ_{CPLH} = 0.07 ns and τ_{CPHL} = 0.09 ns. So total propagation delay of current starved inverter is 0.08 ns. Thus total propagation delay of proposed delay block is sum of current

TABLE I. COMPARISION OF DELAY

	CMOS Inverter	1 inv. Inverter + CMOS Inverter [12]	Propsed Delay block
Transistor Count	8	8	8
Propagation Delay (τ)	175.43 ps	357.78 ps	4.86 ns

TABLE II. SIMULATION RESULTS OF RING OSCILLATOR USING PROPOSED DELAY BLOCK

Stages	Transistor count	Simulated fosc (MHz)	Duty cycle (%)
5	44	43.56	51.08
13	108	17.05	50.39
21	172	10.60	50.25
29	236	07.69	50.18
37	300	06.03	50.14
45	364	04.96	50.11
53	428	04.21	50.07
61	492	03.66	50.05

TABLE III. COMPARISION OF DIFFERENT RING OSCILLATOR

	CMOS Inverter	1 inv Inverter + CMOS Inverter [12]	Proposed delay block
Transistor count	98	96	92
Frequency (MHz)	861.01	235.59	20.05
I_{dc} (μA)	782.5	377.7	39.51
I_{avg} (μA)	49	138	16.6
P_{dc} (μW)	939	453.24	47.41
P_{avg} (μW)	58.8	165.6	19.92

TABLE IV. AREA & POWER ANALYSIS OF PROPOSED RING OSCILLATOR

	CMOS Inverter	1 inv. Inverter + CMOS inverter [12]	Proposed delay block
Aprox. Frequency (MHz)	20	20	20
Transistor count	4224	1132	92
P_{avg} (μW)	2534.28	1952.42	19.92

TABLE V. PROCESS ANALYSIS OF PROPOSED RING OSCILLATOR

Process	Frequency (MHz)	Duty cycle (%)
SS	12.05	50.39
SF	16.12	50.91
FS	17.71	50.29
TT	20.05	50.45
FF	29.43	50.51

TABLE VI. VOLTAGE ANALYSIS OF PROPOSED RING OSCILLATOR

Voltage (V)	Frequency (MHz)	Duty cycle (%)
1.08	14.55	50.15
1.14	17.26	50.3
1.2	20.05	50.45
1.26	23.11	50.64
1.32	26.26	50.83

TABLE VII. TEMPRATURE ANALYSIS OF PROPOSED RING OSCILLATOR

Temp ($^{\circ}C$)	Frequency (MHz)	Duty cycle (%)
-40	07.31	50.08
-20	11.10	50.22
0	15.03	50.33
20	18.76	50.43
27	20.05	50.45
40	22.13	50.54
60	25.07	50.66
80	27.60	50.78
100	29.75	50.86

Table VIII. COMPARISION OF NOC PERIOD OF DIFFERENT DELAY BLOCK

Number of transistor	T_{NOC} (ns) of 1 inverted + 1 CMOS inverter [12]	T_{NOC} (ns) of proposed delay block
20	0.49	06.95
36	0.85	11.3
52	1.22	15.65
68	1.59	20.05
84	1.97	24.60

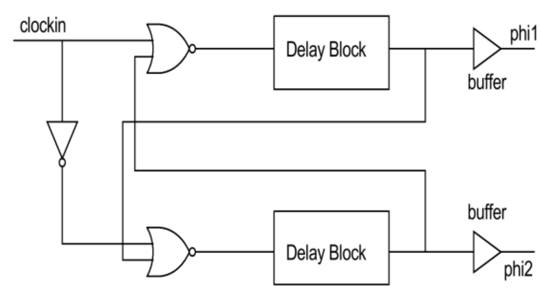

Figure 6. Block diagram of NOC generator

starved inverter propagation delay and inverted inverter propagation delay. This is given by $\tau_P = (\tau_{CP} + \tau_{iP})$. Fig.2 and Fig.3 shows the VTC curve and input vs. output plot of proposed inverter respectively.

III. Simulation Results

This section presents simulation results carried out in Cadence environment using minimum size transistors in GPDK 90 nm technology. Table I shows the delay of proposed delay block is more than delay of four static CMOS inverter in series and other combination [12] using minimum size transistor. So a large delay is obtained using same number of transistors.

Fig. 4 shows block diagram of ring oscillator using odd number of proposed delay blocks. Frequency of ring oscillator is given by

$$f_{osc} = \frac{1}{2n\tau_p} \tag{13}$$

Where τ_P = average propagation delay,

n = number of delay stages connected in series.

This is evident from Fig. 5 that output of ring oscillator is not rail to rail, so two CMOS inverters are added as buffer to make it rail to rail. Table II shows simulation results of proposed ring oscillator. Table III shows comparison of different delay block for power dissipation including voltage reference circuit. Table IV shows comparison for area and power for a given frequency. Table [V]-[VII] shows PVT analysis of proposed delay block.

Traditional NOC generator block diagram is shown in Fig. 6. Proposed delay chain block is used to implement NOC generator. Total non-overlapping period of NOC generator is same as delay produced by delay chain. So, if τ_P is delay of one proposed delay block, then total delay will be given by no of stages times τ_P. So total number of stages required to achieve a given non-overlap period is given by,

$$n = \frac{T_{NOC}}{\tau_p} \tag{14}$$

Fig. 7 shows output of NOC generator using proposed delay block. So it is evident from Table VIII that to achieve higher non-overlap period, lesser area is required in proposed delay block as compared to other standard delay blocks.

Using proposed NOC, a switch capacitor based integrator has been designed as in Fig. 8 for 10 KHz cut off frequency and results are obtained as follows. Fig. 9 and Fig. 10 shows gain and phase plot of integrator and Table VIII shows comparison of non overlapping clock for proposed delay block with other delay block.

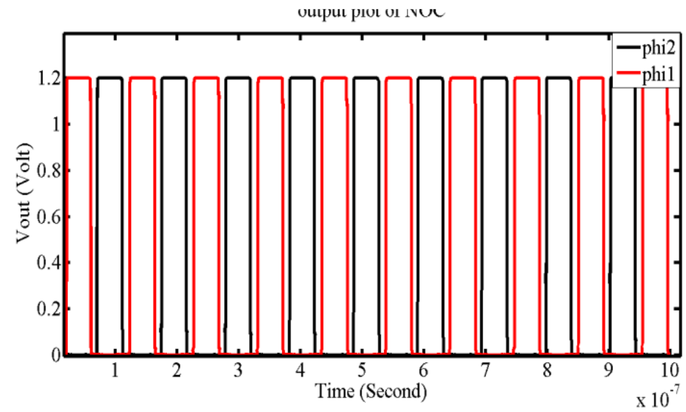

Figure 7. Output of NOC Generator

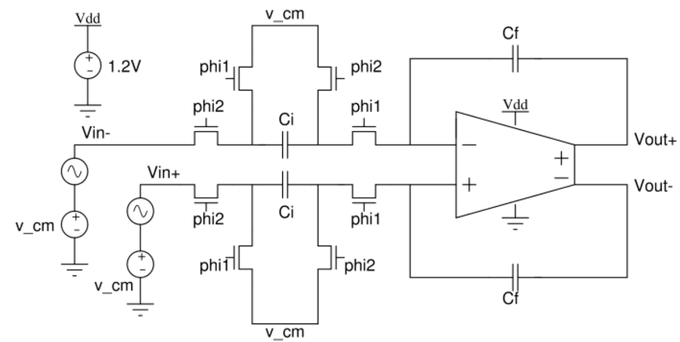

Figure 8. Block diagram of switch capacitor integrator

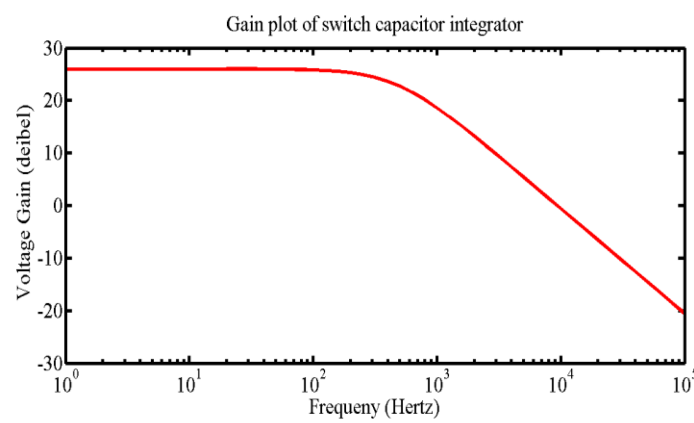

Figure 9. Gain plot of switch capacitor integrator

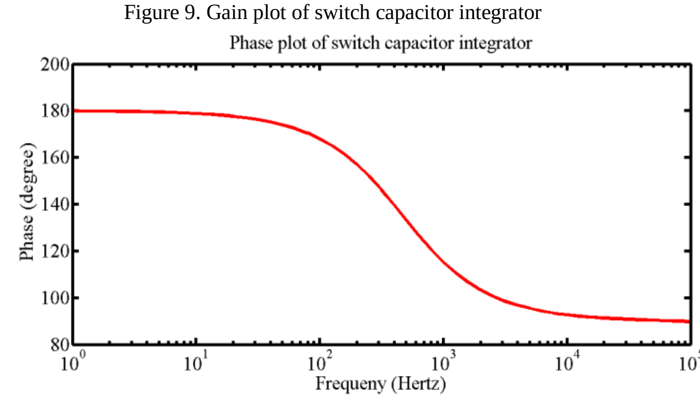

Figure 10. Phase plot of switch capacitor integrator

Conclusion

This paper describes a new inverter circuit, which offer more delay as compared to other inverters. A ring oscillator is designed with the above inverters, which is area and power efficient. Then a two phase Non-overlapping clock generator is designed using above delay circuit in which ring oscillator made of proposed delay block is also used for clock generation. Ring oscillator requires 2 % of area compared to CMOS inverter and 8 % compared to 1 Inv. Inverter + 1 CMOS Inverter. Finally a switch capacitor integrator is designed using above two phase non overlapping clock and simulation results are presented.

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