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Decoupling Capacitor Induced Bandwidth and Delay expressions for On-Chip RLC global interconnects

Santosh Ku Chhotray, Sandeep Ku Dash, Subhakanta Swain, Mrigendra Kumar, Nivedita Rout

***Abstract*— Continuously scaling down devices is the main goal in deep sub-micron (DSM) technology. Though using DSM technology we are achieving many advantages. But circuit performances are badly affected because of secondary effects like crosstalk noise. According to International Technical Roadmap for Semiconductors(ITRS) 2011 report today's DSM technology outsmarted Moore's law to work in a new industrial trend called "More than Moore" (MtM). To accomplish this, it is necessary to analyze the timing behavior of the interconnect. Decoupling capacitor can have significant effect on principal characteristics of an integrated circuit (IC) i.e. speed, cost and power. So by including a decoupling capacitor intentionally can control secondary effects in very deep sub-micron (VDSM) technology. But inserting a decoupling capacitor affects delay and bandwidth of the interconnect. So while inserting decoupling capacitor we have to check for the disturbances in delay and bandwidth. Here in this paper two expressions for calculating delay and bandwidth have derived.**

***Keywords*— Decoupling capacitor, interconnects, Bandwidth, Delay**

I. Introduction

An electronic system consists of 2 parts: the basic components (transistor, diode, passive circuit elements, MEMS etc.) and the highly complex interconnect fabric linking them(from local to global in a hierarchical manner). As global interconnects are responsible for power supply, so any disturbance in global interconnect can effect a lot to signal propagation along it and the victim (idle) interconnect. Circuit integration densities rise with each very deep sub-micron (VDSM) due to smaller devices and larger dies. By using VDSM technology we are achieving many advantages. Again to handle high speed and low power in VDSM technology we intentionally add decoupling capacitors to interconnect line. But these decoupling capacitors show some unexpected results because of secondary effects like crosstalk noise. Because of crosstalk functional and timing problems arises like delay, bandwidth etc. Several factors bound to VDSM technology like density of integration, no. of metal layers etc are reason behind these unexpected outcomes. RC modelling is not enough for global interconnection at high frequencies. Working in VDSM technology we cannot ignore wire resistances, capacitances and inductances. So to handle this two-fold nature of VDSM technology here in our proposed model we focus on global interconnects where we consider wire resistances, inductances and practical decoupling capacitances. The timing parameters like propagation delay and bandwidth depends on power supply level during the signal transition. Various techniques have been proposed for the delay analysis of global interconnects. Here in this paper the crosstalk effects because of capacitive coupling and inductive coupling are considered on different nodes of global interconnects. Then using derived expression delay and bandwidths are calculated and compared with 180nm HSpice technology.

II. Decoupling capacitor effects

Decoupling capacitors are often utilized to manage the power supply noise. Due to importance of decoupling capacitors in current and future ICs, significant research has been developed over past several decades. To be effective, the decoupling capacitor should satisfy two requirements. First, the capacitor should have sufficient capacitance to store a significant amount of energy. Second, to supply sufficient power at high frequency, the capacitor should be able to release and accumulate energy at high rate.

III. Proposed Model

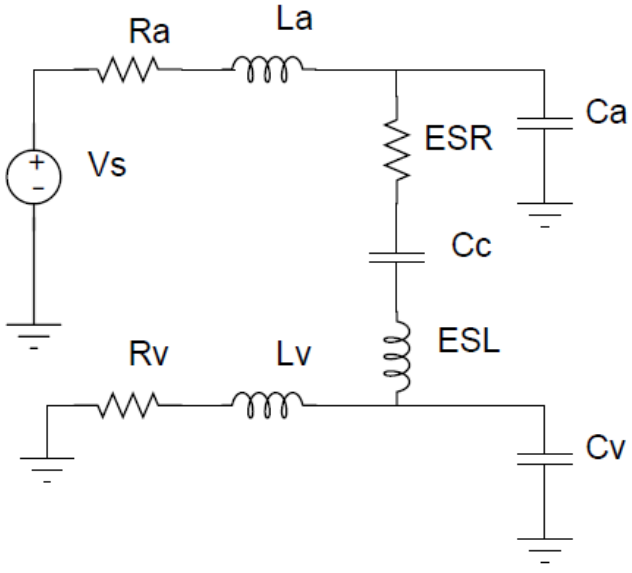

Figure 1 Proposed model with decoupling capacitor

Above figure shows two interconnect lines connected by a decoupling capacitor. At high frequency as the frequency increases, the impedance of the decoupling capacitor increases linearly with frequency as shown in fig. 2. This increase in the impedance of a practical decoupling capacitance is due to the

parasitic inductance of the decoupling capacitor. The parasitic inductance is referred to as the Effective Series Inductance (ESL) . The impedance of a decoupling capacitor reaches minimum impedance at frequency $\omega = 1/\sqrt{LC}$ to get negligible disturbance in delay and bandwidth. Effective Series Resistance (ESR) of a decoupling capacitor is the minimum impedance of the decoupling capacitor.

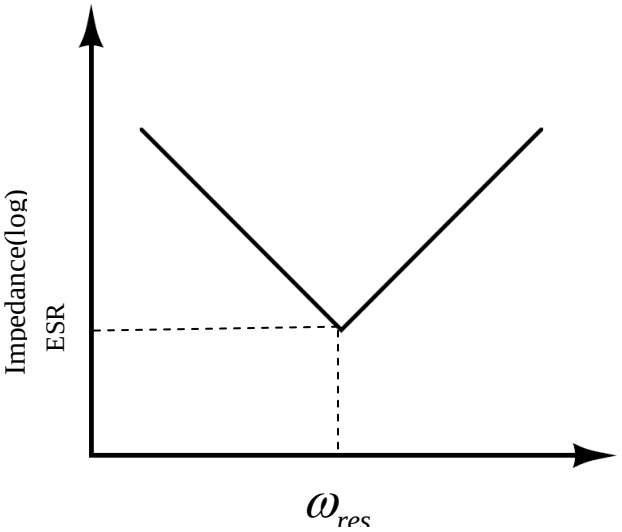

Figure 2 Frequency Vs Impedance plot for high frequency interconnect

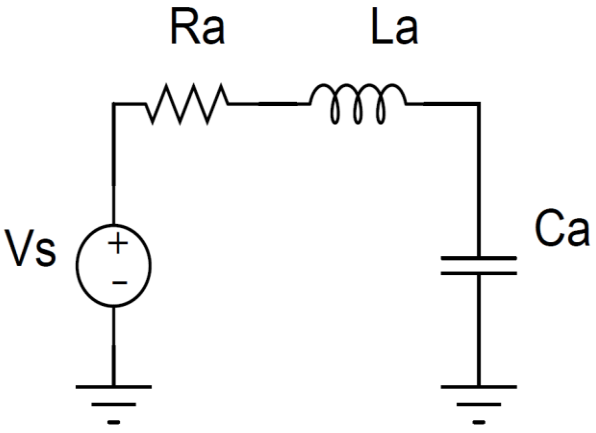

Figure 3 Equivalent model of aggressor line

Proposed estimation method separates the victim (idle) net and the aggressor net into two equivalent circuits. The aggressor is modeled as shown in Fig. 3 and victim line is modeled as shown in Fig. 4.

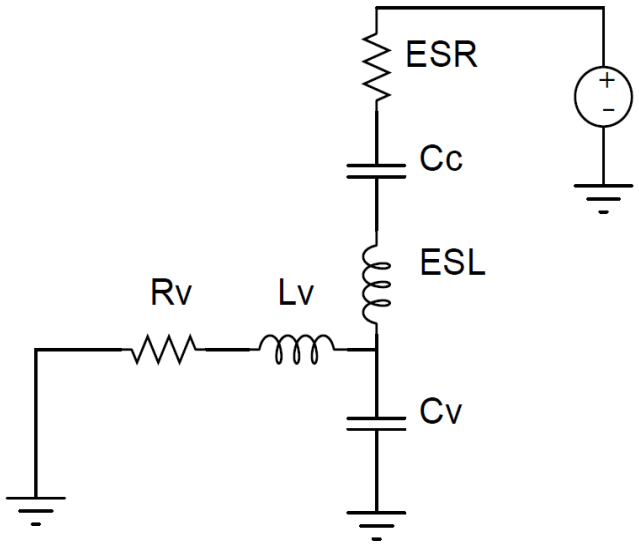

Figure 4 Equivalent model of victim line

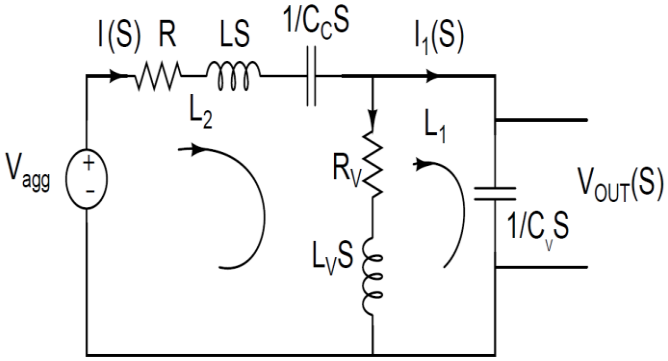

Figure 5 Equivalent circuit

A. *Bandwidth Calculation*

$$V_{agg}(t) = \begin{cases} \frac{t}{\tau_a} V_{dd} & 0 < t < \tau_a \\ V_{dd} & t > \tau_a \end{cases} \quad (1)$$

It can be represented in S-domain as

$$V_{agg}(s) = \frac{1}{s^2 \tau_a} V_{dd} \quad (2)$$

Here for simplicity we have taken V_{dd}=1.

Proposed model is based on the above circuit shown in Fig. 5. Figure represents victim line parameters and V_{out}(S) is the coupled voltage of decoupling capacitor.

Now applying KVL to loop L_1

$$-\frac{I_1}{C_V S}+L_V S(I-I_1)+R_V(I-I_1)=0$$

$$(\frac{1}{C_V S}+L_V S+R_V)I_1=I(L_V S+R_V)$$

$$I=\frac{(\frac{1}{C_V S}+L_V S+R_V)I_1}{(L_V S+R_V)} \quad (3)$$

Now applying KVL to loop L_2

$$V_{agg}(S)-RI-LSI-\frac{I}{C_C S}-R_V(I-I_1)-L_V S(I-I_1)=0$$

$$V_{agg}(S)-I(R+LS+\frac{1}{C_C S}+R_V+L_V S)+(L_V S+R_V)I_1=0$$

Now using (3)

$$V_{agg}(S)=\frac{(\frac{1}{C_V S}+L_V S+R_V)I_1}{(L_V S+R_V)}(R+LS+\frac{1}{C_C S}+R_V+L_V S)+(L_V S+R_V)I_1$$

Now simplifying above equation

$$I_1(S)=\frac{V_{agg}C_C S(L_V C_V S^2+R_V C_V S)}{\left[\begin{array}{l}C_V S(L_V C_V S^2+R_V C_V S+1)(RC_C S+R_V C_C S+LC_C S^2+L_V C_C S^2)\\-(R_V+C_V S)(L_V C_V S^2+R_V C_V S)C_C S\end{array}\right]} \quad (4)$$

$$V_{out}(S)=\frac{I_1}{C_V S} \quad (5)$$

Now using (4) in (5) and rearranging

$$\frac{V_{out}(S)}{V_{agg}(S)}=\frac{C_C S(L_V C_V S^2+R_V C_V S)}{\left[\begin{array}{l}C_V S(L_V C_V S^2+R_V C_V S+1)(RC_C S+R_V C_C S+LC_C S^2+L_V C_C S^2)\\-(R_V+C_V S)(L_V C_V S^2+R_V C_V S)C_C S\end{array}\right]}$$

Considering dominating pole and ignoring higher order terms

$$\frac{V_{out}(S)}{V_{agg}(S)}=\frac{jC_C L_V C_V\omega+R_V C_V C_C}{RC_V C_C+R_V C_V C_C}$$

Applying modulus on both sides and equating to $\frac{1}{\sqrt{2}}$

$$\frac{1}{\sqrt{2}}=\frac{\sqrt{(C_C L_V C_V\omega)^2+(R_V C_V C_C)^2}}{RC_V C_C+R_V C_V C_C}$$

$$\omega^2=\frac{1}{\left(\frac{RC_V C_C+R_V C_V C_C}{\sqrt{2}C_C L_V C_V}\right)^2-\left(\frac{R_V C_V C_C}{C_C L_V C_V}\right)^2}$$

$$\omega=\frac{1}{\sqrt{\left(\frac{RC_V+R_V C_V}{\sqrt{2}L_V C_V}\right)^2-\left(\frac{R_V}{L_V}\right)^2}}$$

$$f_{3dB}=\frac{1}{2\pi\sqrt{\left(\frac{RC_V+R_V C_V}{\sqrt{2}L_V C_V}\right)^2-\left(\frac{R_V}{L_V}\right)^2}} \quad (6)$$

B. *Delay Calculation*

For calculation of delay we consider 50% rise time when $V_{out}(t)=0.5V_{dd}$

From (5) we can get delay expression as

$$V_{out}(S)=\frac{\frac{V_{dd}}{s^2\tau_a}C_C S(L_V C_V S^2+R_V C_V S)}{\left[\begin{array}{l}C_V S(L_V C_V S^2+R_V C_V S+1)(RC_C S+R_V C_C S+LC_C S^2+L_V C_C S^2)\\-(R_V+C_V S)(L_V C_V S^2+R_V C_V S)C_C S\end{array}\right]} \quad (7)$$

Now for delay calculation equating $V_{out}(t)=0.5V_{dd}$

$$V_{out}(S)=\frac{0.5V_{dd}}{S}$$

Using above value in (7)

$$\frac{0.5V_{dd}}{S}=\frac{\frac{V_{dd}}{s^2\tau_a}C_C S(L_V C_V S^2+R_V C_V S)}{\left[\begin{array}{l}C_V S(L_V C_V S^2+R_V C_V S+1)(RC_C S+R_V C_C S+LC_C S^2+L_V C_C S^2)\\-(R_V+C_V S)(L_V C_V S^2+R_V C_V S)C_C S\end{array}\right]}$$

Now taking inverse Laplace transform and solving

$$t_{50\%}=1.18*\sqrt{3X^2-2Y}$$

Where

$$X=R(C_V+C_C)+R_V C_V-\frac{R_V}{L_V}$$

And

$$Y=RR_V C_V C_C+\frac{R_V{}^2 C_C}{L_V}-\frac{R^2 C_V}{L_V}$$

IV. Simulation Result and Discussion

Our experimented high-speed interconnect system consist of two coupled interconnect lines of length d=100 um. The extracted values for the parameters R, L, and C are given in Table 1.

Table I
RLC Parameters for a Minimum- Sized Wires in a 0.18μm Technology

Parameter(s)	Value/m
Resistance(R)	120 kΩ/m
Inductance(L)	270 nH/m
Coupling Capacitance(C_c)	681.23pF/m
Capacitance(C)	240 pF/m

Table-II compares the bandwidth we got by proposed model with the values from SPICE simulator for different source resistances. With the varying source resistance we got different values of bandwidth with approximately 3.881% of error.

Table II
Bandwidth comparison of proposed model with SPICE model

R_s(Ω)	L_s(pH)	C_c(pF)	SPICE Bandwidth (MHz)	Proposed Model (MHz)	% Error
45	2.5	0.175	99.74	105.13	5.4040
95	2.5	0.175	147.64	154.43	4.5990
445	2.5	0.175	245.72	252.71	2.8447
995	2.5	0.175	295.9	303.82	2.6765

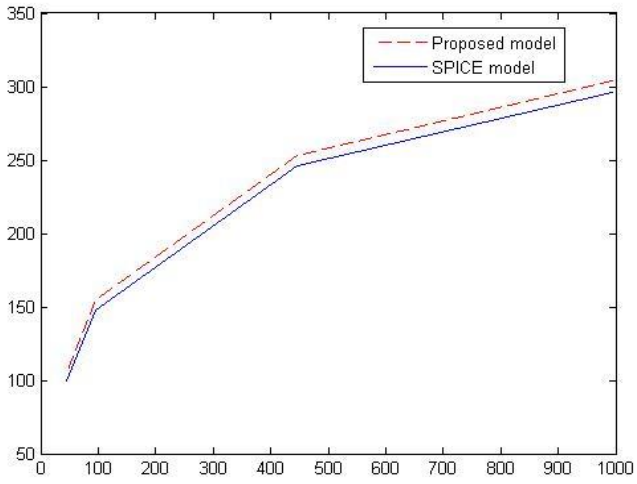

Figure 6 Bandwidth comparison of proposed model with SPICE model

Fig.5 shows the deviation of bandwidth using derived expression from SPICE simulator and Fig. 7 shows the deviation of delay using derived expression from SPICE simulator

Table-III compares the delay we got using derived expression with SPICE simulator values and the average percentage of error is about 0.5499%.

Table III
Delay comparison of Proposed model with SPICE model

R_s(Ω)	L_s(pH)	C_c(pF)	SPICE Delay(ps)	Proposed Model(ps)	% Error
45	2.5	0.175	20.14	20.05	0.4468
95	2.5	0.175	41.55	41.35	0.4813
445	2.5	0.175	221.36	220.03	0.6008
995	2.5	0.175	465.13	462.01	0.6707

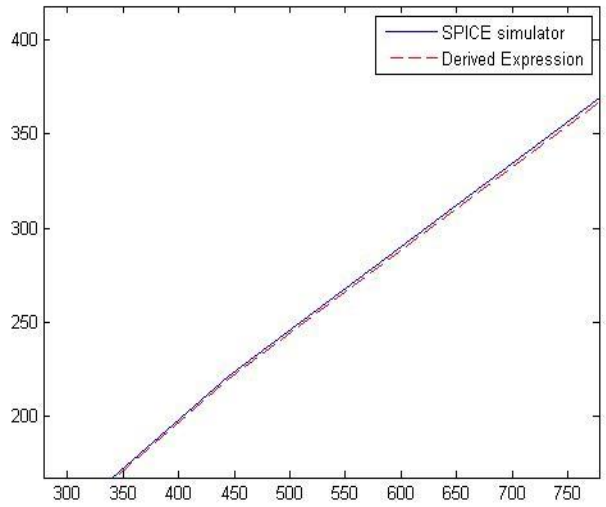

Figure 7 Delay comparison of proposed model with SPICE model

V. Conclusion

In this study simple and explicit analytical expressions have been proposed for calculating delay and bandwidth for global interconnects in very deep sub-micron (VDSM) technology where we consider decoupling capacitors for controlling signal timing behavior. It is expected that these expressions will also applicable to 90nm and 45nm technology and to be used efficiently in high speed and large scale circuits. Hence these closed form expressions can be implemented in VLSI design tool for efficient modeling of interconnection in high speed VLSI chips. These analytical delay formulas are much faster than simulating using SPICE. So can save time and of course the cost of using expensive tools like SPICE. In future we will try to simplify these equations to simpler form as possible.

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About Author (s):

Santosh Kumar Chhotray received B.Tech from BPUT, Orissa and continuing M.Tech in the specialization of Microelectronics and VLSI in National Insti. Of Technology, Durgapur, West Bengal, India.
For last 1 year he has performed research in the areas of IC interconnect characterization, modeling and simulation for the high speed and low power application. His research interests are high speed and low power SRAM design, interconnect modeling.

Sandeep Kumar Dash received B.Tech from BPUT, Orissa in 2010. And continuing his M.Tech in the specialization of Microelectronics and VLSI in National Insti. Of Technology, Durgapur, WestBengal,India..
He has performed research in the areas of ideal Op-Amp characterization for the high speed application. His research interests are filter design, Mixed signal IC design for low power application.

Subhakanta Swain received B.Tech from BPUT, Orissa in 2010. And continuing his M.Tech in Sikhsa 'O' Anushandhan University, Bhubaneswar, Orissa, India.
He has performed research in the areas of Wireless multimedia sensor networks. His core area of research is Priority-based rate control for service differentiation and congestion control in Wireless multimedia sensor networks.

Mrigendra Kumar received B.Tech from WBUT, Kolkata in 2012. He is doing research in VLSI system modeling. His area of interests are control system, signal processing and VLSI interconnections.

Nivedita Rout received B.Tech from BPUT, Orissa in 2012. She is working as teaching assistant in Aryan Insti. Of Technology and working on power issues related to VLSI circuits. Her core area of research are Automated access of information and fast data tracking.