UACEE International Journal of Advancements in Electronics and Electrical Engineering – IJAEEE
Volume 2 : Issue 2 [ISSN 2319 – 7498]
Publication Date : 05 June 2013

"FPGA BASED SINGLE PHASE MULTILEVEL INVERTER"

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Abstract-

The application of Field programmable Gate Array(FPGA) in the development of electronics circuit control scheme has drawn much attention lately due to its shorter design cycle, lower cost and higher density. This paper presents an FPGA based gate signal generator for single phase multilevel inverter employing an sinusoidal PWM switching strategy to control its output voltage. The XILINX FPGA based single phase multilevel PWM inverter was constructed by adding a bi-directional switches to the conventional bridge topology. The inverter can produce three and five different output voltage levels across the load. FPGA is chosen for the hardware implementation of switching strategy mainly due to its high computation speed that can ensure the accuracy of the instants that gating signals are generated. VHDL language is used to model the inverter switching strategies The PWM pulses was downloaded in FPGA(XC3S400PQ208) from Spartan 3. In addition to FPGA, Xilinx/modelsim software was used for simulation and verification of the proposed circuit before implementation. Simulation results are obtained which will be compared with the experimental results.

Keywords:

Field programmable Gate Array, Field programmable Gate Array and PWM switching strategy

I. INTRODUCTION

Multilevel inverters have been attracting increasing attention in the past few years as power converters of choice in many applications. They have significant advantages over the conventional one because of the capability to reduce the undesirable harmonics in order to improve the performance and efficiency.It may be easier to produce a high power and high voltage inverter with multilevel structure because of the way in which device voltage stresses are controlled in structure. Increasing the no of voltage levels in the inverter without requiring higher rating on individual devices can increase the power rating. A multilevel inverter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, dv/dt stresses, and stresses in the bearings of a motor.

Several multilevel inverter topologies have been developed; i) diode clamped, ii) flying capacitors, and iii) cascaded or H-bridge. The H-bridge inverter eliminates the excessively large number of (i) bulky transformers required by conventional multilevel inverters, (ii) clamping diodes required by multilevel diode-clamped inverters, and (iii) flying capacitors required by multilevel flying-capacitor inverter which are the drawbacks of these topologies. In 1998-99 , the proposed cascaded multilevel inverter (CMI) with separated DC sources is clearly the most feasible topology for use as a power inverter for medium & high power applications due to their modularization and extensibility.

For the generation of PWM signal microcontroller can also be used but it has lots of hierarchical rules and commands over its input and output. Microprocessor can perform loops, timings, conditioned branching, and calculations like a small PC under program control they are used where the operation is relatively complex but processing speed relatively less than FPGA. FPGA is only an array of gate that can be connected as the user wishes. FPGA are used for relatively simpler operations but higher processing speed in comparison to microcontrollers. Field Programmable Gate Array (FPGA) offers the most preferred way of designing PWM Generator for Power Converter Applications. They are basically interconnection between different logic blocks. When design is implemented on FPGA they are designed in such a way that they can be easily modified if any need arise in future. We have to just change the interconnection between these logic blocks. This feature of reprogramming capability of FPGA makes it suitable to make your design using FPGA. Also using FPGA we can implement design within a short time and efficient hardware for rapid prototyping. Thus FPGA is the best way of designing digital PWM Generators. Also implementation of FPGA-based control schemes proves less costly and hence they are economically suitable for small designs.

This paper presents a multilevel PWM inverter whose output voltage maybe has three or five levels based on modulation index used. Xilinx Web Pack software 8.1 is used to generate PWM pattern by means of VHDL programs. The final design is implemented on Xilinx **FPGA** (XC3S400PQ208) from Spartan 3.

II. Proposed Block Diagram

The block diagram of the proposed work is shown in figure 1.The Sinusoidal PWM technique is used for the pulse generation. The carrier signal which is nothing but the triangular wave and the modulating signal which is sinusoidal wave are compared to get the different PWM pulses. This is done by VHDL coding. And these pulses are downloaded in FPGA deice as shown in figure 1.1.This FPGA device can be used to drive the single phase multilevel inverter through the interfacing and driving circuit.

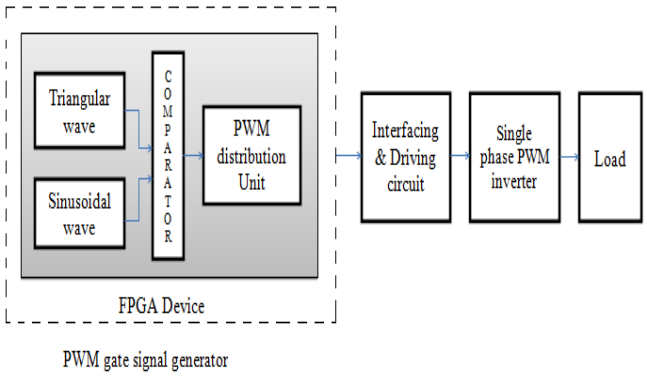


Figure 1. Proposed block diagram

Proposed Circuit

The proposed circuit of the single phase multilevel inverter is shown in the figure 2 .It consist of on full H bridge inverter having the switech S1,S2,S3 and S4 and two bi-directional switech S5 and S6. These bi-directional switchs are used for current controlling.

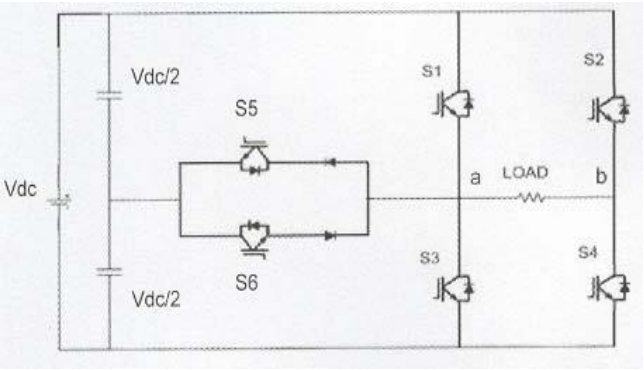


Figure 2. Proposed circuit of single phase multilevel inverter

Two dc capacitors, which are considered as an energy tank for the inverter, are also connected to the dc voltage source. The function of bi-directional switch is to control current flow. The PWM pattern adopted in the proposed inverter makes the inverter producing output voltage with three levels (zero and half supply dc voltage positive and negative respectively) at modulation index (Ma ≤ 0.5) and five levels (zero, half and full supply voltage positive and negative respectively) at modulation index (Ma > 0.5).

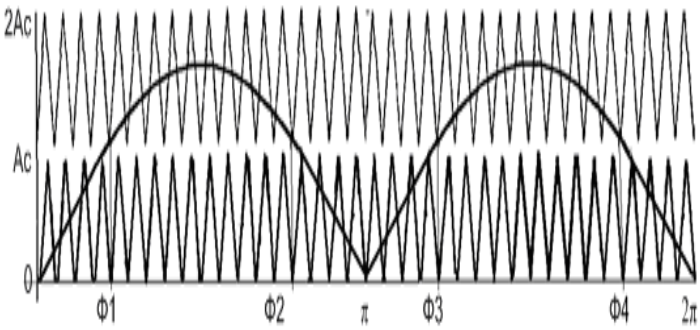


Figure 3. PWM generation technique

The modulation index is defined as:

$$Ma = \frac{Am}{2Ac}$$

Where Am is peak value of sinusoidal wave and Ac is the peak is the carrier peak-peak value.

The angle of displacement existing between the sinusoidal wave and the first positive carrier wave can be defined as following:

$$AmSin^{-1}(\frac{Ac}{Am}) = \phi 1$$

The proposed inverter may be operate in four modes defined as following:

Mode 1 : $\Phi 1 < \omega t < \Phi 2$

Mode 2 : $0 < \omega t \leq \Phi 1$ *and* $\Phi 2 < \omega t \leq \pi$

Mode 3 : $\pi < \omega t \leq \Phi 3$ *and* $\Phi 4 < \omega t \leq 2\pi$

Mode 4 : $\Phi 3 < \omega t \leq \Phi 4$

At modulation index Ma > 0.5 the inverter operates in all modes producing five voltage levels 0, Vdc/2,Vdc, -Vdc/2, -Vdc respectively. At certain load when the required voltage is Vdc/2 or less the inverter operates at modulation index Ma≤0.5 in two modes 2 and 3 only.

The output voltage is depend on the switching sequence which is shown in below table

Switch ON	Va	Vb	Vo=Va-Vb
S4,S1	Vdc	0	+Vdc
S4,S6	Vdc/2	0	+Vdc/2
S4,S3	0	0	0
S2,S1	Vdc/2	Vdc/2	0
S2, S5	0	Vdc /2	-Vdc/2
S2,S3	0	Vdc	-Vdc

Table 1. Switching sequence

III. PWM GENERATION VIA FPGA

Control algorithm of the proposed inverter is digitally implemented in *Universal VLSI Moon1* board. The board has X*C3S400PQ208* FPGA device as the main feature consists of 400k system gates, 8,064 logic cells, 896 CLBs, 264 maximum user I/Os. Other features used on the

Universal VLSI Moon1 board are a 4 MHz oscillator for clock source, one pushbutton switch for system reset and toggle switches for the selection of modulation index values.

For the generation of PWM it is required to compare the sinusoidal modulating signal and the triangular carrier signal. A simple logic which I have used is the "COUNTER". The pulse width depends on the counter speed. The count is nothing but the input data which will be variable. If the counter speed is slow then the width of the pulse is more and if it counts fast the short width pulse will be generated. The speed of the counter depends on the clock. This clock is nothing but the system clock which I will use as sinusoidal modulating signal. The system clock is high frequency near about 4 MHz to 6 MHz . By using "divide by" network required modulating signal can be obtained.

The following figure shows the flow how the six PWM pulses are generated.

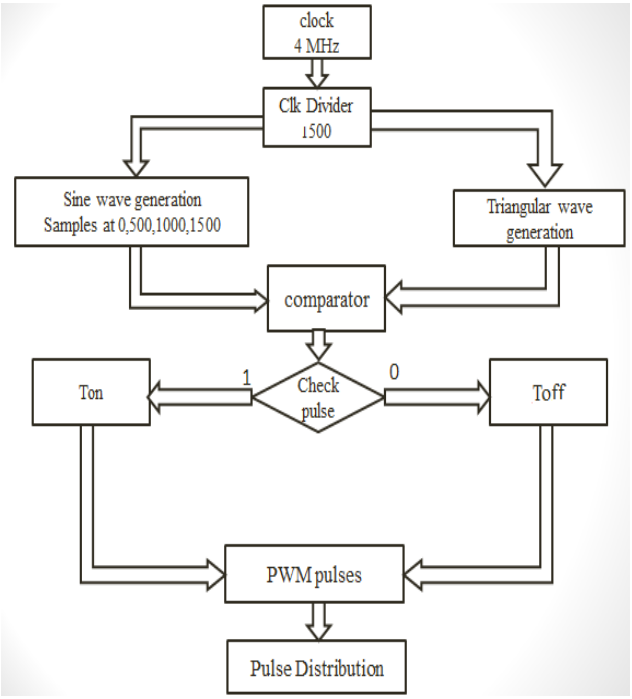
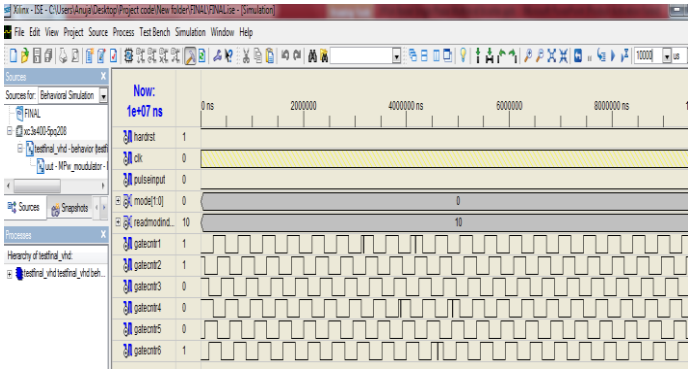


Figure 4. Block diagram of the PWM generator

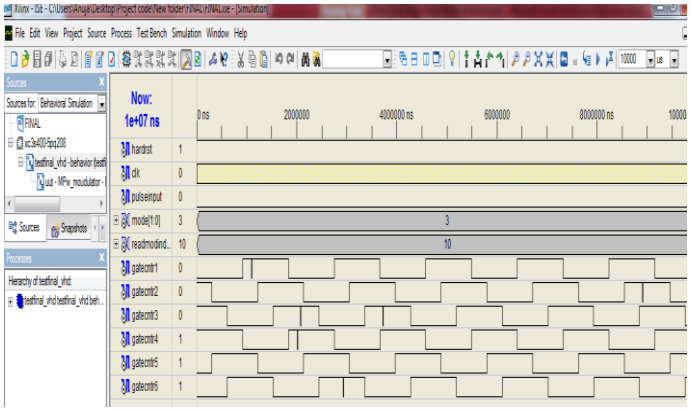
The main system frequency of 4 MHz is divided by 1500 to get the triangular frequency of 2668 Hz. This frequency is used as a carrier frequency. Further this frequency is again divided by 50 to get the 53 Hz, which is used as sinusoidal wave and which is further used as modulating signal. The different samples of sine wave are taken in the form of sine wave data at different points. The different points like 0, 500, 1000, 1500 are taken for the reference. The check pulses are taken at the reference points. Thus the six PWM pulses are generated using the above said logic. The generated pulses cannot be given directly to the inverter circuit. To avoid the short circuit problem and to provide the isolation between FPGA device which is working as control circuit and the inverter circuit which is power circuit, the opto-isolaters are used. The PWM pulses are given to the MOSFETs through interfacing and driving circuit. It contains buffer and opto-isolater.

IV. RESULTS

The model of the proposed multilevel PWM single phase inverter is simulated by using Xilinx simulation tool. The PWM pattern is derived and simulated at different modulation indexes (Ma) as a control signals; the system is tested and simulated by resistive. The waveforms of voltage output and load current are obtained, experimental and simulated results are compared and show satisfactory results.



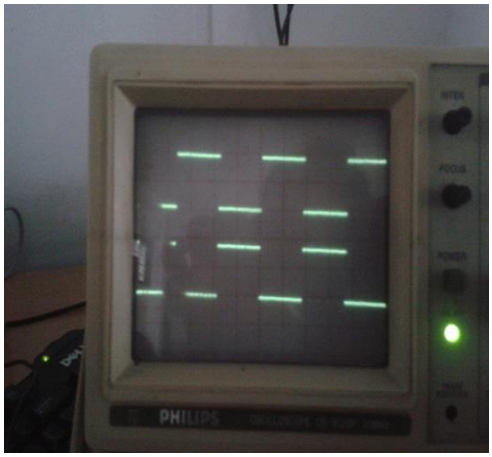
Multilevel PWM single phase simulation results using XILINX FPGA at Ma < 0.5



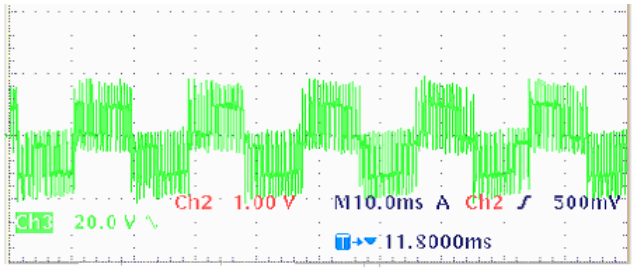
Multilevel PWM single phase simulation results using XILINX FPGA at Ma ≥ 0.5

The generated pulses are then downloaded in FPGA device. These pulses are tested on CRO. The CRO results are shown below

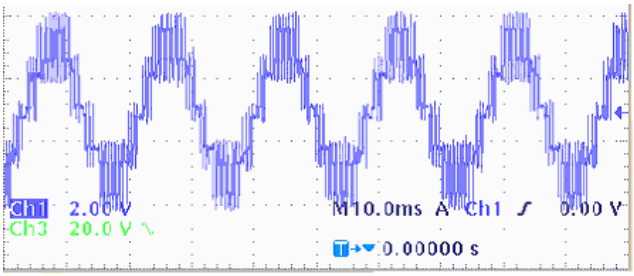
Multilevel PWM single phase experimental results using at Ma < 0.5



Multilevel PWM single phase experimental results at Ma ≥ 0.5



output voltage three levels at Ma < 0.5



output voltage five levels at Ma ≥ 0.5

V. CONCLUSION

The switching patterns adopted are applied at the six inverter switches to generate five or three output voltage levels at different modulation indexes. XILINX FPGA enables to make easy, fast and flexible design and implementation. The experimental and simulated results are show satisfactory results in term of total harmonic distortion and output voltage and current waveform shapes.

ACKNOWLEDGEMENT

This research project would not have been possible without the support of my mentor, guide, teachers and friends. I am thankful to all the individuals who encouraged and helped me directly and indirectly to carry this work. Their continuous invaluable knowledgably guidance throughout the course of this study helped me to complete the work up to this stage and hope will continue in further research.

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