UACEE International Journal of Advancements in Electronics and Electrical Engineering – IJAEEE
Volume 2 : Issue 2 [ISSN 2319 – 7498]
Publication Date : 05 June 2013

Analysis of Two & Three Level Diode Clamped Multilevel Inverter Fed PMSM Drive Using Space Vector Pulse Width Modulation (SVPWM)

G. Sree Lakshmi Dr. S. Kamakshaiah Dr. Tulasi Ram Das

***Abstract*—This paper proposes implementation of Two & Three Level Diode-Clamped Multilevel inverter using IGBT's fed to both built -in and mathematical model of PMSM drive. The pulses for the inverters have been developed by using Space Vector Pulse Width Modulation Technique (SVPWM). Space Vector Pulse Width Modulation Technique is most prominent PWM technique for three phase voltage source inverters for the control of AC Induction Motors, Brushless DC Motors, Switched Reluctance and Permanent Magnet Synchronous Motors. The output voltages, currents, torque & speed characteristics have studied for two & three-level inverters fed to both mathematical model and built -in model. It has observed that both have same results. Three -level inverter can use more DC link voltage than two- level inverter and also SVPWM Technique utilizes DC bus voltage more efficiently and generates less harmonics.**

***Keywords*— Diode Clamped Two-level inverter, Three-level inverter, Space Vector Pulse Width Modulation (SVPWM), PMSM.**

I. Introduction

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive applications of this technology are in the medium- to high-voltage range (2-13 kV), and include motor drives, power distribution, power quality and power conditioning applications. In general, multilevel power converters can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels. The selection of the best multilevel topology and the best control strategy for each given application is often not clear and is subject to various engineering tradeoffs. By narrowing this study to the DC/AC multilevel power conversion technologies that do not require power regeneration, several attractive topological, modulation and power semiconductor device choices present themselves [1]-[4].

G. Sree Lakshmi, Associate Professor, Department of EEE,
CVR College of Engineering, Hyderabad, India
s_sreelakshmi@yahoo.com

Dr. S. Kamakshaiah, Former Professor and Head, Department of EEE,
JNT University, Hyderabad
s_kamakshaiah@yahoo.com

Dr. Tulasi Ram Das, Vice Chancellor,
JNT University, Kakinada
das_tulasi@gmail.com

The most actively developed of these multilevel topologies are

- Diode Clamped
- Flying Capacitor
- Cascade Full Bridge

The Modulation strategies are classified as

- Fundamental Frequency Switching
- Pulse Width Modulation

Pulse Width Modulation has again classified as

- Sinusoidal Pulse Width Modulation (SPWM)
- Space Vector Pulse Width Modulation (SVPWM)

The Two-Level inverter topology has attracted attention in low power low voltage drive applications where as Three-Level inverter topology has attracted attention in high power high performances voltage drive applications. The Main purpose of these two-level and three-level inverter topologies is to provide a three phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. The two-level inverter is composed of only one switching cell per phase but the three-level inverter has two switching cell per phase. Three level diode clamped (Neutral point) inverter is most favorable among the various multi level configuration. Using enough levels the multi-level inverter generates approximately a sinusoidal voltage waveform with very low harmonic distortion [2]-[6].

With the availability of high speed power semi conductor devices the harmonic contents of output voltage can be minimized or reduced significantly by switching techniques like space vector pulse width modulation (SVPWM). To control multilevel converters, the pulse width modulation (PWM) strategies are the most effective, especially the space vector pulse width modulation (SVPWM) one, which has equally divided zero voltage vectors describing a lower total harmonic distortion (THD). Although the complexity that presents the SVPWM strategy (many output vectors) compared with the carrier-based PWM one, it remains the preferred seen that it reduces the power losses by minimizing the power electronic devices switching frequency (limiting the minimum pulse width). In this paper the analysis of two & three-level diode clamped multilevel inverters has simulated using IGBT's , pulses for the switches has simulated using SVPWM technique and the output of these inverters are fed to Permanent Magnet Synchronous Motor. A Torque & Speed characteristic of PMSM has been studied [4].

II. Diode Clamped Multilevel Inverter

A. *Two Level Diode Clamped Inverter*

The three phase two level voltage source diode clamped inverter has shown in the Fig.1. It consists of six power (IGBT) switches. When the pulses are given to the switches the switches will conduct accordingly. When the positive IGBT is switched on (i.e) when the switches a, b or c is on then the corresponding lower IGBT will be in off state. Therefore by properly switching the IGBT'S we can get the output voltage[10].

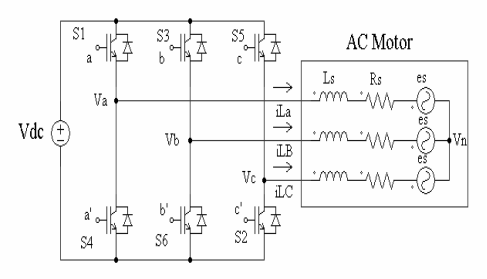

Fig.1. Three Phase Two-Level Diode Clamped Inverter

B. *Three Level Diode Clamped Inverter*

The three Phase three level diode clamped multilevel inverter is shown in Fig.2. Which consists of 12 -IGBT's; in each leg it contains 4 switches. Each switch contains anti-parallel diode. The inverter leg A is composed of four active switches S_1 to S_4 with four anti-parallel diodes D_1 to D_4. On the DC side of the inverter, the DC bus capacitor is split into two, providing a neutral point n. The diodes connected to the neutral point, D_{n1} and D_{n2} are the clamping diodes. When the switches S_2 and S_3 are turned on, the inverter output terminal A is connected to the neutral point through one of the clamping diodes. The voltage across each of the dc capacitors is $V_{dc}/2$, which is normally equal to half of the total dc voltage V_{dc}. Therefore the voltage stress of switching devices is greatly reduced. The output voltage has three different states $+V_{dc}/2$, 0, $-V_{dc}/2$.

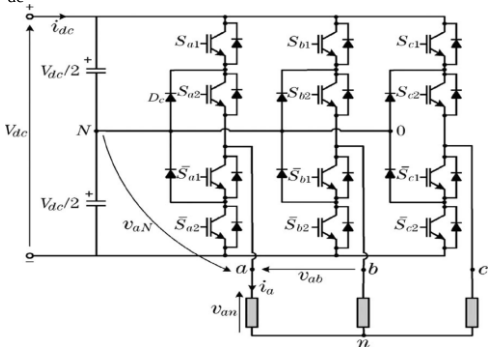

Fig. 2. Three Phase Three-level diode-clamped inverter

For example if Phase A is taken , then to get $+V_{dc}/2$, the switches S_1 and S_2 need to be turned on; to get 0 voltage switches S_2 and S_3 need to be turned on; to get $-V_{dc}/2$, switches S_3 and S_4 need to be turned on. These states can be defined as 2, 1 and 0 respectively. Then the switching variable S_a is shown in the table 1. Similar to two level inverter, the switching states of one leg of three level inverter is described by using switching variables S_a, S_b and S_c whereas the difference is that in three level inverter, each leg has three different switching states [11].

TABLE.I

V_{an}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_a
$+V_{d/2}$	1	1	0	0	2
0	0	1	1	0	1
$-V_{d/2}$	0	0	1	1	0

a.Switching Sequence of Switch S_a

III. Space Vector Pulse Width Modulation

The SVM approach is the most powerful, because it allows more freedom to control and optimize the switching patterns than any other modulation approach. The basic principle depends on synthesizing the reference voltage vector by time averaging of the three nearest vector produced by the inverter. The implementation of the SVPWM technique involves many steps. They are mainly

- Transformation of 3-phase to 2-phase.
- Calculating the space vector voltage.
- Identifying the three nearest vectors
- Calculation of the dwelling times on the three nearest vectors.
- Determination of the switching instants.

A. *SVPWM for Two-Level inverter*

SVPWM for two level inverter consists of 8 switching states out of which 6 are active space vectors which are phase displaced by 60^0 with $2V_{dc}/3$ length and form a hexagon. The 2 zero space vectors are located at the center of the hexagon.

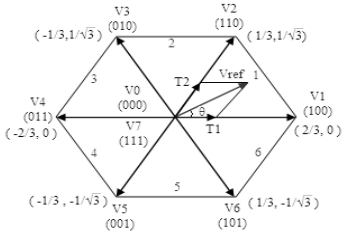

Fig.3. Basic switching vectors and sectors for two level inverter

The three voltages which are displaced by 120^0 are converted into two phase's (i.e.) into d-q frame.

$$V_d = V_{an} - V_{bn}{}^{*}\text{Cos}60 - V_{cn}{}^{*}\text{Cos}60$$
$$V_d = V_{an} - (1/2)\, V_{bn} - (1/2)V_{cn}$$
$$V_q = 0 + V_{bn}{}^{*}\text{Cos}30 - V_{cn}{}^{*}\text{Cos}30$$
$$V_q = (\sqrt{3}/2)\, V_{bn} - (\sqrt{3}/2)\, V_{cn}$$

The required space vector voltage and the angle θ

$$V^{*} = \sqrt{(V_{d2} + V_{q2})}$$
$$\theta = \text{Tan}^{-1}(V_q / V_d)$$

Now the dwelling times are calculated as:

$$V^{*} = V_a + V_b$$
$$= V_1 (T_a/T_c) + V_2(T_b/T_c) + (V_0 \text{ or } V_7)(T_0/T_c).$$

$V^* T_c = V_1 (T_a) + V_2 (T_b) + (V_0 \text{ or } V_7) (T_o)$

Where,

$T_a = (V_a/V_1) T_c$

$T_b = (V_b/V_2) T_c$

$T_o = T_c – (T_a + T_b)$

T_a and T_b are the dwelling times of the command voltage vector on V_1 and V_2 .The time intervals T_a and T_b satisfy the command voltage, but the time to fills up the remaining gap for T_c with the zero or null vectors. The time period $T_c = T_s/2$ where F_s = switching frequency.

B. *SVPWM for Three-Level Inverter*

The SVPWM technique for three level inverter consists of 27 switching states out of which there are 24 active states and 3 zero states at the center of the hexagon. If the triangle sector is defined by vector V_x, V_y, V_z, then V^* can be synthesized by V_x, V_y, and V_z Assuming the duration of vector V_x, V_y, and V_z are T_x, T_y, and T_z respectively, and $T_x+T_y+T_z = T_s$, where T_s is switching period[7]-[9]. Then X, Y and Z can be defined as the following equations:

$X = T_x/T_s$

$Y = T_y/T_s$

$Z = T_z/T_s$

Based on the principle of vector synthesis, the following equations can be written:

$X+Y+Z=1$

$V_x^*X + V_y^*Y + V_z^*Z = V^*$

The modulation ratio of three-phase three-level inverter is represented as follows:

$m = |V^*|/(2/3V_d) = 3|V^*|/2V_d$

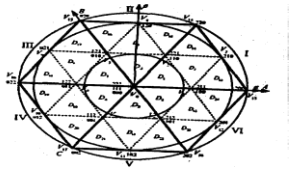

Fig.4 Basic switching vectors and sectors for three level inverter

The boundaries of modulation ratio are $Mark_1$, $Mark_2$, and $Mark_3$

$Mark_1 = (\sqrt{3}/2) / (\sqrt{3}\cos(\theta) + \sin(\theta))$

$Mark_2 = (\sqrt{3}/2) / (\sqrt{3}\cos(\theta) - \sin(\theta))$: $\theta \le \pi/6$

$= (\sqrt{3}/4) / \sin(\theta)$ $\pi/6 < \theta \le \pi/3$

$Mark_3 = \sqrt{3} / (\sqrt{3}\cos(\theta) + \sin(\theta))$

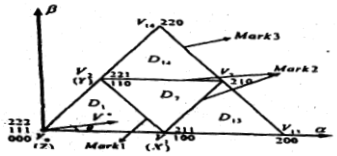

Fig.5. Calculation of dwelling times

Case 1: When the modulation ratio $m<Mark_1$, the rotating voltage vector V*is in sector D_1 ,V* is synthesized by V_0, V_1, and V_2

$1/2X + 1/2[\cos(\pi/3)\, Y + j \sin(\pi/3)]\, Y = m [\cos(\theta) + j \sin(\theta)]$

Using above equations, we can obtain X, Y, and Z as follows:

$X = 2m. [\cos(\theta) – \{\sin(\theta)/\sqrt{3}\}]$

$Y = m*4*\sin(\theta)/\sqrt{3}$

$Z = 1-2*m [\cos(\theta) + (\sin(\theta))/\sqrt{3}]$

Case 2: when ($Mark_1 < m < Mark_2$), V* is in sector D1, V* can be synthesized by V_1, V_2, and V_7 And the corresponding X, Y, and Z are:

$X = 1- m*4*\sin(\theta)/\sqrt{3}$

$Y = 1- 2*m. [\cos(\theta) - (\sin(\theta))/\sqrt{3}]$

$Z = -1 + 2*m [\cos(\theta) + (\sin(\theta))/\sqrt{3}]$

Case 3: When ($Mark_2<m<Mark_3$) and ($0<\theta<\pi/6$), V* is in sector D_{13} V_1, V_{13}, and V_7 are selected to synthesize V*. The durations of them are obtained as follows:

$X = -1 + 2*m [\cos(\theta) - (\sin(\theta))/\sqrt{3}]$

$Y = m*4*\sin(\theta)/\sqrt{3}$

$Z = 2-2*m [\cos(\theta) + (\sin(\theta))/\sqrt{3}]$

Case 4: When ($Mark_2 < m < Mark_3$) and ($\pi/6<\theta<\pi/3$), V^* is in sector D_{14}. Vectors V_2. V_7, and V_{14} will be employed to generate the required voltage. X, Y, and Z can be expressed as follows:

$X = 2*m [\cos(\theta) - (\sin(\theta))/\sqrt{3}]$

$Y = -1+ m*4\sin(\theta)/\sqrt{3}$

$Z = 2-2*m [\cos(\theta) + (\sin(\theta))/\sqrt{3}]$

When the reference vector falls into the others major sectors, similar argument can be applied.

Replacing θ by θ-60, θ-120, θ-180, θ-240, and θ-300 respectively, the calculation of the entire coordinate plane can be established.

IV. Permanent Magnet Synchronous Motor

In this paper the simulation analysis has done both with MATLAB built-in PMSM and Modeled PMSM.

The stators of the PMSM and the wound rotor synchronous motor (SM) are similar and there is no difference between the back EMF produced by a permanent magnet and that back EMF produced by an excited coil. Hence the mathematical model of a PMSM is similar to that of the wound rotor SM.

The stator *d*, *q* equations of the PMSM in the rotor reference frame are:

$$Vq = RIq + P\omega r\lambda d + p\lambda q$$
$$Vd = RId - P\omega r\lambda q + p\lambda d$$

Where

$$\lambda q = LqIq$$
$$\lambda d = LdId + \lambda m$$

where *P* is the pole pairs, *p* is the *d/dt* operator, v_q and v_d are the *q*, *d* axis voltages, i_q and i_d are the *q*, *d* axis stator currents, L_q and L_d are the *q*, *d* axis inductances, λ_q and λ_d are the *q*, *d* axis stator flux linkages, while *r* and ω_r are the stator resistance and rotor speed, respectively. λ_m is the flux linkage due to the rotor magnets linking the stator.

The electromechanical torque developed by the motor is :

$$Tem = \frac{3}{2}P(\lambda dIq - \lambda qId)$$

By substituting the values of λ_q and λ_d in the above equation

$$Tem = \frac{3}{2}P(\lambda mIq + (Ld - Lq)IqId)$$

The relationship between the electromechanical torque and the load torque is given as :

$$\frac{d\omega r}{dt} = \frac{1}{Jm}(Tem - Tl - Bm\omega r)$$

$$\frac{d\theta r}{dt} = \omega r$$

The parameters of the PMSM are:

```
Ld=0.025434;
Lq=0.005;
R=8.668446735;
PM_flux=0.167;
P=6;
F=0.00004;
J=0.15;
```

v. Simulation Results and Analysis

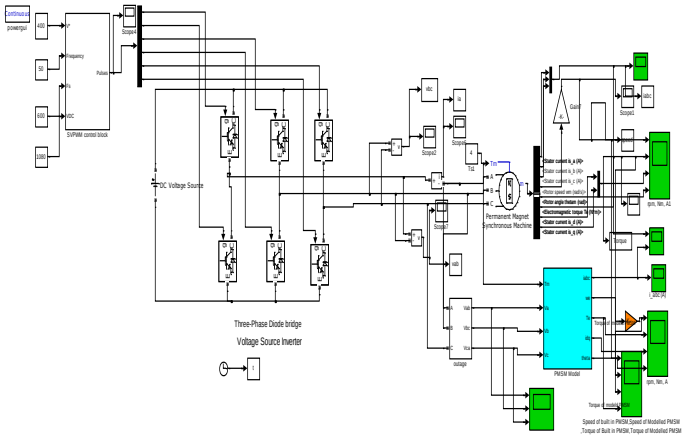

Fig.6. Simulation of Three phase Two-Level Inverter

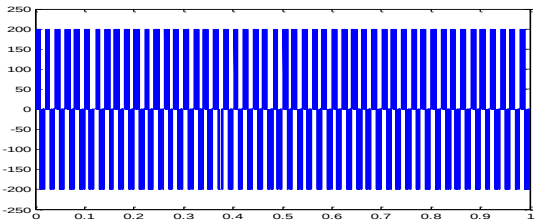

Fig.7. Output Voltage of two level inverter

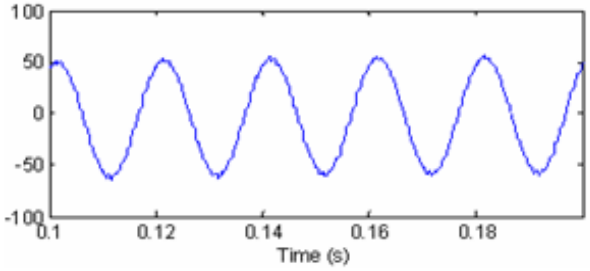

Fig.8. Output Current of two level inverter

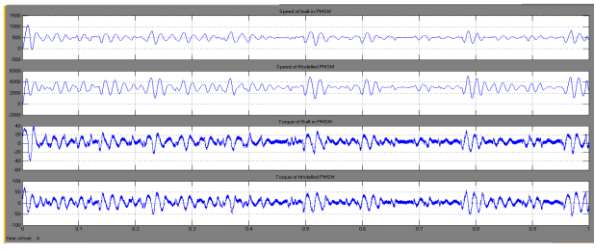

Fig.9. Output Speed & Torque of a built-in & modelled PMSM with two level inverter

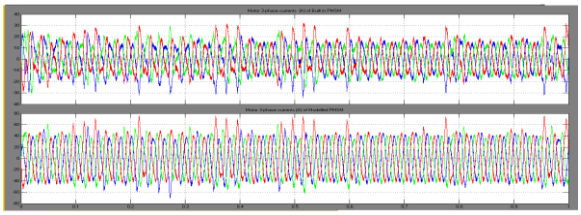

Fig.10. Output three phase currents of a built-in & modeled PMSM with two level inverter

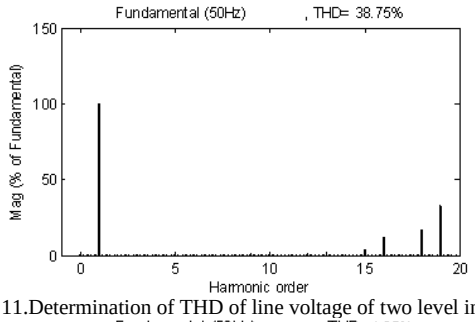

Fig .11.Determination of THD of line voltage of two level inverter

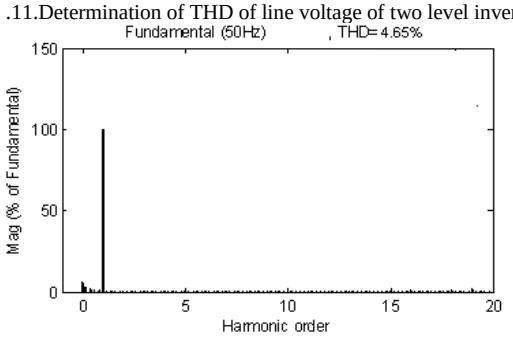

Fig .12 Determination of THD of line current of two level inverter

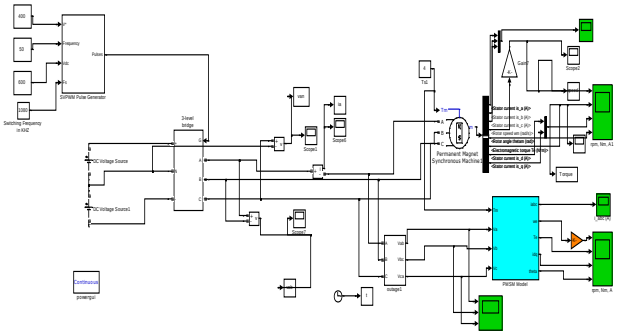

Fig.13 Simulation of Three phase Three-Level Inverter

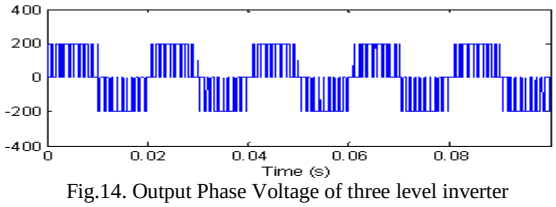

Fig.14. Output Phase Voltage of three level inverter

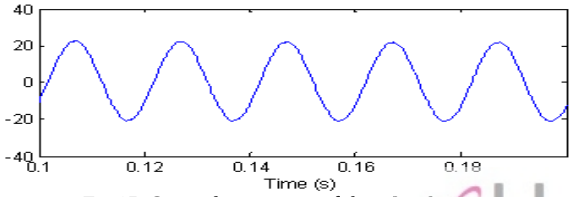

Fig.15. Output line current of three level inverter

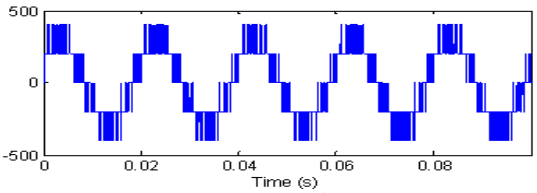

Fig.16. Output Line Voltage of three level inverter

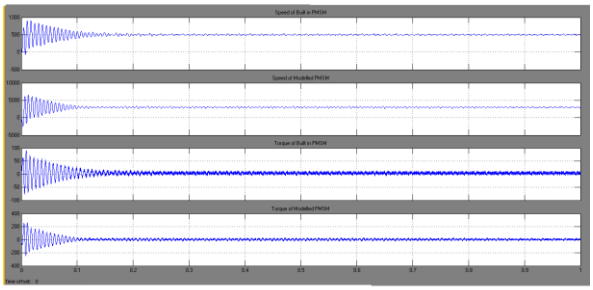
Fig.17 Output Speed & Torque of a built-in & modelled PMSM with three level inverter

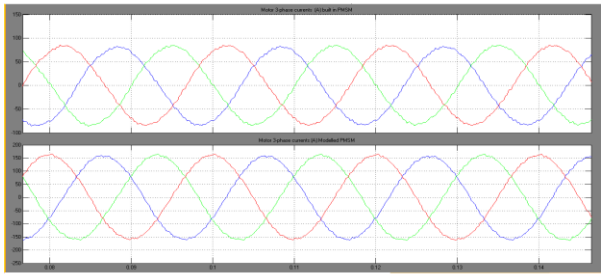
Fig.18 Output three phase currents of a built-in & modeled PMSM with three level inverter

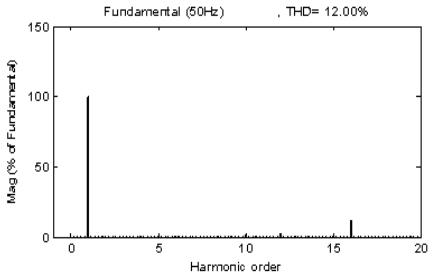

Fig .19.Determination of THD of line voltage of three level inverter

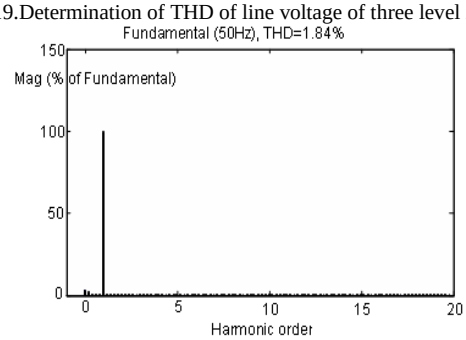

Fig .20. Determination of THD of line current of three level inverter

VI. Conclusion

In this paper, Two & Three level diode clamped inverters are simulated using IGBT's. The Pulses for the switches has developed using Space Vector Pulse Width Modulation Technique. The Outputs of the inverters are fed to the Permanent Magnet Synchronous Motor for two types one is built in model and the other is simulated model. Simulation analyses concerning the applications of SVPWM control strategy on the two and three level diode clamped IGBT's inverters Fed PMSM drive are presented. The output Voltages of Two Level & Three Level inverters and the Torque, Speed characteristics of PMSM drive has been studied. From this analysis author can conclude that multilevel inverter can eliminate the harmonics produced by the normal inverter. It has been observed that three level inverter gives good performance characteristics than two level inverter. The output Torque, Speed has been improved using three level diode clamped inverter. From the results it is concluded that three level inverter can use more dc link voltage than two level inverter and also SVPWM Technique utilizes DC bus voltage more efficiently and generates less harmonics. Also it has been observed that the torque, speed and three phase currents of both built-in & modeled PMSM drive have same waveforms.

References

[1] Aneesh, M.A.S., Gopinath.A, Baiju.M.R. " A Simple Space Vector PWM Generation Scheme for Any General n-Level Inverter "Vol.56, issue-5, Industrial Electronics, IEEE Transactions, pp.1649-1656, May-2009

[2] Gupta.G.K, Khambadkone.A.M.," A Space Vector PWM Scheme for Multilevel Inverters Based on Two-Level Space Vector PWM " vol.53, issue-5,Industrial Electronics, IEEE Transactions,Oct.2006

[3] "Pulse width modulation for power converters" principles and practice by D. Grahame Holmes and Thomas A. L

[4] "Multilevel inverters: a survey of topologies, controls, and applications" by José Rodríguez, Jih-Sheng Lai, and Fang Zheng Peng 1999 IEEE paper.

[5] Multilevel converters for large electric drives" by Leon M. Tolbert, Fang Zheng Peng, and Thomas G. Habetler.

[6] "Fault diagnosis system for a multilevel inverter using a neural network" by Surin Khomfoi & Leon M. Tolbert.

[7] "A simple svpwm algorithm for multilevel inverters" by Lei Hu, Honyan Wang, Yan Deng and Xiangning He College of Electrical Engineering, Zhejiang University Hang Zhou, China. 2004 35th Annual IEEE Power Electronics Specialists Conference.

[8] Jae Hyeong Seo, Chang Ho Choi, Dong Seok Hyun "A new simplified space-vector PWM method for three-level inverters "Vol.16, issue-4, Powerelectronics IEEE Transcations, pp..545-550, july-2001.

[9] Reney.D, "Modeling and Simulation of Space Vector PWM Inverter ", Devices and Communications (ICDeCom), International Conference, pp.1- 4, 24-25th feb,2011.

[10] Lwwicki.A, Krzeminski.Z, Abu-Rub.H. "Space-Vector Pulsewidth Modulation for Three-Level NPC Converter With the Neutral Point Voltage Control " Vol.58, issue-11, pp.5076-5086,Industrial Electronics, IEEE Transactions, Nov.2011.

[11] Lourci.N, Berkouk.E.M., Boudiema.F., Petzoldt.J. Dali.M.Y., "A simplified space vector pulse width modulation algorithm for five level diode clamping inverter " pp.1349-1354, Power Electronics Electrical Drives,SPEEDAM,23-26th May,2006.