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Digital System Analysis using Xilinx ChipScope Logic Analyzer

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***Abstract*—The present research paper depicts a technique to debug FPGA based systems by merely viewing internal signals pertaining to real time processes. There are established techniques prevailing in this domain based on Logic Analyzer that facilitates display of 16 to 32 simultaneous signals. However, the main bottleneck comes when monitoring of the internal signals of reconfigurable devices like Field Programmable Gate Array (FPGA) is concerned; especially when it is not practically possible to bring them out at I/O pins for the purpose of monitoring. Through the present paper author showcases an EDA tool, ChipScope-Pro from Xilinx Inc., for viewing signals inside the FPGA. For that, a prototype of data acquisition system has been technologically advanced using serial Analogue to Digital Convertor (ADC) and different Soft Intellectual Property (IP) Cores developed in Very High Speed Integrated Circuit Hardware Description Language (VHDL) and implemented in the Xilinx FPGA. A physical parameter, humidity was observed on computer screen using the Logic Analyzer of Xilinx Electronic Design Automation (EDA) tool ChipScope; instead of producing its digital equivalent signals on I/O pads of the FPGA. A top level module was developed by instantiating three VHDL cores: Integrated Controller (ICON), Integrated Logic Analyzer (ILA), and a Soft IP core driving a 12 bit serial ADC. The interface between FPGA internal signals and ChipScope was accomplished using the Xilinx Joint Test Action Group (JTAG) cable and the FPGA Virtex-5 board.**

***Keywords*— ChipScope, FPGA, Vitrex-5, internal signals, ICON, ILA, Core Generator, JTAG**

I. Introduction

Currently one option for the Field Programmable Gate Array, i.e. FPGA designer is to use Hardware Description Language (HDL) simulators like Mentor's ModelSim. With the simulator one can verify all HDL, modelling everything from internal flops to an I/O pad. Simulation can be a step backwards for FPGA development. This is because FPGAs have reprogramability built-in. Generally FPGA designers use features to verify their design in-circuit. This is of tremendous value because designers not only saves time in generating the simulation testbench, but actually verify design against real live data [5].

Furthermore, FPGA designs have become increasingly dense and complex. They are difficult to debug because more and more of the relevant signals are buried deep within the logic fabric. Access to signals in the FPGA, on board or in the system is very restricted whether troubleshooting is done in the lab or in the field [1]. To address the controllability and observability issues of in-circuit verification, Xilinx has created an Electronic Design Automation (EDA) tool ChipScope, in which there are two fundamental intellectual property (IP) cores giving real-time observability and controllability [5]. By inserting an "Integrated Controller core" (ICON) and an "Integrated Logic Analyzer" (ILA) into the top level design and connecting them properly, it is possible to monitor any or all of the signals in design. ChipScope provides with a convenient software based interface for controlling the "Integrated Logic Analyzer," including setting the triggering options and viewing the waveforms [6]. The Xilinx ChipScope-tools communicate with these components and provide the designer with a robust Logic Analyzer solution [2].

ChipScope-Pro provides number of other tools like Xilinx Core Generator, internal bit error ratio tester (IBERT) Core Generator, Core Inserter and Analyzer. The Core Generator, which is the part of Xilinx Integrated Software Environment (ISE) setup can generate necessary cores like ICON, ILA, Virtual Input/Output (VIO), and Agilent Trace Core 2 (ATC2) in VHDL or Verilog HDL.

All of the ChipScope-Pro cores use the Joint Test Action Group (JTAG) Boundary Scan port to communicate to the host Personal Computer via a JTAG download cable. The ICON core is used as a testing control logic core and provides a communications path between the JTAG Boundary Scan port of the target FPGA and the ILA cores. The ILA core is a module that can be adapted to the testing system, working as customizable Logic Analyzer to monitor any internal signal of the design. Since the ILA core is synchronous to the monitored design, all design clock constraints that are applied to the design are also applied to the components inside the ILA core [4].

The module PmodAD2 deployed in this research work is an analogue-to-digital converter (ADC) with four channels, 12-bit resolution powered by the Analogue Devices AD7991 [7]. As given in ADC Transfer Function, the output coding of the AD7991 is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size for the AD7991 is $V_{REF}/4096$ [8]. The data acquisition system used here transfigures humidity

into its digital equivalents and send it serially towards the FPGA to store internally. The present paper gives emphasis on ChipScope-Pro Logic Analyzer to view FPGA internal signals at run-time in a frame of predefined number of signal-samples and also it probes other features provided with the tool.

II. System Overview

Out of several cores provided from ChipScope-Pro, ICON and ILA cores were generated using Xilinx Core Generator software. The sole ICON core controls various Logic Analyzer cores. However, for the existing work, only one ILA core was connected to the core ICON. A soft IP Core provided in [3], was used to drive the serial Analogue to Digital Convertor (ADC) and the same design was put into the analysis using the Logic Analyzer. This module was instantiated with ICON and ILA cores. The top level VHDL entity integrating three modules together was developed. The design was placed and routed using Implementation tools after efficacious completion of Synthesis process; being followed in the Xilinx ISE design flow. Finally, a bitstream of top level module was generated and configured into the target device under test. ChipScope Analyzer was then deployed to accomplish the final goal of this research work i.e. to analyse internal signals of the FPGA.

The number of samples per window was defined at the time of ILA Core generation. Conversely, during the analysis process it is possible to modify such window size and number of windows too. Wherein the multiplication of these two figures does not exceed the number 1024, e.g. a Logic Analyzer window comprising of 512 samples may contain maximum of 2 windows. In existing paper, the Logic Analyzer shows FPGA internal signal i.e. digital equivalents of humidity, external trigger input to trigger Analyzer, two signals that drive a 12 bit ADC, based on Inter IC (I^2C) serial communication protocol, Serial Clock (SCL) and Serial Data (SDA).

The all-inclusive experimental setup consists of a humidity sensor module SY-HS-230 connected to ADC module embedding serial ADC IC-AD7991, the FPGA Viertex-5 board developed by vendor Digilent Inc. The FPGA was interfaced to the computer's Universal Serial Bus (USB) socket by means of Xilinx USB JTAG cable available on the board.

III. Logical System Development

Fig. 1 illustrates a logic block diagram of the system with required hardware setup to deploy Xilinx ChipScope-Pro Logic Analyzer. The humidity sensor is shown at the input of ADC, which is further connected to I/O lines of FPGA. The device ADC delivers 12 bit serial data associated with sampled analogue input voltage. The Soft IP core "masterControler" was configured in FPGA to receive such digital signal using Inter IC (I^2C) serial communication protocol. This serial data was further collected in a 16 bit FPGA internal signal, and a 12 bit slice of which was further given towards the data port of ILA core for its analysis using ChipScope Analyzer. In addition to the core "masterControler", there are two more soft IP cores ICON and

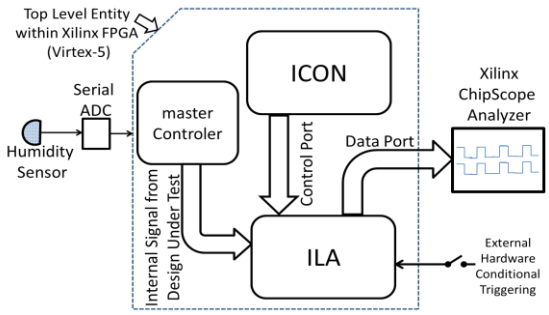

Figure 1. Logic block diagram of the system with Soft Intellectual Propriety (IP) Cores implemented within FPGA and necessary External Hardware for application of Xilinx ChipScope-Pro Logic Analyzer.

ILA, connected in such a way that the core ICON governs the control over ILA. An external hardware trigger port was used as decision-making control to capture ILA data port signals.

The Core Generator of Xilinx ISE 14.1 was used to generate ICON and ILA cores on the same directory of computer hard-drive. In process of creating the core ICON, it was customised to generate with a single Control Port of 36 bits, because there was only one ILA core to be controlled by ICON. Control Ports of ICON and ILA were having similar width and hardwired together. Data Port of ILA was 32 bits wide, produced for visualization on Logic Analyzer window. In the frame of ChipScope Analyzer, it includes a trigger signal "TRIG0" (out of 8 bits), which may be accountable to start and capture the predefined number of signal-samples per window. The Fig. 2 shows a flow diagram for implementation of this application.

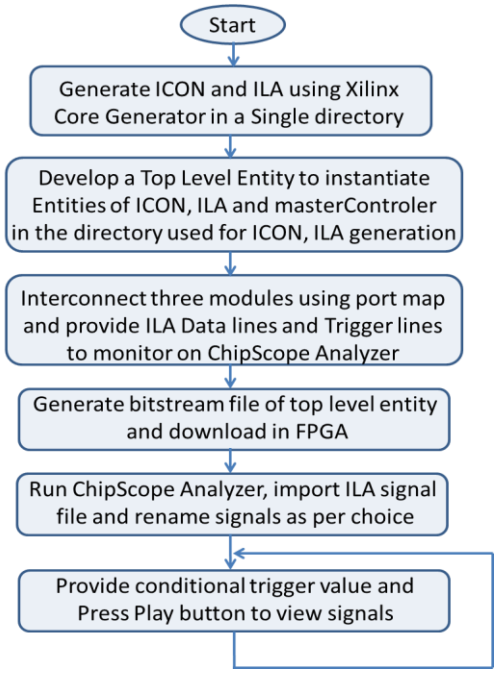

Figure 2. Flow diagram for deployment of Xilinx ChipScope-Pro Logic Analyzer.

IV. Synthesis Results of Integrated Soft IP Cores

Fig. 3 shows a Register Transfer Level (RTL) synthesis result of the top level entity named as "chipscopepaperTOP". A global reset "RESET_cs" is shown at the input of FPGA. The system clock "SYS_CLK_cs" shown, provides a generic clock input for soft IP cores inside the module. A conditional trigger input, necessary to capture analyzer signal-window is provided from external signal, "TRIG_COND". Also there are two more I/O lines as shown in Fig. 3, i.e. "AD2_SCL_cs" and "AD2_SDA_cs" to provide clock and data lines of serial ADC module respectively.

A detailed view of RTL synthesis shown in Fig. 4, illustrates three soft IP cores namely, "masterControler", "icon" and "ila" with their interconnections. There is an internal signal "DCH0_view" which is 16 bits wide, and it is internally connected to the output of ADC driving module "masterControler". However, as given in [3], out of these 16 bits, 0 through 11 bits represent magnitude of the sampled analogue voltage. The Xilinx ChipScope-Pro Logic Analyzer was meant to monitor such internal signal named as "DCH0_view[11:0]", that too without assigning to I/O pins of FPGA. In this way, it shows the potential of this technologically advanced method for monitoring internal signals of such reconfigurable devices.

The external hardware trigger input, "TRIG_COND" (which was obtained from slide switch provided on FPGA board from Digilent Inc.) triggers the Logic Analyzer conditionally, if conditional trigger option is enabled properly when the analyzer is in-process. Three extra signals, "AD2_SCL_cs", "AD2_SDA_cs" and "TRIG_COND" were added to the Data Port of the Analyzer for visualization purpose. The following lines of VHDL code, developed for top level entity forms interconnection between DATA port, Trigger port of the core ILA with top level entity signals.

```
ILA_DATA(15 downto 0)<=DCH0_view;

ILA_DATA(16)<=AD2_SDA_cs;

ILA_DATA(17)<=AD2_SCL_cs;

ILA_DATA(18) <=TRIG_COND;

TRIG0(0)<=TRIG_COND;
```

The top level entity "chipscopepaperTOP", consisting of merely five I/O lines was connected to the FPGA I/O pins using Xilinx ISE I/O pin allocation process. Following are the lines edited in the file named as "chipscopepaperTOP.ucf" after performing the pin allocation process.

```
NET "RESET_cs" LOC = G6;

NET "SYS_CLK_cs" LOC = AG18;

NET "AD2_SCL_cs" LOC = AM13;

NET "AD2_SDA_cs" LOC = AM12;

NET "TRIG_COND" LOC= J19;
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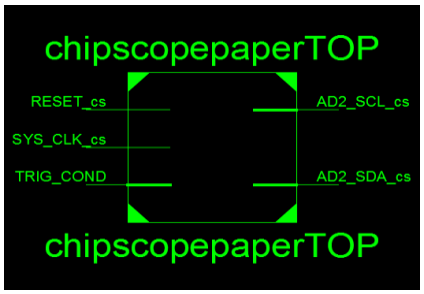

Figure 3. A top view of Synthesis result at Register Transfer Level (RTL) of integrated modules developed in VHDL.

V. Final Testing of the System

A photograph taken at the time of actual testing of the system is shown in Fig. 5, in which it displays FPGA Virtex-5 board interfaced with a small embedded board comprising 4 channel serial ADC IC-7991. The ADC receives analogue voltage from Humidity sensor module SYHS-230 mounted at the aperture of humidity generator. For comparing analogue voltage and its related values shown by ChipScope analyzer, a multimeter (showing voltage when humidity generator was off) is also attached in the setup as shown in Fig. 5. Interconnection of Xilinx USB JTAG cable and PC is also shown in Fig. 5. The computer screen illustrates Logic Analyzer window.

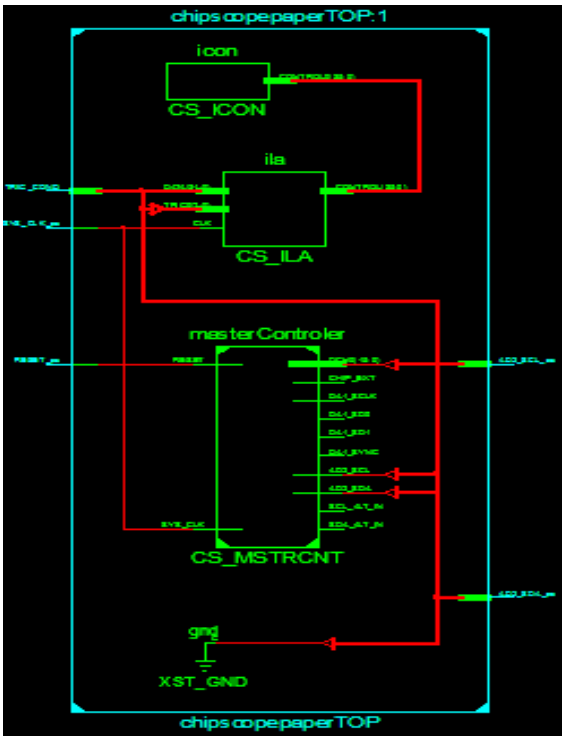

Figure 4. Internal view of Register Transfer Tevel (RTL) Synthesis result showing interconnection of "masterControler", "icon", "ila" modules within the top level entity "chipscopepaperTOP".

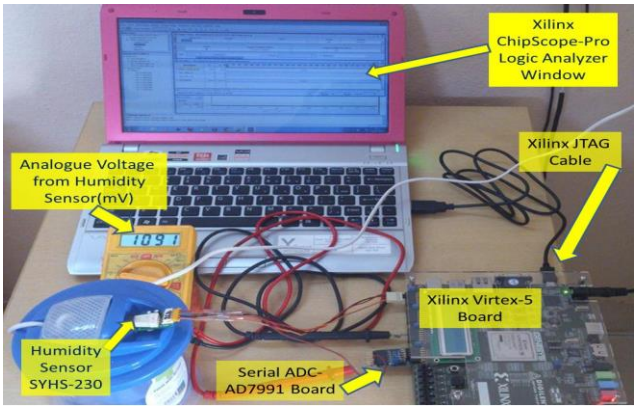

Figure 5. Photograph taken at the time of final testing of the system.

The Fig. 6 shows sub-windows on main frame of the logic analyzer, like Trigger Setup and Waveform window with various internal and external signals. For final testing of the system, a bitstream file "chipscopepaperTOP.bit" of top level entity was configured in SRAM based memory cell within the FPGA and ChipScope Logic Analyser was started. Humidity sensor was exposed to humidity generator. The data port of ILA was set to 32 bits during the core generation process. The 12 bit digital signal generated by serial ADC was to be monitored on the ChipScope analyzer. Therefore, 32 bit data port of ILA was arranged into a 12 bit bus and renamed as "DCH0_view[11:0]". This signal was set to display in a hexadecimal format. The FPGA I/O signals "AD2_SDA_cs" and "AD2_SCL_cs" were displayed on the same window.

The Trigger Setup window displays a conditional trigger input that captures 1024 samples per window here. An 8 bit value associated with analyzer's match unit M0 is "XXXX_XXX1". It specifies that, out of 8 conditional trigger lines, a least significant bit, as shown in Fig.6, starts the logic analyzer to capture signals; only on arrival of logic '1' at the trigger input. On failing to provide such a value, the logic analyzer keeps on waiting for appropriate trigger and does not capture any signal into its buffer.

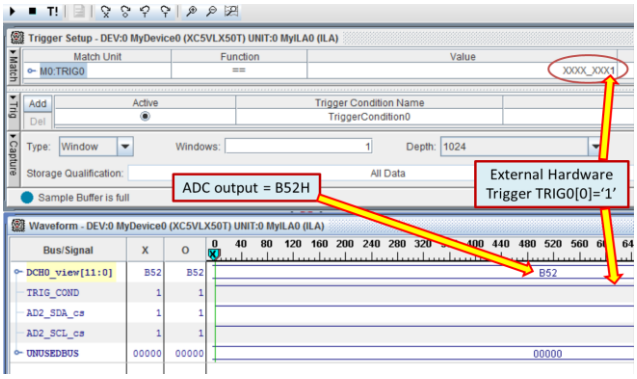

Figure 6. Xilinx ChipScope-Pro Logic Analyzer showing Field Programmable Gate Array (FPGA) internal signal; pertaining to the output of ADC, its driving signals and external hardware conditional trigger input in run-time.

By means of dividing the reference voltage, V_{REF} (i.e. 3.3 V) by 4096, it gives a value of ADC step size, 0.805 mV. The multiplication of step size with expected decimal equivalent of a 12 bit binary number reveals theoretical input voltage of the ADC. During actual testing of the system, the humidity generator was powered on to generate the humidity; due to this analogue input of ADC was measured 2.32V. However, the ChipScope analyzer waveforms display a hexadecimal value B52, as shown in Fig.6, pertaining to FPGA internal signal bus DCH0_view[11:0]. Unswervingly, multiplying decimal equivalent of this number by the step size result an analogue input 2.3348 V. Through this finding, it can be said that theoretical value of ADC input and value shown by ChipScope Logic Analyzer matches each other. As given in [9], the relative humidity and voltage characteristics of SY-HS-230 series, the sensor produce output voltage of 2.38V for 60% of the relative humidity (%RH). Therefore, as shown in Fig.6, as ADC output value is $(B52)_{16}$ i.e. $(2898)_{10}$ then calculated analogue value from this is 2.3348 V, thus the relative humidity must be nearby 60%.

Acknowledgment

The present paper shows the potential of JTAG boundary scan system technologically advanced for Xilinx FPGA devices. The prototype developed here depicts an in-circuit FPGA internal signal analysis in run-time operation; avoiding necessity of writing testbench or entering in the phase of time consuming simulations.

References

[1] K. Arshak, E. Jafer, and C. Ibala, "Testing FPGA based digital system using XILINX ChipScope logic analyser", IEEE Proc. Conf. on Electronic Technology, May 2006, pp. 355-360.

[2] User Guide, "ChipScope Pro 12.3 Software and Cores", Xilinx Inc., September 2010, UG029 (v12.3), pp.15.

[3] Support Document, "Xilinx ISE demo project for the PmodAD2 and a PmodDA1", Digilent, Inc., Pullman, WA 99163-0428, November 2011, DSD-0000321.

[4] Heng Tan, Ronald F. DeMara, Anuja J. Thakkar, Abdel Ejnioui, Jason D. Sattler, "Complexity and Performance Evaluation of Two Partial Reconfiguration Interfaces on FPGAs: a Case Study", Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'06), Las Vegas, Nevada, U.S.A, 2006.

[5] Application Note 1456, "On-Chip Design Verification with Xilinx FPGAs", Agilent Technologies, Inc., U.S.A., April, 2003.

[6] Greg Gibeling & Chris Fletcher, "Using ChipScope", February, 2009, viewed 11 February 2013 from http://www-inst.eecs.berkeley.edu/~cs150/sp13/resources/ChipScope.pdf

[7] Reference manual, "PmodAD2 Reference Manual", Digilent Inc., Pullman, Whiteman, August, 2011, Doc: 502-217.

[8] Datasheet, "4-Channel, 12-/10-/8-Bit ADC with I2C-Compatible Interface in 8-Lead SOT-23", Analog Devices, Inc., U.S.A., 2007–2010.

[9] Application Document, "CAPTEUR D'HYGROMETRIE SY-230", Selectronic 86 rue de CAMBRAI 59000 LILLE, 2004, Reference: 4391-2.