UACEE International Journal of Advancements in Electronics and Electrical Engineering – IJAEEE
Volume 2 : Issue 2 [ISSN 2319 – 7498]
Publication Date : 05 June 2013

Performance Improvement of Diode Clamped Multilevel Inverter Using Carrier Based PWM Scheme and Balancing Circuit

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***Abstract*—Multilevel inverter (MLI) has attracted huge interest in high power and medium voltage application. MLI provides higher power quality at the ac side, can operate at higher ac voltage levels and minimize or even eliminate the interface transformer. It reduces the required voltage rating of the power semiconductor devices. It enables to work at lower switching frequency, so it produces less number of harmonics, lower switching losses and lowerelectromagnetic interference (EMI). Diode clamped inverter (DCI) is one of the most popular topology of the MLI, has achieved huge demand in industrial application and renewable energy system.Among the problem concerning DCI, balancing of the voltages in the dc – link capacitors of diode clamped multilevel inverter with more than three levels is a great challenge. This paper presents carrier based pulse width modulation scheme for five-level diode clamped inverter where the voltage across each capacitor in the dc – link of five-level DCI is maintained constant using a balancing circuit. Simulation results of a five-level DCI are given to validate the performance of proposed scheme.**

Keywords-Diode clamped inverter (DCI), Buck–Boostbalancing circuit, Carrier based pulse widthmodulation.

I. Introduction

The growing attraction towards the high and medium power application in utility, industrial and renewable energy systems has increased a tremendous interest in the high and medium power electronic converters.Accordingly, a multilevel power converter structure has been introduced as an alternative for high and medium voltage application. The general structure of multilevel converter is based on series connection of switching components with several lower dc voltage sources to synthesize a sinusoidal voltage from several levels of voltages [1]-[3].

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One of the multilevel inverter topology that has achieved huge attraction in renewable energy system is the diode clamped multilevel inverter (DCI). Its main advantage, the multilevel voltage outputs of the inverter are easily obtained with the low cost string of dc capacitors.The multilevel diode clamped inverter has attracted significant interest for high-power/voltage application such as static varcompensation, variable speedmotor drives, and high-voltage system interconnections [1]-[4].

Unfortunately, with more than three-levels in DCI, there is a serious problem of capacitor voltage unbalancing. The DCI capacitors tend to overcharge or completely discharge due to the non-uniform power drawn from them. This unbalance problem deteriorates the quality of output voltages and consequently, results in less sinusoidal output, have a higher harmonic content& conversion will have a lower efficiency. Thus there is need for equal voltage sharing among dc capacitors [5]. This limitation can be addressed by using separate dc source [6]. Also, auxiliary dc/dc converter can be added for capacitor voltage balancing [7], [8].

This paper presents concept of voltage balancing circuit for the equalization of dc capacitor voltages in five-level DCI based on carrier based PWM scheme, which is simple and able to effectively reduce lower order harmonic component. The proposed approach is verified using MatLab simulation studies.

II. Voltage Balancing Control Scheme

A. *Five-Level Diode Clamped Inverter*

The diode clamped inverter is proposed by Nabae, Takahashi and Akagi in 1981 was essentially a three-level diode clamped inverter [4]. An m-level diode clamped inverter consist of a $(m-1)$ capacitors on the dc bus and produce m levels of the output phase voltage and $(2m-1)$ levels of output line voltage waveform [9]-[10]. Fig.1 shows the structure of three phases five-level DCI each of the three phases of the inverter shares a common dc bus, which has been subdivided by four capacitors into five levels.

Voltage across each capacitor is V_{dc} and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes, where $4V_{dc}$ is the total dc-link voltage.

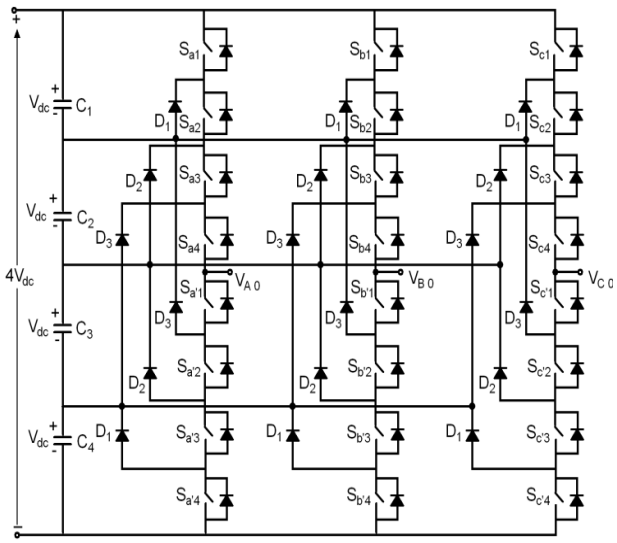


Figure 1. Three phase five-level structure of diode clamped inverter.

The switches S'_{a1} to S'_{a4} be complementary of the switches S_{a1} to S_{a4}, respectively. The output waveform consist of five steps corresponding to five voltage levels from 0to $4V_{dc}$. The operation of diode clamped inverter is taken as follows (with the negative dc rail voltage V_0 as a reference) [1]-[4].

(1) If we want to get voltage level $V_{ab} = 4V_{dc}$, turn on all upper switches S_{a1} to S_{a4} from first leg and turn off all lower switches. Remember that, there must be ON four switches from particular leg at a time.
(2) For getting voltage level $V_{ab} = 3V_{dc}$, turn on upper switches S_{a1} to S_{a3}, turn on lower switch S'_{a4}, turn off switch S_{a4} and also turn off S'_{a1} to S'_{a3}.
(3) Similarly all other combination can be possible.
(4) For getting voltage level $V_{ab} = 0$V, all four upper switches are turned off and all lower four switches from the same leg are turned on.

Fig. 2 shows line-to-line voltage waveform for five-level DCI. The line voltage V_{ab} consists of phase-leg 'a' voltage and phase-leg 'b' voltage. The resulting line voltage is a 9-level staircase waveform.

The DCI is chosen based on its tow advantages over other inverters

(1) Implementation of control strategy is simple.
(2) Enough levels implemented, so the harmonic content in the output is minimized and there is no requirement of filter.

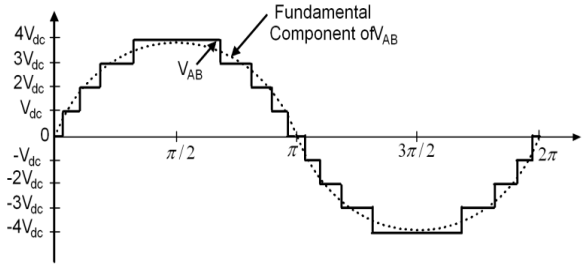


Figure 2. Line voltage waveform for a five-level diode clamped inverter.

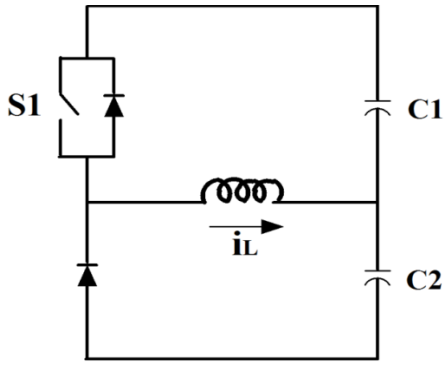


Figure 3. Buck-boost balancing circuit

One major limitation of DCI is the capacitor voltage unbalancing problem [13]. In case of five-level configuration, the top and bottom (C_1 & C_4) capacitors increase in voltage and the middle (C_2 & C_3) capacitors decrease in voltage because these middle capacitor are more utilized, hence they are discharge more in the circuit operation, as compare to top & bottom capacitors and these leads to increase in voltage across the top & bottom capacitors in order to maintain the total dc-link voltage. Since this voltage drift phenomenon affects the ac side voltage waveform and consequently, results in unsatisfactory operation or even failure of the DCI. Thus there is a need for equalization of voltage among dc capacitors. Therefore additional circuitry is desired in order to keep the voltage balance between the capacitors.

B. *Buck – Boost Balancing Circuit*

Voltage unbalance problem of dc-link capacitor in five-level DCI can be resolved by usinga buck-boost balancing circuit, which added to the set of the capacitors [10], [11]. In this circuit switch, diode & inductor is included. The layout of this circuit is shown in fig. 3, same circuitry will be used for lower capacitor (C_3&C_4).

The use behind this balancing circuit is to transfer the energy to the middle capacitor using inductor for energy storing purpose. Assuming an imbalance occurs and C_1 is at high voltage value than C_2, then the switch S_1 will close and energy of C_1 is transfer to the inductor. Once the C_1 reaches the desired voltage, then the switch S_1 will open and stop energy transfer between C_1 and inductor. When switchS_1 is open, the energy stored in the inductor is then transferred to the capacitor C_2 and increasing the voltage of C_2 to its desired value. This exchange of the energy keeps the voltages of capacitor to a desired voltage value continuously.

III. CarrierBased Pulse Width Modulation

Carrier based pulse width modulation with an in phase disposition (IPD) scheme also called as sinusoidal pulse width modulation (SPWM) is utilized for the operation of five-level DCI [13]-[14]. This control schemeis selected

because of its ease of implementation and it provides relatively low THD at the output.

In this modulation scheme, two signals are present one is sinusoidal (reference) signal and another is triangular carrier signal, this two signals are compare to each other. When sinusoidal signal is greater than carrier signal then the gate pulse to the semiconductor device is generated and when sinusoidal signal is lesser than carrier signal then no gate pulse generation is there, in such a way the operation of pulse generation for five-level DCI is performed.

The three phase system of DCI structure requires three reference signals each of them having 120^0 phase shift for the implantation of modulation scheme. In five-level topology, there are four sets of switches and therefore four carrier signal are required, one wave to govern each set of switch. The carrier signal and reference signal is shown in fig. 4.

Magnitude of the output voltage of the inverter can be controlled by altering the amplitude of reference signal with respect to carrier signal. The amplitude of the reference signal is determined by modulation index m_a,

$$m_a = \frac{V_{ref}}{V_{carrier}}$$

Where, V_{ref} is the peak amplitude of reference signal and $V_{carrier}$ is the peak amplitude of carrier signal.

In case oftwo-level inverter, the peak amplitude of carrier signal is equal to 1. In case of five-level DCI, four carrier signals are used, therefore this constant value of one carrier signal is equally divided for four carrier signals. The interaction of this four carrier signal and reference signal determines the switching instants and commutation of the modulated pulse; this can be more easily seen from the fig. 4.

The frequency of each carrier signal is determined by a modulation frequency ratio m_a,

$$m_f = \frac{f_{carrier}}{f_{ref}}$$

By utilizing higher carrier frequency, the output voltage obtains with lesser harmonic content but there is increase in switching losses. Therefore to obtain desirable voltage output and minimum losses in the system, we have to choose optimal value of the $f_{carrier}$. As a basic concept, m_f is

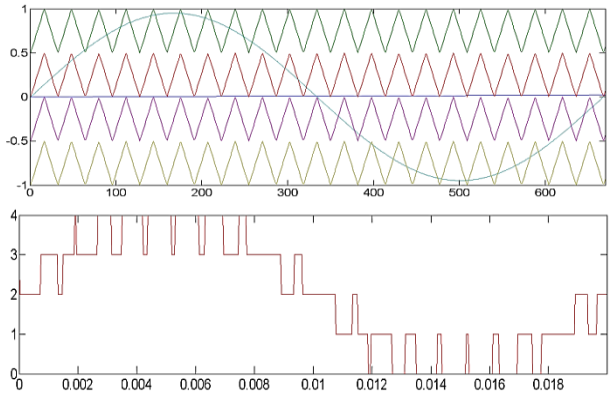


Figure 4. Pulse generation for five-level diode clamped inverter.

chosen as an odd multiple because it results in automatically eliminates all even harmonics from the output signal [11].

IV. Simulation Results

The effectiveness of the proposed scheme for the five-level DCI is realized in MatLab simulation software using the default library component. The diode and IGBT used are inviolate from their default state values. The model of the DCI is shown in fig. 5 in which RL load is used for the validation of proposed theory. The inverter subsystem block contains a model of five-level diode clamped inverter following the buck-boost balancing circuit. Table I shows the simulation parameter.As discussed in this paper, the control strategy chosen for the five-level DCI is the carrier based pulse width modulation in phase disposition. This strategy is implemented in pulse generator block from fig. 5 is described in fig. 6 for only one phase.

The voltage source serves as a reference signal for each phase by a phase shift of 120^0 from each other. The amplitude of each reference signal is decided by a constant value that can be adjusted depending upon the desired output of five-level DCI. The carrier signals are arranged based on a maximum amplitude of 1.0 and for five-level DCI requirement of carrier signal are four, then this amplitude split into four parts for positive half cycle 0 to 0.5 and 0.5 to 1.0 and for negative half cycle 0 to -0.5 and -0.5 to -1.0. So by comparing reference signal with the carrier signal, its output becomes a switching signal which are used for the operation of inverter.

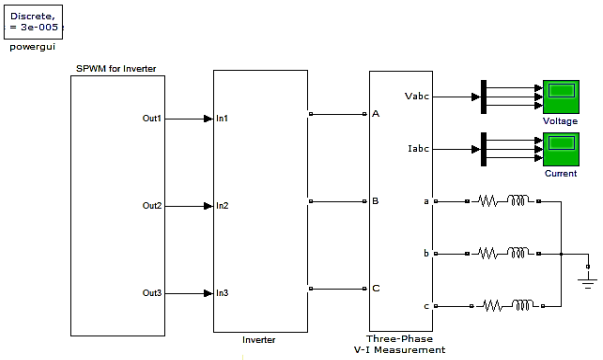


Figure 5. Diode clamped inverter model with RL Load

TABLE I. FIVE-LEVEL DCI SYSTEM PARAMETER

Parameters	Rating
Source (DC)	$400V$
DC link Capacitance	$R = 0.001$, $C = 5000\mu F$
DC side Inductance	$10mH$
AC side Load Resistance	10Ω
AC side Load Inductance	$1mH$

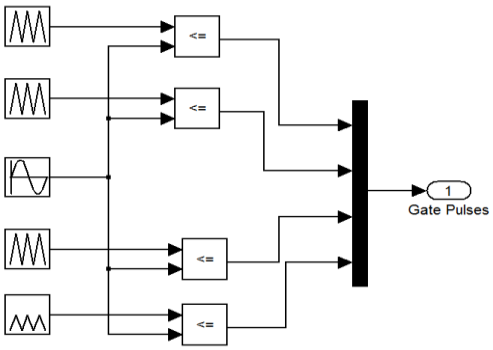


Figure 6. Carrier based pulse width modulation scheme.

The frequency of the triangular carrier signal is chosen to be 259 times the fundamental frequency which means that there will be a total of 259 carrier cycles in one entire cycle of the fundamental and the frequency of the modulating signal is set equal to 50 Hz with the dc-bus voltage for the five-level inverter taken as 400Volts at the modulation index 'm_a' equal to 0.9. The modulation index 'm_a' as defined earlier in this paper is the ratio of the amplitude of reference signal to theamplitude of carrier signal. The switching frequency of the inverter would be 12950Hz and the modulation index of the inverter would then be equal to 0.9.

The buck-boost balancing circuit for the capacitor voltage balancing is shown in fig. 7.

The phase voltage, line voltage and its normalized harmonic spectrum all taken when the fundamental frequencyis equal to 50Hz are shown in fig. 8 and fig. 9 respectively. It can be seen from thenormalized harmonic spectrum of the output voltage (fig. 8 & fig. 9) that harmonics are lower in the five-level inverter configuration.

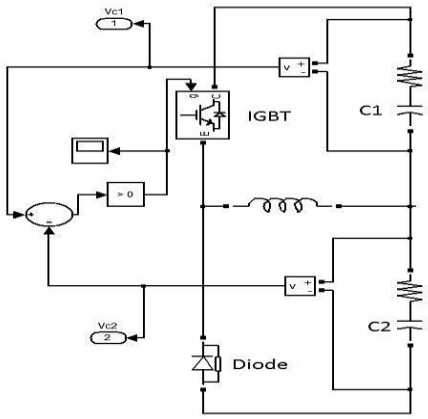
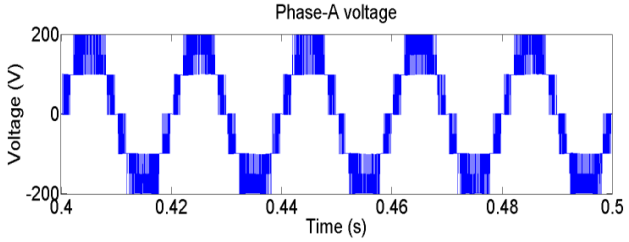
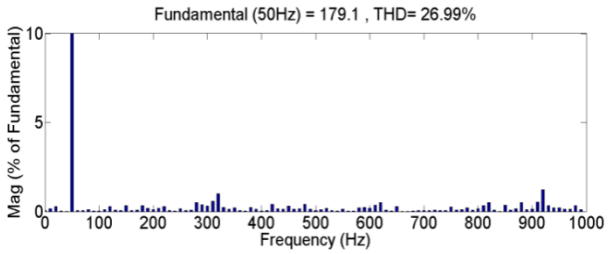


Figure 7. Buck-boost balancing circuit implemented in MatlabSimulink

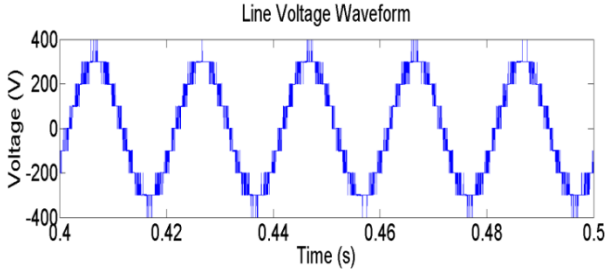


(a)



(b)

Figure 8. (a) Phase voltage & (b) its harmonic spectrum



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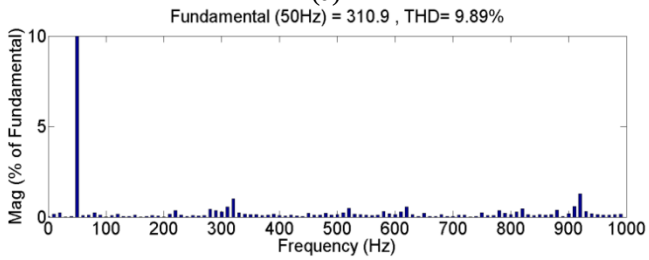
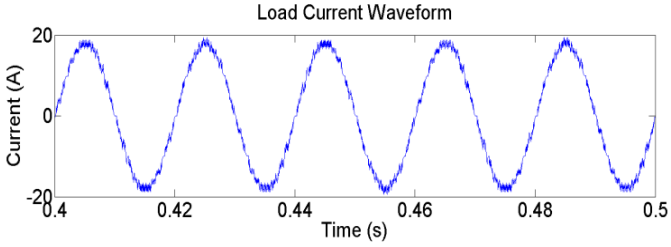


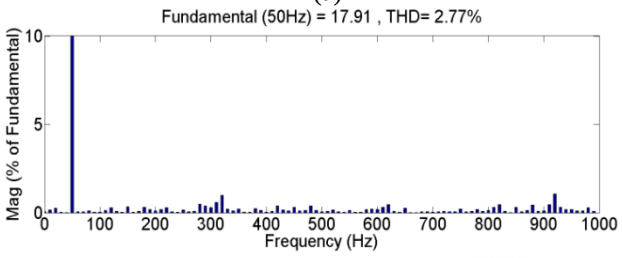
(b)

Figure 9. (a) Line-to-line voltage & (b) its harmonic spectrum

Hence, it demonstrated that the five-level diode clamped inverter is capable of generating multiple levels in its output. The principal advantage with this PWM scheme improved spectral performance. The current drawn from this five-level diode clamped inverter is shown in fig. 10, which generates almost sinusoidal current waveform. The total harmonic distortion (THD) of the output current as low as 2.77%.



(a)



(b)

Figure 10. Load current & (b) its harmonic spectrum

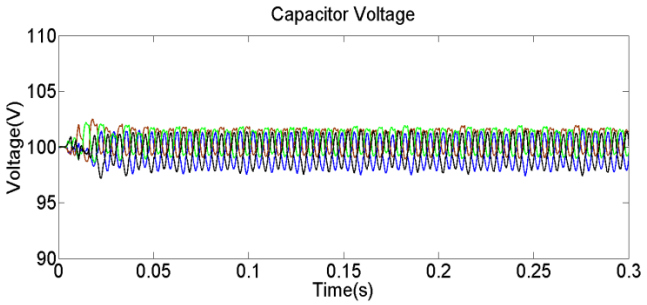


Figure 11. Capacitor voltage balanced at 100V

Each capacitor voltage of the five-level diode clamped inverter is balanced at 100V by using modulation scheme and buck-boost balancing circuit. The result of capacitor voltage balancing is shown in fig. 11.

v. Conclusion

In this paper, carrier based pulse width modulation scheme is proposed for five-level diode clamped inverter with resolving the voltage balancing problem. Carrier based pulsed width modulation method is used for the switching operation of the five-level diode clamped inverter switches demonstrating the multiple levels obtained from the inverter. The main issue of this paper that is voltage balancing problem is resolved by using buck-boost balancing circuit.

Through simulation studies, it is demonstrated that the harmonic profile of the phase voltage of the inverter improves with the use of carrier based pulsed width modulation scheme with proper utilization of dc-bus voltage by using balancing circuit, suggesting that the THD in the output voltage can be reduced.

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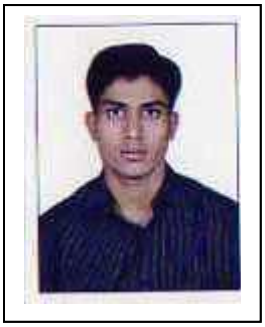

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