

To study and analyse Mixers under CMOS Technology

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Abstract

In this paper various mixers are defined for CDMA applications . Using CMOS makes easier for mixers to act on same chip with other digital and analog circuits . The topologies we are defining are dual gate mixers , back gate mixers, single balanced current switching mixers and back end mixers . The back-gate mixer utilizes the inherent lateral bipolar transistor in CMOS. Device simulations were performed to analyze the behavior of the lateral bipolar transistor and extract a model for it. The characteristic of the transistor were verified through measurements. The mixer circuit only draws 1.3 mW from a 1 V supply . Other mixers are also defined not only to achieve linearity , but also conversion gain and power dissipation.

Introduction

The back-gate mixer utilizes the inherent lateral bipolar transistor in CMOS. Device simulations were performed to analyze the behavior of the lateral bipolar transistor and extract a model for it. The characteristic of the transistor were verified through measurements. The mixer circuit only draws 1.3 mW from a 1 V supply

Configuration of Mixer	Conversion Gain (dB)		Input 1 dB Compression Point (dBm)		Noise Figure (dB)	Mixer Current (mA)
	Sim	Meas	Sim	Meas	Sim	Meas
Single Balanced CS	3.8	2.4	-9	-11.3	15.62	1.32
Single Balanced Cascode	4.5	4.7	-3.9	-14.6	14.5	1.43
Double Balanced CS	8.1	6.1	-5.2	-8.3	8.33	2.24
Double Balanced Cascode	6.7	6.9	-5.9	-13.3	10.04	2.18
Single Cascode	8	4.8	-12.2	-20.8	10	6.11

Mixer type	Signal input and output method	Characteristics	Comments & Applicable Device
Passive (LNA)	Single drive	<ul style="list-style-type: none"> Low conversion loss -4dB Low isolation Needs high LO power - 1 dB Needs 3 dB Poor spurious rejection Poor linearity 	Use for very high frequencies (i.e. millimeter waves)
	Sampling	<ul style="list-style-type: none"> Good linearity Low noise figure Low conversion loss Needs high LO power 	Only MESFET, Si BICMOS, Si CMOS
	Resistor	<ul style="list-style-type: none"> Very good linearity Full noise Low conversion loss -4dB Needs 3 dB Needs high LO power 	Only MESFET, Si BICMOS, Si CMOS
	Doubly-balanced	<ul style="list-style-type: none"> Low conversion loss Full isolation Needs high LO power Needs 3 dB higher LO power than single drive Good spurious rejection Needs 3 dB higher LO power than single drive Good linearity 	Difficult to integrate in a VLSI technology
Active (LNA)	Single-ended	<ul style="list-style-type: none"> Low conversion loss Low noise figure Low isolation Poor spurious rejection Needs diplexer and filter Needs high LO power 	<ul style="list-style-type: none"> Characteristics to receiver Only MESFET, Si BICMOS, Si CMOS
	Dual-Gate	<ul style="list-style-type: none"> Good isolation without filters Moderate conversion gain Moderate noise figure Low distortion Low LO power 	<ul style="list-style-type: none"> A nice start for low cost Good performance, especially commercial applications Only MESFET, Si BICMOS, Si CMOS
	Back-Gate	<ul style="list-style-type: none"> Very low power consumption High linearity High conversion gain Good isolation Low LO power 	Si CMOS
	Single-Matched	<ul style="list-style-type: none"> Essentially the same as single-ended mixer Low conversion gain 3 dB better SFP Needs isolation 	<ul style="list-style-type: none"> High performance IC applications where the number of transistors and the size of device is acceptable Only MESFET, Si BICMOS, Si CMOS
	Doubly-Matched	<ul style="list-style-type: none"> Essentially the same as single-ended mixer Low conversion gain 6 dB better SFP Needs isolation 	<ul style="list-style-type: none"> Essentially the same as the single-ended mixer, but better intermodulation rejection provided the mixer complexity and LO power Only MESFET, Si BICMOS, Si CMOS

Silicon MOSFET dual-gate mixers have been widely used in mobile and hand-held radio transceivers since the 1960s [1]. They exhibit good noise figures and reasonable conversion gains and most importantly, they allow the application of the two input signals to two separate gates thus making separate LO and RF matching possible thus avoiding passive couplers and simplifying the design. The inherent isolation between the gates of the two FETs also results in very good LO-to-RF isolation without the use of filters. A double balanced CMOS dual-gate mixer has been reported [4]. However, low voltage single ended dual-gate CMOS mixers have not been reported thus far. The absence of a theoretical distortion analysis makes it difficult to predict and optimize the intermodulation performance of such a mixer.

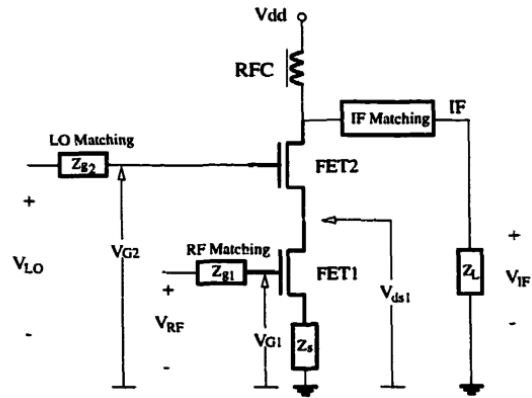


Fig 1.1 Dual Gate Mixer

Two MoSFETs (FET1 and FET2) are connected in a cascode configuration. The LO signal V_{to} is injected into the gate of FET2 while the RF signal V_{RF} is injected into FET1. The IF output signal V_w is accessed from the drain of FET2. Z_{g1} and Z_{g2} represent for the input matching networks associated with FET1 and FET2 respectively. Z_s is the source impedance associated with the source of FET1. "IF Matching" is the output matching network, and Z_L is the load usually 50 Q. RFC is the RF choke used to prevent the RF signal from flowing through the power supply V_{dd} to ground. V_{G1} and V_{G2} are bias voltages applied to the gates of FET 1 and FET2, respectively. The SOI devices have zero threshold voltages and the supply voltage chosen is 1 V.

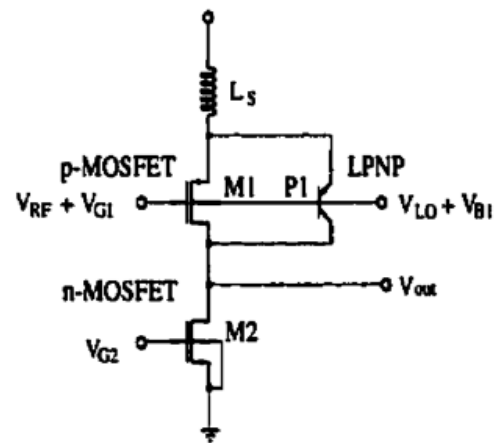


Fig 1.2 Back Gate Mixer

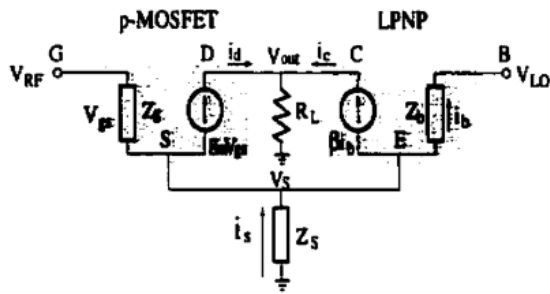


Fig 1.3 Back Gate Equivalent

A pMOSFET M 1 with an inherent LPNP P 1 is used as a four terminal device. The RF input signal V_w is applied to the gate of the MOSFET and the LO signal V_{LO} is fed to the substrate or base of the LPNP. The output signal V_{out} is accessed from the drain. V_{G1} and V_{DD} are the bias and supply voltages respectively. The n-MOSFET M2 acts as a load and the conversion gain of the mixer can be adjusted by changing its gate voltage V_{G2} . V_S is used to shift the ac voltage level at the source of M1, V_p is the signal voltage across Z_g which is the impedance associated with the gate of M1, g_m is the transconductance of M1, Z_s is the impedance of L_s , β is the current gain of P1 and Z_b is the impedance associated with the base of the LPNP. To simplify the circuit, the n-MOSFET is replaced by a resistor R_L . V_S is the voltage at the source of the M1.

1.3 Single Balanced Current-Switching Mixers

Mixers based on the multiplication of two signals exhibit superior performance as they ideally generate only the desired mixing products. Both the RF and LO signals are applied at different ports resulting in high degree of inherent isolation among all the three ports. Down-conversion mixers usually employ LO short at the IF port to achieve optimum IM performance. The LO short is practically important for the active mixers because LO signal is typically larger than the RF signal and it is further amplified by the active devices. The mixer that accommodates a differential LO signal and a single-ended RF signal is termed as single-balanced mixer.

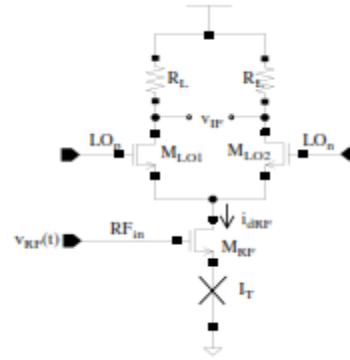


Fig 1.4 Single balanced Current Switching Mixers

In Figure the incoming RF voltage signal is first converted into a current signal and then multiplied in current domain. The FETs M_{LO1} and M_{LO2} are biased slightly above their threshold level. This results in the LO alternatively switching M_{LO1} and M_{LO2} on

and off. Consequently, one LO transistor is always on, while other LO transistor is ideally off, keeping the RF transistor in saturation. Hence, the LO signal can be considered as a square wave consisting of odd harmonics of the LO frequency. The magnitude of this signal should be large enough to ensure complete switching of the differential LO transistors. The RF input current signal is multiplied by the odd-order harmonics of LO signal, resulting in mixing products to appear at the output IF port.

1.4 Single Cascade Mixer

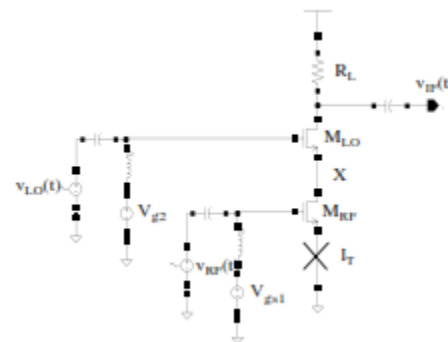


Figure shows a simple CMOS single-cascade mixer. The upper transistor has several effects on the mixer operation. Its primary use is to control the small signal transconductance of the lower device and

therefore, the RF gain of the device, making it useful as a mixer [6]. In addition, this configuration is well suited to CMOS technology since the drain and source of the two cascoded devices can be shared reducing capacitance at the common junction. It has been proved that the usual mode of operation is the one in which LO signal is applied to the top gate and the RF signal is fed to the lower gate [6-7]. This not only improves the LO ,RF-to-IF isolation but also enhances the linearity by allowing the use of standard port matching techniques for the RF signal. The applied LO signal modulates the common node voltage . The modulated node is the drain of M resulting in the mixing of LO and RF signal. The gate-source voltage of M RF is approximately constant because the RF signal is usually very small and the modulated drain-source voltage swings Min and out of linear and saturated regions of operation over the LO cycle. Frequency mixing occurs due to the modulated transconductance g_m and drain-source conductance g_{ds} of M. R_M remains in current saturation over most of the LO cycle, thus, it operates, simultaneously, as a source-follower amplifier for the LO and a common RF.

Conclusion

All these mixers are studied and defined to obtain better results in order to attain linearity, Conversion gain , slew rate, power dissipation and frequency .

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