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Carrier Recovery Circuit for Digital Keying for Non-Coherent Receivers

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Abstract*— An increasing majority of applications in electronics, as well as in most other technologies, use digital techniques to perform operations that were once performed using analog methods. The chief reasons for the shift to digital technology are that the digital systems are generally easier to design, Information storage is easy, Accuracy and precision are greater, Operation can be programmed, are less affected by noise, digital circuitry can be fabricated on IC chips.

The objective of this project is to build communication links using existing modulation blocks, constructed modulators and demodulator using operational function blocks based on their mathematical expressions, and conducted simulations of the links and modulators, all in tanner Tool to design a communication link.

Keywords— **FSK- Frequency Shift Keying, VCO- Voltage Controlled Oscillator, PD-Phase Detector, CP-Charge Pump, PLL-Phase Lock Loop**

Introduction

The transmission of digital signals is increasing at a rapid rate. Low-frequency analogue signals are often converted to digital format (PAM) before transmission. The source signals are generally referred to as baseband signals. Of course, we can send analogue and digital signals directly over a medium. From electro-magnetic theory, for efficient radiation of electrical energy from an antenna it must be at least in the order of magnitude of a wavelength in size; $c=f\lambda$, where c is the velocity of light, f is the signal frequency and λ is the wavelength. For a 1 kHz audio signal, the wavelength is 300km. An antenna of this size is not practical for efficient transmission. The low-frequency signal is often frequency- translated to a higher frequency range for efficient transmission. The process is called modulation. The use of higher frequency range reduces antenna size.

In the modulation process, the baseband signals constitute the modulating signal and the high-frequency carrier signal is a sinusoidal waveform. There are three basic ways of modulating a sine wave carrier. For binary digital modulation, they are called binary amplitude-shift keying (BASK), binary frequency-shift keying (BFSK) and binary phase-shift keying (BPSK). Modulation also leads to the possibility of frequency multiplexing. In a frequency-multiplexed system, individual signals are transmitted over adjacent, non-overlapping frequency bands. They are therefore transmitted in parallel and simultaneously in time. If we operate at higher carrier frequencies, more bandwidth is available for frequency-multiplexing more signals.

Modulation Types:

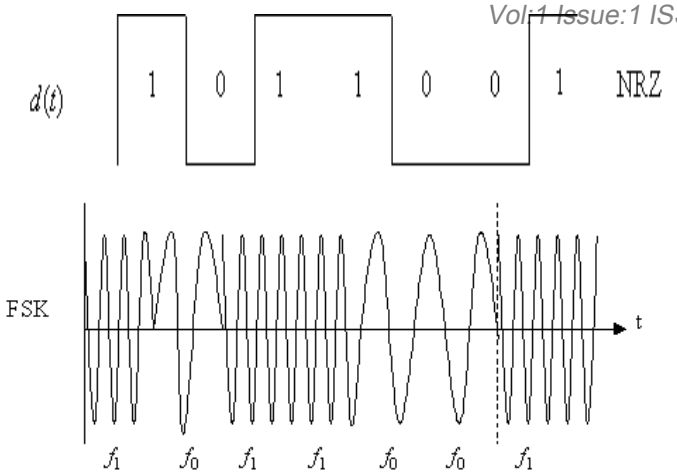

Fig. 1 Input and FSK signal

The fig. Illustrates the FSK methods of modulation for the case of a source supplying binary data. We can note following points:

Although in continuous-wave modulation it is usually difficult to distinguish between phase-modulated and frequency-modulated signals by merely looking at their waveforms, this is not true for PSK and FSK signals.

Unlike ASK signals, both PSK and an FSK signal has a constant image.

generation of Fsk

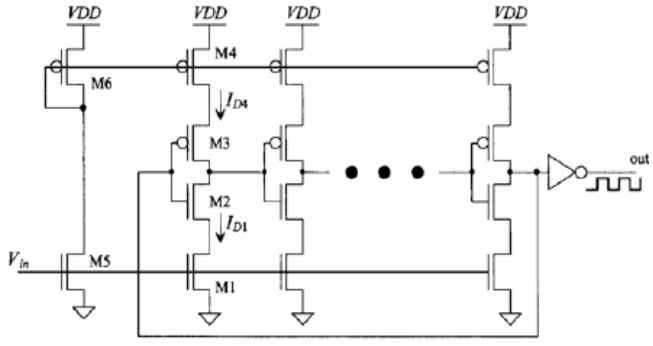

Fig. 2 Voltage Controlled Oscillator

To determine the design equations for use with the VCO, consider the simplified schematic of one stage of the VCO shown in fig. The total capacitance on the drains of M2 and M3 is given by

$$C_{tot} = C_{out} + C_{in} = \overbrace{C'_{ox}(W_pL_p + W_nL_n)}^{C_{out}} + \overbrace{\frac{3}{2}C'_{ox}(W_pL_p + W_nL_n)}^{C_{in}}$$

which is simply the output and input capacitance of the inverter. This equation can be written in a more useful form as

$$C_{tot} = \frac{5}{2}C'_{ox}(W_pL_p + W_nL_n)$$

The time it takes to charge C_{tot} from zero to VSP with the constant current Id4 is given by

$$t_1 = C_{tot} \cdot \frac{V_{SP}}{I_{D4}}$$

while the time it takes to discharge C_{tot} from VDD to Vsp is given by

$$t_2 = C_{tot} \cdot \frac{VDD - V_{SP}}{I_{D1}}$$

If we set Id4=Id1=Id (which we will label Idcenter when Vin=VDD/2), then the sum of T1, and T2 is simply

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N \cdot C_{tot} \cdot VDD}$$

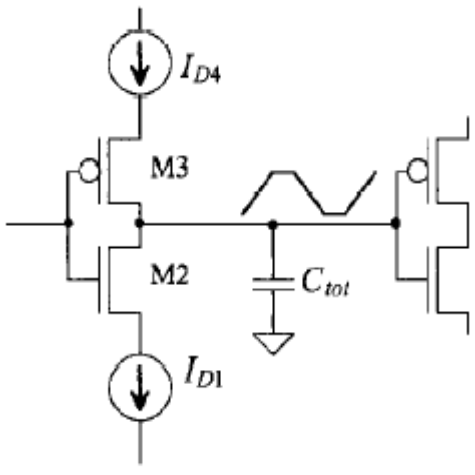

Fig. 3 Schematic of One Stage VCO

Last Equation gives the centre frequency of the VCO when ID=Idcenter.

generation of dIGITAL SIGNAL

It is used to demodulate the incoming FM/ FSK signal. Basic components of the PLL being as shown in the figure given below:

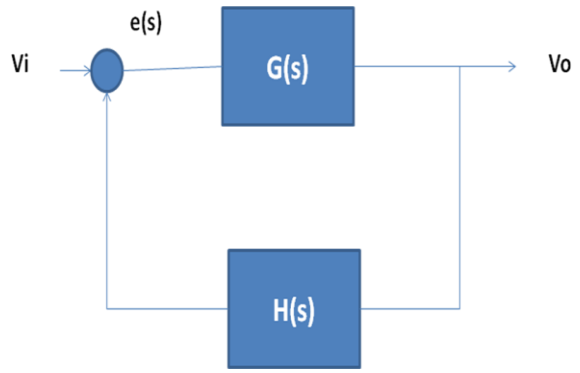

Fig .4 Standard negative-feedback control system model

A phase-locked loop is a feedback system combining a voltage-controlled oscillator and comparator also called phase detector so connected that the oscillator frequency can accurately track the frequency that is been applied. Phase-locked loop can be used to generate stable output frequency signals from a fixed low-frequency signal.

In general phase locked loop is been analyzed as a negative feedback system with forward gain term and a feedback term.

A simple block diagram of a voltage-feedback system is shown in fig.4

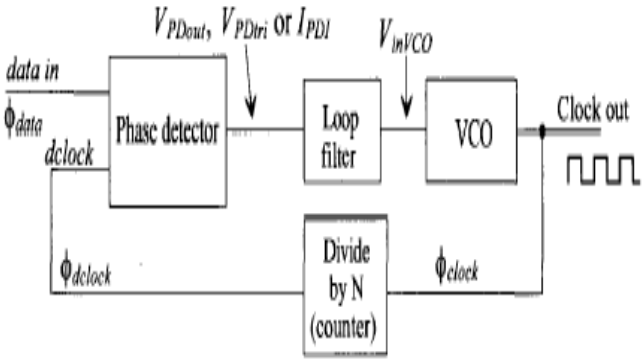

Fig. 5 Basic Phase-Locked-Loop Model

Components of a PLL that contribute to the loop gain include:

The *phase detector* (PD) and *charge pump (*CP).

The *loop filter*, with a transfer function of Z(s)

The *voltage-controlled oscillator* (VCO), with a sensitivity of KV/s

The *feedback divider*, 1/N

In this particular phase-locked loop, the error signal from the phase comparator is nothing but the difference between input frequency and that of the signal feedback. The system will now force the frequency error signal to zero in the steady state. The usual equations for a negative-feedback system can be given as,

Forward Gain=G(s), [s=jw=j2πf]

*Loop Gain=G(s) *H(s)*

$$\textit{Closed-Loop Gain} = \frac{G(s)}{1+G(s)\,H(s)}$$

Steady state gain because of the integration in the loop can be given as,

$$Vo/Vi = \frac{1}{H}\ , \text{(Closed Loop Gain)}$$

If a linear element like a four-quadrant multiplier is used as the phase detector, and the loop filter and VCO are also analog elements, this is called an analog or *linear PLL* (LPLL).

If a *digital* phase detector (EXOR gate or D flip flop) is used, and everything else stays the same, the system is called *a digital PLL* (DPLL).

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If the PLL is built exclusively from digital blocks, without any passive components or linear elements, it becomes an *all-digital PLL* (ADPLL).

Finally, with information in digital form, and the availability of sufficiently fast processing, it is also possible to develop PLLs in the software domain. The PLL function is performed

by software and runs on a DSP. This is called a *software PLL* (SPLL).

Referring to Figure 2, a system for using a PLL to generate higher frequencies than the input, the VCO oscillates at an angular frequency of w*D*. A portion of this frequency/phase signal is fed back to the error detector, via a frequency divider with a ratio 1/N. This divided-down frequency is fed to one input of the error detector. The other input in this example is a fixed reference frequency/phase. The error detector compares the signals at both inputs. When the two signal inputs are equal in phase and frequency, the error will be zero and the loop is said to be in a "locked" condition. If we simply look at the error signal, the following equations may be developed.

$$e(s)= F_{REF} - \frac{Fo}{N}$$

When

$$e(s)=0, \frac{Fo}{N} = F_{REF}$$

Thus,

$$Fo=N\ F_{REF}$$

In commercial PLLs, the phase detector and charge pump together form the error detector block. When *FO* not equal to *N FREF*, the error detector will output source/sink current pulses to the lowpass loop filter. This smooths the current pulses into a voltage which in turn drives the VCO. The VCO frequency will then increase or decrease as necessary, by *KV* D*V*, where *KV* is the VCO sensitivity in MHz/Volt and D*V* is the change in VCO input voltage. This will continue until *e*(*s*) is zero and the loop is locked. The charge pump and VCO thus serves as an integrator, seeking to increase or decrease its output frequency to the value required so as to restore its input (from the phase detector) to zero.

The phase transfer function is

$$H(s) = \frac{\phi_{clock}}{\phi_{data}} = \frac{K_{PDtri}K_F K_{VCO}}{s + \beta \cdot K_{PDtri}K_F K_{VCO}} \quad \text{.....1}$$

$$K_F = \frac{1 + sR_2C}{1 + s(R_1 + R_2)C}$$

When this filter is driven with the tri-state output, no current flows in R1 or R2 with the output in the high impedance state. The voltage across the capacitor remains unchanged. We can think of the filter, tri-state output as an ideal integrator with a transfer function

$$K_F' = \frac{1 + sR_2C}{s(R_1 + R_2)C}$$

Putting it in 1 we get :

$$H(s) = \frac{K_{PDtri}K_{VCO}\frac{1+sR_2C}{(R_1+R_2)C}}{s^2 + s\frac{K_{PDtri}K_{VCO}R_2C}{N(R_1+R_2)C} + \frac{K_{PDtri}K_{VCO}}{N(R_1+R_2)C}} = \frac{\phi_{clock}}{\phi_{data}} = \frac{f_{clock}}{f_{data}}$$

And the value for natural frequency is,

$$\omega_n = \sqrt{\frac{K_{PDtri}K_{VCO}}{N(R_1 + R_2)C}}$$

And gives damping factor as,

$$\zeta = \frac{\omega_n}{2} \cdot R_2C$$

The lock range is,

$$\Delta\omega_L = 4\pi\zeta\omega_n$$

while the lock time, TL, remains 2*pi/Wn. The pull-in range is limited by the VCO operating frequency. The pull-in time is given by:

$$T_P = 2R_1C \cdot \ln \frac{(K_{VCO}/N) \cdot (VDD/2)}{(K_{VCO}/N)(VDD/2) - \Delta\omega}$$

PFd with charge pump output

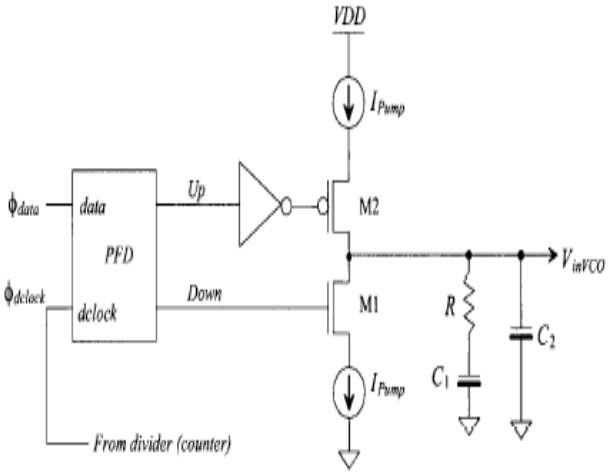

Fig. 8(a)

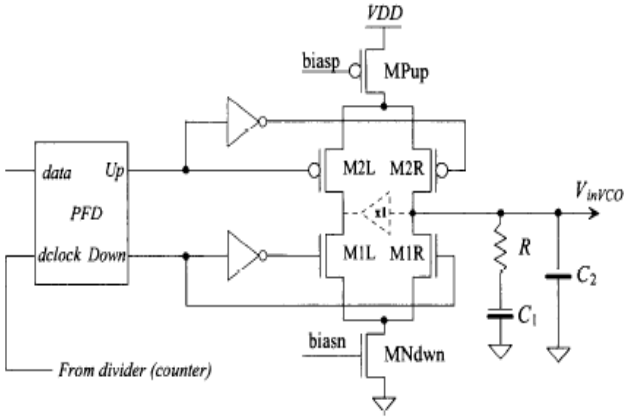

Fig. 8(b) A practical circuit for PFD with a Charge Pump Output

PHASE FREQUENCY DETECTOR

A schematic diagram of the phase frequency detector is shown in Fig d. The output of the PFD depends on both the phase and frequency of the inputs. This type of phase detector is also termed a sequential phase detector. It compares the leading edges of the *data* and *dclock.* A *dclock* rising edge cannot be present without a data rising edge.

The first thing we notice is that the *data* pulse width and the *dclock* pulse width do not matter. If the rising edge of the *data* leads the *dclock* rising edge, the "up" output of the phase detector goes high, while the *Down* output remains low. This causes the *dclock* frequency to increase, having the effect of moving the edges closer together. When the *dclock* signal leads the data (Fig. b), *Up* remains low, while the *Down* goes high a time equal to the phase difference between *dclock* and *data.* Figure c shows the condition of the locked loop. Notice that, unlike the XOR PD, the outputs remain low when the loop is locked. Again, several characteristics of the PFD can be described:

1. A rising edge from the *dclock* and *data* must be present when making a phase comparison.
2. The widths of the *dclock* and the *data* are irrelevant.
3. The PFD will not lock on a harmonic of the data.
4. The outputs *(Up* and *Down)* of the PFD are both logic low when the loop is in lock, eliminating ripple on the output of the loop filter.

RECEIVER SENSITIVITY

Receiver sensitivity specifies the ability of the receiver to respond to a weak signal. Digital receivers use maximum bit-error rate (BER) at a certain rf level to specify performance. In general, device gains, noise figures, image noise, and local-oscillator (LO) wideband noise all combine to produce an equivalent noise figure. This is then used to calculate the overall receiver sensitivity. Wideband noise in the LO can elevate the IF noise level and thus degrade the overall noise factor. For example, wideband phase noise at FLO + FIF will produce noise products at FIF. This directly impacts the receiver sensitivity. This wideband phase noise is primarily dependent on the VCO phase noise. Close-in phase noise in the LO will also impact sensitivity. Obviously, any noise close to FLO will produce noise products close to FIF and impact sensitivity directly.

Receiver selectivity specifies the tendency of a receiver to respond to channels adjacent to the desired reception channel. *Adjacent channel*

interference (ACI), a commonly used term in wireless systems, is also used to describe this phenomenon. When considering the LO section, the reference spurs are of particular

importance with regard to selectivity. Figure 13 is an attempt to illustrate how a spurious signal at the LO, having the same spacing as the channel-spacing frequency, can translate energy from an adjacent radio channel directly onto the IF. This is of particular concern if the desired received signal is distant and weak and the unwanted adjacent channel is nearby and strong, which can often be the case. So, the lower the reference spurs in the PLL, the better it will be for system selectivity.

I. ANALYSIS RESULTS OF FSK MODULATOR

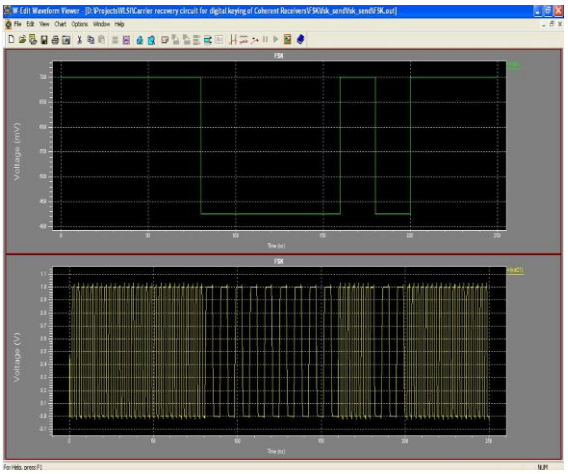

Fig. 4 Analysis of the FSK Modulator

CONCLUSION

In this first part of the paper, we have done the analysis of the FSK modulator. The analysis results shows that the Digital Signal is been modulated. This analysis is been done with the simple block diagrams and equations.

We have shown a typical example of where the PLL structure is used and given a detailed description of a practical implementation.

In the next installment, we will delve deeper into the specifications which are critical to PLLs and discuss their system implications.

REFERENCES

[1]Mini-Circuits Corporation,"VCO Designers Handbook."
[2] L.W. Couch, "Digital and Analog Communications Systems" Mscmillan Publishing Company, New York.
[3]P.Vizmuller, "RF Design Guide, "Artech House.
[4] R.L. Best," Phase Locked Loops: Design, Simulation and Applications," 3rd Edition, McGraw Hill.
[5] Mini-Circuits Corporation, *VCO Designers' Handbook*, 1996.
[6] L.W. Couch, *Digital and Analog Communications Systems*, Macmillan Publishing Company, New York, 1990.
[7] P. Vizmuller, *RF Design Guide*, Artech House, 1995.
[8] R.L. Best, Phase Locked Loop; Design, Simulation and Applications, 3rd edition, McGraw-Hill, 1997
[9]D.E. Fague "Open Loop Modulation of VCOs for Cordless Telecommunications, " RF Design, July 1994.
[10]D.B. Leeson, " A Simplified Model of Feedback Oscillator Noise Spectrum," Proceedings of IEEE,Volume 42,Feb.2002,oo 329-330.