Design of CMOS Current Comparator for High Speed and Low Power Applications

Manoj Kumar, Neelam Rani , Ramnish Kumar
Department of Electronics & Communication Engineering
Guru Jambheshwar University of Science & Technology, Hisar, India,
manojtaleja@yahoo.com, neelamguri30@gmail.com, contactram1@rediffmail.com

***Abstract*- This paper presents a CMOS current comparator with high speed and low power consumption having minimum circuit complexity. Circuit shows a low response time to provide high speed. SPICE is used to verify the circuit performance with a standard 0.5µm and 0.35 µm CMOS technology. Circuit with 0.5µm CMOS technology shows the propagation delay of 292.19 ps to 10.10 ns and total power dissipation of 12.19 mW to 854.69 nW for input current pulse of 1 mA to 1 µA. Similarly circuit with 0.35 µm CMOS technology shows the propagation delay of 390.15 ps to 20.223 ns and total power dissipation of 7.37 mW to 572.88 nW for input current pulse of 1 mA to 1 µA. Comparisons have been made with the earlier circuit for power dissipation and delay. It has been observed that present circuit shows better performance than previous circuit.**

Keywords: CMOS, current comparator, delay and low power.

I. Introduction

In recent years current mode signal processing using CMOS technology has gained great interesting circuit designing. With the shrinkage of feature size and increasing demand of high speed and low power application, the current-mode circuit has been considered to be an alternative to voltage-mode circuit. Current comparator is fundamental component of analog system because of better accuracy, low noise and low power consumption. It can be used in A/D converters, oscillators, current to frequency converters, VLSI neural network, sensor circuit and portable wireless communication etc. H. Traff [1] proposed the first high speed, low input impedance current comparator using a simple inverter. Traff's approach has been modified by a number of designs, A. T. K. Tang et al. [2] and L. Ravezzi et al.[3], where speed increases have been attained at the cost of an increase in power consumption. It is desirable that comparators must provide high speed and low power consumption. Conventional current comparator is based on high output-resistance cascaded current mirror which are connected as class AB stage. It amplifies the small input differences to large variation in output. The large capacitive loads in CMOS inverting stages are added to achieve rail-to-rail slewing and short transition time. The high output resistance will reduce the frequency performance. So operating frequency is limited by high output resistance. This places a serious restriction on the available processing for on-chip system where high dynamic range low-power circuits are essential.

A schematic of current comparator by C. B. Kushwah, et al. [4] is shown in Fig. 1. Here I_{in} represents the difference of the input currents, and V_{out} represents the output voltage result, which can be amplified by CMOS inverting stages.

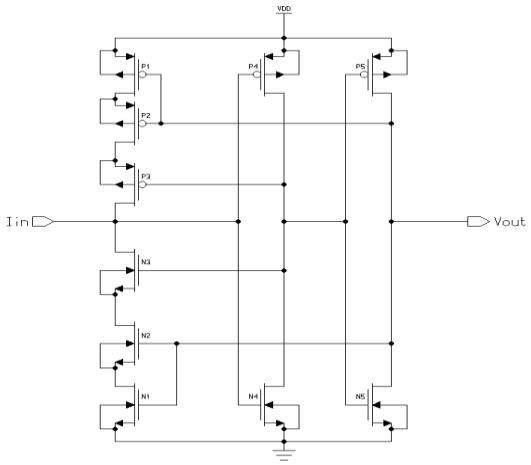

Figure 1. Schematic of current comparator [4].

To achieve the sufficient gain for amplifying the small voltage variations at input stage node, latched feedback system from CMOS inverters is used. The feedback operation of this circuit allows the input node to slew from rail to rail. So it increases the speed and consumes less power than the Traff circuit. Positive feedback operates at the output nodes of inverters P4/N4 and P5/N5, respectively. Transistors in series of P3 and N3 are speed up the decision process. Here transistors P1, P2 and N1, N2 have common latched feedback from inverter P5/N5. So it decreases the speed of operation at

low current decision. A modified design of current comparator for low power consumption and high speed is presented in this paper. This paper is organised as: In Section 2 the modified current comparator circuit has been presented and working has also been explained. In Section 3 the results of modified circuits have been obtained and compared with earlier reported circuits. Finally Section 4 concludes the work.

II. Circiut Description

A schematic of modified design is shown in Figure.2.

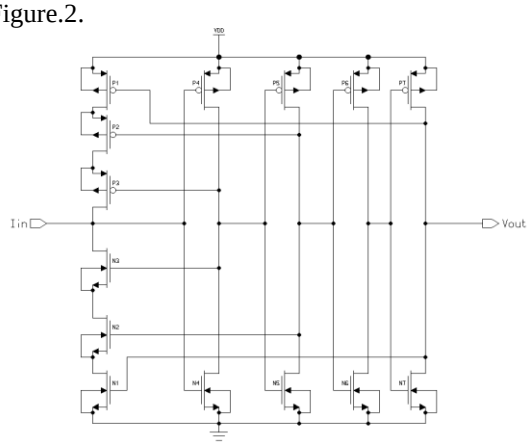

Figure 2. Schematic of proposed current comparator

In this circuit, redesigned feedback system has been used that allows high-speed operation at low current decision. Here we have added two more inverters P6/N6 and P7/N7 to improving the feedback system. Positive feedback operates at the output nodes of the inverters P4/N4, P5/N5 and P7/N7 respectively. In the pre-decision state transistors N3 and P3 are closed and transistors P1, P2 and N1, N2 are open. As the voltage on the comparator node is affected by input current so the inverter begins to switch. As this slew to either rail the transistors P3 or N3 are switched open, and then with a delay of few nano seconds the transistor P2 or N2 is switched closed. The input of inverter P7/N7 is affected by output of inverter P6/N6. So the transistor P1or N1 is also switched closed after delay of some nano seconds. This redesigned latched feedback system dumps enough charge on the comparator node to significantly speed the design process, particularly at low input current. The chip area of the comparator is maintained by reducing the size of all transistors. It also reduces the power consumption.

III. Results And Discussion

In order to demonstrate the effectiveness of the circuit, SPICE is used to simulate the proposed circuit using 0.35µm and 0.5µm CMOS process with 3V supply voltage. Proposed circuit has less delay as compared to earlier existing circuits. Figure 3 shows the result of earlier work done by [4] and Figure 4 shows the simulation result of proposed circuit with applied input current pulse of 1mA. We have also reported the results for delay considering applied input current pulse of 1mA to earlier design and present design in Figure 5 & 6. Results of output voltage with applied input current pulse of 100µA for circuit [4] and present circuits has been shown in Figure 7& 8. Results of output delay with applied input current pulse of 100µA for circuit [4] and present circuits has been shown in Figure 9& 10.

Similarly Figure 11& 12, shows the results of output voltage with 10µA current. Figure 13& 14 shows the delay results for 10µA current. Figure 15&16 shows the results of output voltage for 1 µA. Figure 17& 18 reports delay by [4] and present design with 1 µA. From Figure 4, 8, 12 & 16 it has been observed that the present design have better output results than earlier design. Similarly from Figure 6, 10, 14& 18 we conclude that the proposed circuit has got less delay and higher speed. Table I shows the comparison of the results by earlier design [4] and present design considering delay, total power dissipation and maximum slew rate with 0.5 µm CMOS technology. Table II shows the comparison of the results by earlier existing design [4] and present design considering delay, total power dissipation and maximum slew rate with 0.35 µm CMOS technology.

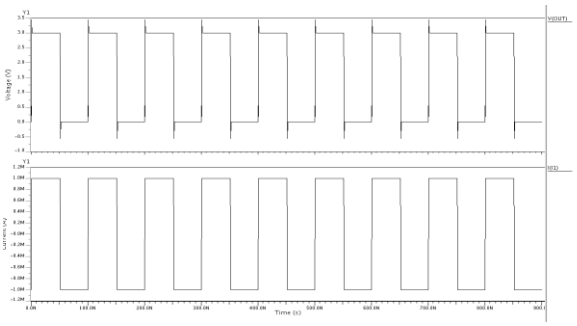

Figure 3. Voltage at output node with current pulse of 1mA in 0.5 µm technology [4]

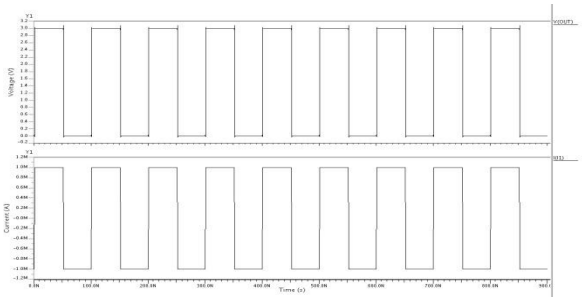

Figure 4. Voltage at output node with input current pulse of 1mA with 0.5 µm technology (present work)

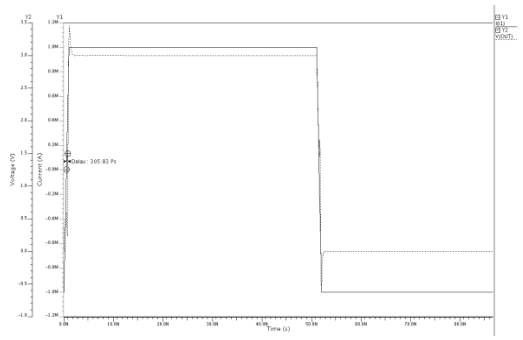

Figure 5. Delay with input current pulse of 1 mA with 0.5 µm technology [4]

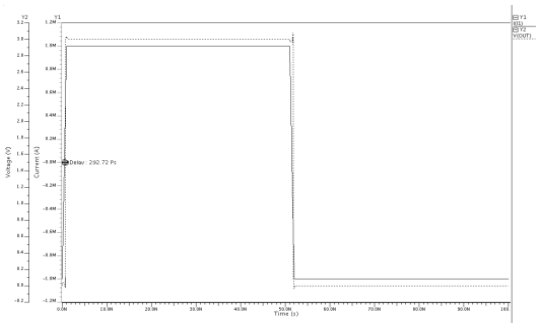

Figure 6. Delay with input current pulse of 1 mA with 0.5 µm technology (present work).

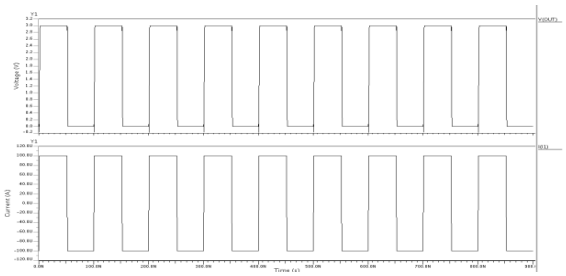

Figure 7. Voltage at output node with applied input current pulse of 100 µA with 0.5 µm technology [4]

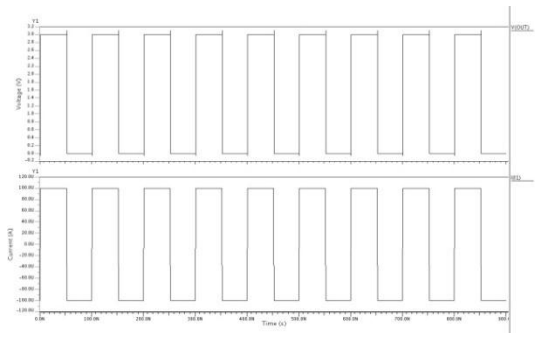

Figure 8. Voltage at output node with applied input current pulse of 100 µA with 0.5 µm technology (present work).

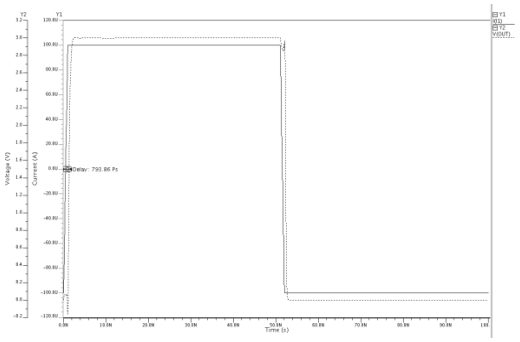

Figure 9. Delay with input current pulse of 100 µA with 0.5 µm technology[4].

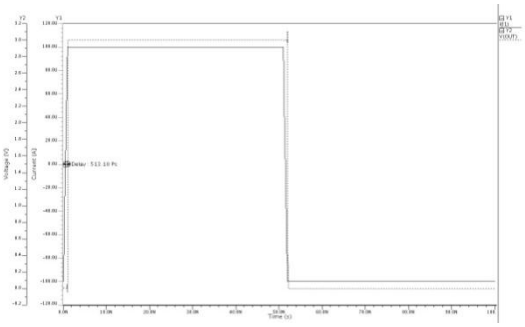

Figure 10. Delay with input current pulse of 100 µA with 0.5 µm technology (present work).

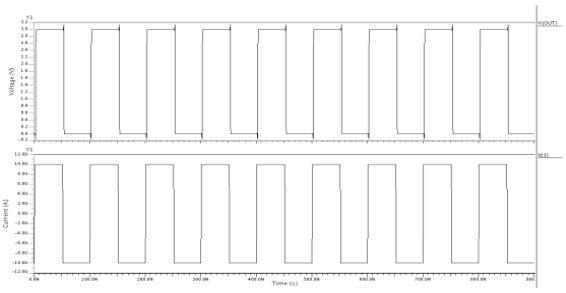

Figure 11. Voltage at output node with applied input current pulse of 10 µA with 0.5 µm technology [4].

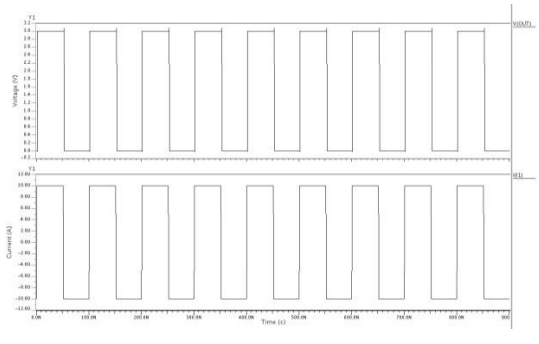

Figure 12. Voltage at output node with applied input current pulse of 10 µA with 0.5 µm technology (present work).

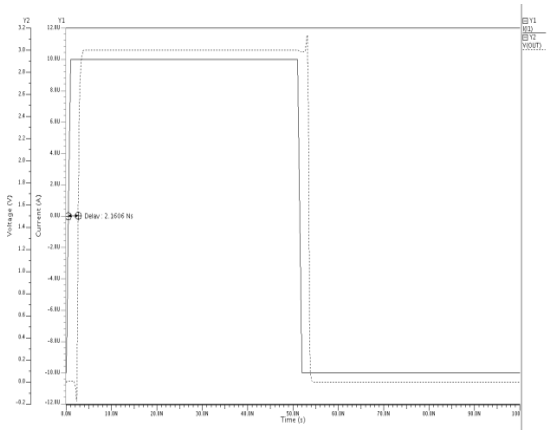

Figure 13. Delay with input current pulse of 10 µA with 0.5 µm technology[4].

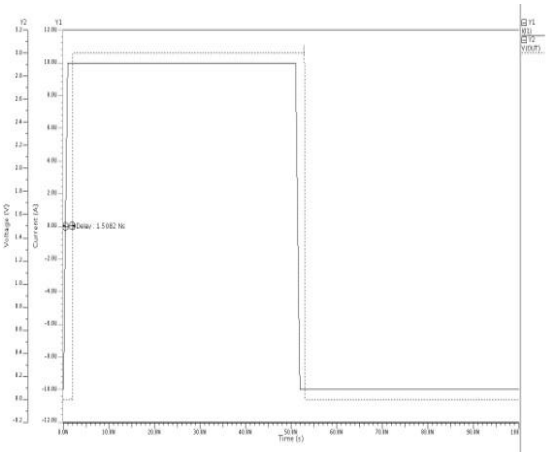

Figure 14. Delay with input current pulse of 10 µA with 0.5 µm technology (present work).

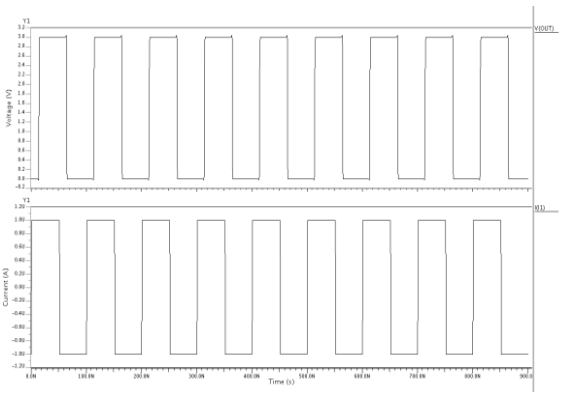

Figure 15. Voltage at output node with applied input current pulse of 1µA with 0.5 µm technology [4].

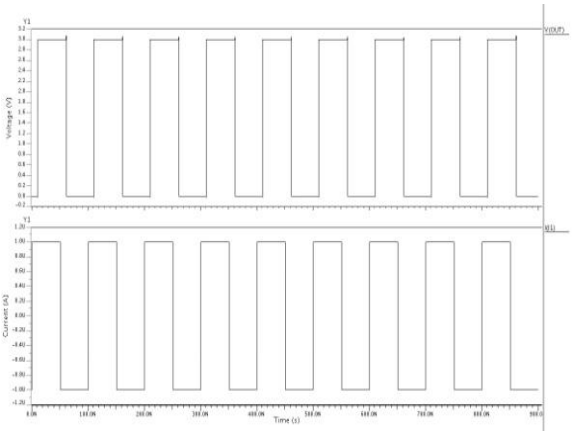

Figure 16. Voltage at output node with applied input current pulse of 1µA with 0.5 µm technology (present work)

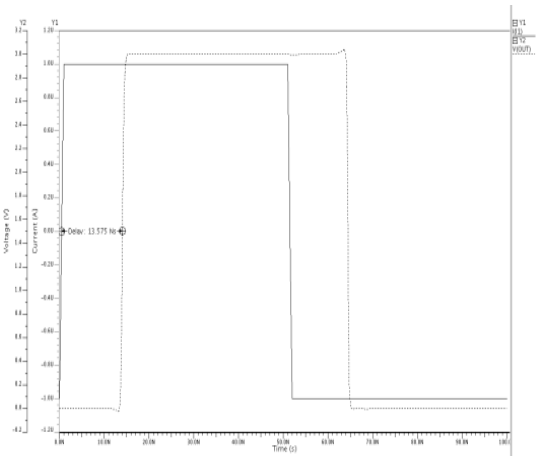

Figure 17. Delay with input current pulse of 1 µA with 0.5 µm technology [4].

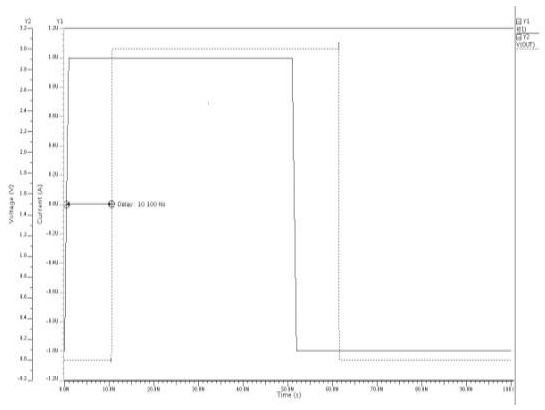

Figure 18. Delay with input current pulse of 1 µA with 0.5 µm technology (present work).

TABLE I. SIMULATION RESULTS FOR DELAY, TOTAL POWER DISSIPATION AND MAXIMUM SLEW RATE WITH 0.5 μm CMOS TECHNOLOGY.

Input Current	*50% propagation delay(from 50% of input to 50% of output) of present design*	*50% propagation delay(from 50% of input to 50% of output) of design [4]*	*Total power dissipation of present design*	*Total power dissipation of design [4]*	*Maximum Slew Rate of present design V/ns*	*Maximum Slew Rate of design [4] V/ns*
1 mA	0.292 ns	0.305 ns	12.19 mW	15.45 mW	30.849	3.191 V/ns
100 μA	0.513 ns	0.793 ns	248.38 μW	307.53 μW	22.719	1.865 V/ns
10 μA	1.51 ns	2.161 ns	10.87 μW	12.27 μW	6.99	1.643 V/ns
1 μA	10.10 ns	13.58 ns	854.69 nW	957.92 nW	6.041	1.584 V/ns

TABLE II. SIMULATION RESULTS FOR DELAY, TOTAL POWER DISSIPATION AND MAXIMUM SLEW RATE WITH 0.35 μm CMOS TECHNOLOGY.

Input Current	*50% propagation delay(from 50% of input to 50% of output) of present design*	*50% propagation delay(from 50% of input to 50% of output) of design [4]*	*Total power dissipation of present design*	*Total power dissipation of design [4]*	*Maximum Slew Rate of present design V/ns*	*Maximum Slew Rate of design [4] V/ns*
1 mA	0.390 ns	0.504ns	7.32 mW	10.71 mW	24.779	6.5 V/ns
100 μA	0.729 ns	1.150 ns	156.32 μW	214.48 μW	17.292	1.861 V/ns
10 μA	2.683 ns	4.308 ns	7.66 μW	8.99 μW	12.168	1.592 V/ns
1 μA	20.223 ns	30.211 ns	572.88 nW	612.37 nW	11.070	0.655 V/ns

IV. Conclusion

A modified current comparator, featuring low power consumption, high speed and maximize slew rate has been presented. SPICE is used to verify the circuit performance. Simulation results show the less propagation delay, low power dissipation with applied input current pulse of 1mA to 1μA for present design. As the proposed circuit shows enhanced performance in a low current range and give less power dissipation. This circuit is suitable for a high-speed circuit realization that includes current detection or data conversions. Comparison of results have been reported here with earlier design [4] and present design This work is an extension of earlier work on current comparator design.

References

[1] H. Traff, " Noval approach to high speed CMOS current comparator," Electron. Letter, vol. 28, no. 3, pp. 310- 312, Jan.1992.

[2] A.T K. Tang and C. Toumazou, "High performance CMOS current comparator," Electron. Letter, vol. 30, pp. 5-6, 1994.

[3] L. Ravezzi, D. Stoppa and G. F. Dalla Betta, "Simple High speed CMOS current comparator," Electron.Letter, vol.33, pp.1829-1830,1997.

[4] C. B. Kushwah, D. Soni and R. S. Gamad, "New design of CMOS Current comparator," Second International Conference on Emerging Trends in Engineering and Technology, ICETET, pp. 125-129, June, 2009.

[5] D. J. Banks and C. Toumazou, "Low-power high-speed Current Comparator Design," Electron. Letter, vol. 44, no.3, pp.171-172, Jan. 2008.

[6] Lu Chen, Bingxue Shi and Chun Lu, "A Robust High-Speed and Low-power CMOS Current Comparator Circuit," IEEE Asia-Pacific Conf. On Circuits and Systems, pp. 174-177, 2000.

[7] S. Rahul, F. L. Richard and M. Carver, "A Low Power Wide Dynamic-Range Analog VLSI Cochlea," Analog Integral Circuits Signal Process, vol. 16, pp. 245– 274, 1998.

[8] P. F. Ruedi, P. Heim, F. Kaese, E. Grenet, F. Heitger, P. Y. Burgi, S. Gyger and P. Nussbaum, "A 128X128 pixel 120 dB dynamic-range vision-sensor chip for image contrast and orientation extraction, " IEEE Journal Solid-State Circuits, vol. 38,pp. 2325-2333, 2003.