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A Low-Power Circuit Technique for Dynamic CMOS Logic

Preetisudha Meher
Dept. of Electronics and Telecommunication
National Institute of Technology
Rourkela, India
Preetisudha1@gmail.com

Kamala Kanta Mahapatra
Dept. of Electronics and Telecommunication
National Institute of Technology
Rourkela, India
kmaha@gmail.com

***Abstract*-- Dynamic logic style is used in high performance circuit designs because of its faster speed and lesser transistor requirement as compared to static CMOS logic style. Dynamic logic has inherent disadvantages like less noise immunity and high power consumption. In this paper we have proposed a novel circuit technique for implementing dynamic gate. The proposed circuit has very less power dissipation with almost same noise immunity compared to the recently proposed circuit techniques for dynamic logic styles to improve noise immunity. The concept is validated through extensive simulation.**

***Keywords*-- Domino logic, dynamic logic, power consumption, leakage tolerance, robustness.**

I. INTRODUCTION

Dynamic logic is used in the implementation of logic circuit for high speed designs such as data path in microprocessor [1]. However, it is not widely used because of its disadvantages like less noise robust and more power consuming compared to static logic style [2]. Domino logic is made by adding one inverter at the output of the dynamic gate. Domino gate has got advantage over the dynamic gate because fan-out of former is driven by inverter which has low output impedance and thus increases the noise immunity of the gate along with decreasing the output capacitance [3]. Figure 1 shows the standard domino logic style. Keeper transistor is used to maintain the logic one in the evaluation phase (CLK goes high) when there is charge leakage from the dynamic node through the pull down network (PDN). When PDN is ON in the evaluation phase dynamic node is discharged to zero through the PDN and evaluation transistor. Output inverter starts switching from zero to one and the keeper transistor starts turning OFF from ON. During this period there is static power dissipation from Vdd to Gnd.

During the evaluation phase small noise-signal at the input(s) of dynamic gate can change the desired output because of discharge of dynamic node. In worst case the circuit becomes very less noise-tolerant in case of high-fan in OR gate implementations.

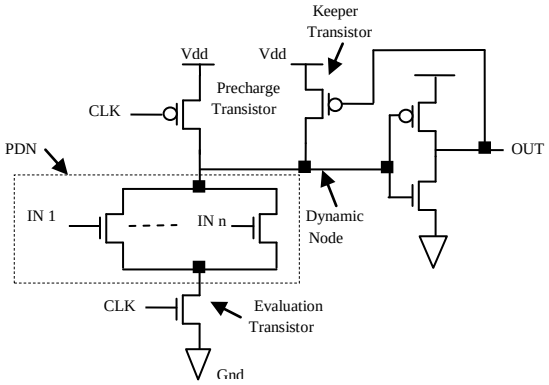


Figure1: Standard Domino OR gate.

Noise robustness can be improved by upsizing the keeper transistor (making wider) which makes keeper (PMOS) more conducting and thus maintains the charge at the dynamic node [4]. But this comes at the cost of static power dissipation which flows from Vdd to Gnd through keeper transistor when noise signal arrives at one of the inputs. To make dynamic circuit more noise robust different circuit styles have been proposed [4-9].

In this paper we have presented a novel circuit scheme for the domino logic. When compared with the recent proposals, the proposed circuit scheme has better noise-tolerance and very less power consumption.

The rest of the sections are organized as follows. Some related works for noise robustness in domino logic are described in section II. Section III presents the novel domino circuit approach and simulation results and comparisons are discussed in section IV. Conclusions are presented in Section V.

II. RELATED WORKS

Figure 2 shows the circuit technique proposed in [4] to improve the noise–tolerance. This technique increases the leakage immunity by a footer transistor in a diode configuration and improves the performance by employing a current mirror technique in the evaluation network. The diode footer transistor

has voltage drop across it because of leakage in evaluation phase. This voltage drop makes the gate-to-source voltage of the OFF evaluation transistor negative causing the exponential reduction of subthreshold leakage current. But this comes at the cost of performance degradation. This performance degradation is balanced by using mirror transistor. This mirror transistor mirrors the evaluation current and hence improves the performance by the draining current from the dynamic node.

Domino circuit to improve noise tolerance proposed in [5] is shown in Figure 3. At the beginning of the evaluation phase node C is at 0 V. Noise glitches at the input temporarily increases the gate-to-source voltage of the corresponding NMOS in PDN. Increase in the subthreshold current increases the charging of node C. During this process, gate-to-source voltage of the active NMOS decreases and the subthreshold leakage current is exponentially reduced.

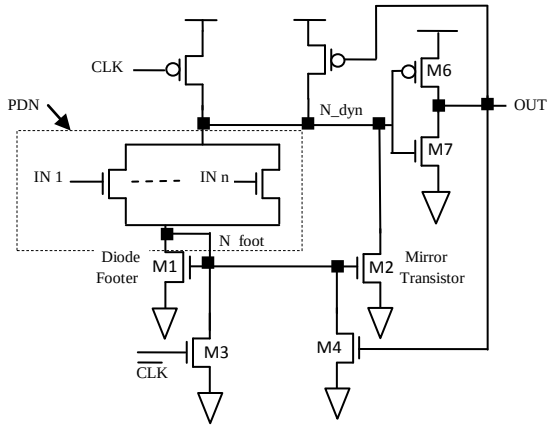


Figure 2: Diode footed domino [4]

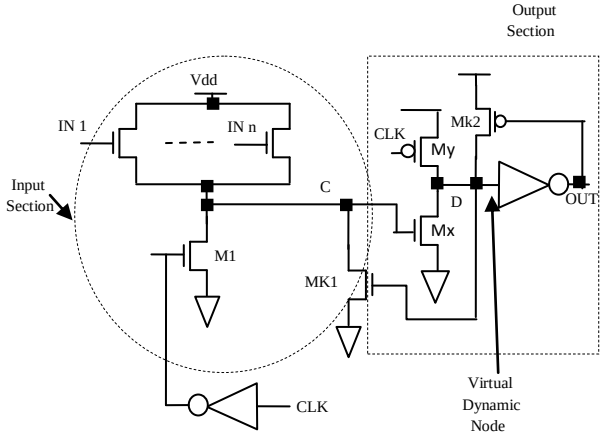


Figure 3: Domino style proposed in [5]

III. PROPOSED DOMINO CIRCUIT SCHEME

The proposed novel domino circuit scheme is shown in Figure 4. Transistor M1 is used as diode. Due to voltage drop across M1, gate-to-source voltage of the NMOS transistor in the PDN decreases (stacking effect [10]). The proposed circuit differs from [4] as it has additional evaluation transistor M5 with gate connected to the CLK. In [4], when M1 has voltage drop due to presence of noise-signals, M2 starts leaking that causes the circuit to dissipate power and also makes it less noise robust. The purpose of M5 in proposed scheme causes the stacking effect and makes gate-to-source voltage of M2 smaller (M2 less conducting).

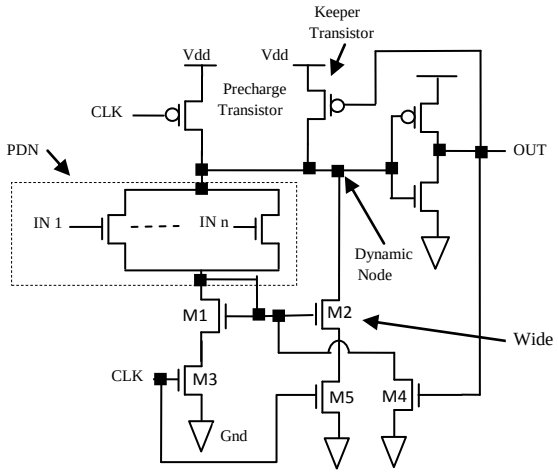


Figure 4: Proposed domino circuit scheme

Hence circuit becomes more noise robust and less leakage power consuming. But for performance degrades because of stacking effect in mirror current path. This can be increased by widening the M2 (high W/L) to make it more conducting.

IV. SIMULATION RESULTS, COMPARISONS AND DISCUSSIONS

Circuits are simulated using HSPICE simulator at temperature of 25 degree Celsius with PTM model card BSIM4 in 45 nm technology for bulk CMOS [11]. Channel length and width taken for simulations are 0.05 um and 0.06 um. Supply voltage Vdd used is 1.8 V. For the noise–tolerance measurement, noise immunity metric, unity noise gain (UNG) is used [4, 5]. Noise pulse width 125 ps (higher than gate delays) are taken and noise-voltages are applied to all inputs. TABLE I shows the UNG normalized to Vdd=1V and power-delay product (PDP) for different schemes of OR gate with fan-in of 2.

Transistor M2 plays a crucial role in terms of leakage and performance of gate in the proposed scheme. Its high width improves the performance but penalty paid is less noise robustness and slightly more power consumption.

TABLE 1: UNG of Different Styles for 2 INPUTS OR Gate with Vdd Normalized to 1.0 Volt

Scheme	UNG (mV)	Power (uW)	Delay (Sec)	PDP
Diode footed domino proposed in [4]	478	38.1	2.72E-11	1.036 E-15
Domino proposed in [5]	812	81.2	4.18E-11	3.394 E-15
Proposed domino (W/L = 0.12um/0.05um for M2)	772	7.4	4.72E-11	3.492 E-16

TABLE 2 shows the UNG, power and delay measurements for various widths of M2. With the increased size of keeper transistor there is very high increase in UNG at slightly more power consumption but high increase in delay as shown in TABLE 3.

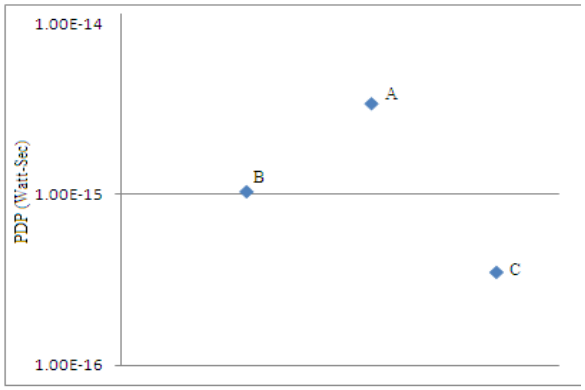


Figure 5. PDP Comparison of proposed circuit with other circuits

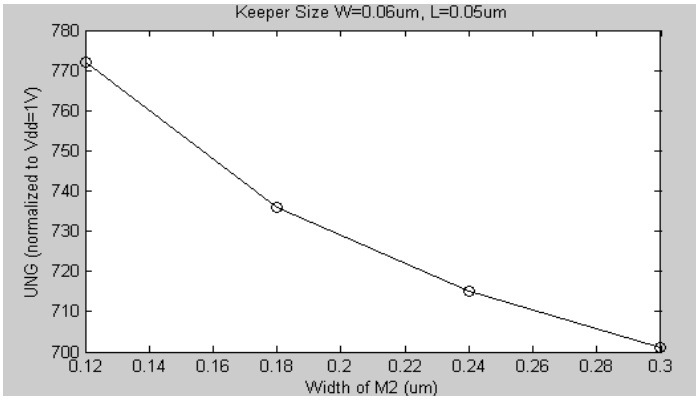
Also, there is increase in UNG as fan-in increases as shown in figure 7. Figure 8 shows the output waveforms obtained in implementation of 2 input OR gate using proposed scheme. It is evident that when width of M2 is less (W/L=1) there is no proper conduction from the dynamic node to ground to discharge the dynamic node. When width of M2 increases (W/L=1.5), proper conduction path is established to discharge the dynamic node and full swing output is obtained.

TABLE 2: UNG and Performance Measurements for Different Width of M2 in Proposed Domino Scheme

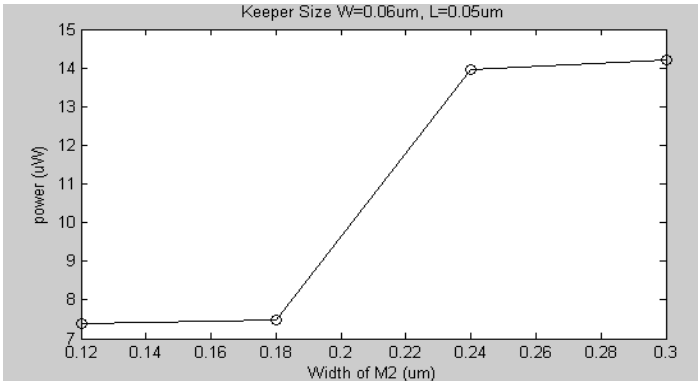
Width of M2	UNG (normalized to Vdd=1V)	Power (uW)	Delay (ps)
0.12 um	772	7.4	87.2
0.18 um	736	7.49	68
0.24 um	715	13.95	68
0.30 um	701	14.2	62.9

TABLE 3: UNG, POWER and Delay Measured at Different Keeper Transistor Width in Proposed Scheme With Width of M2=0.18um

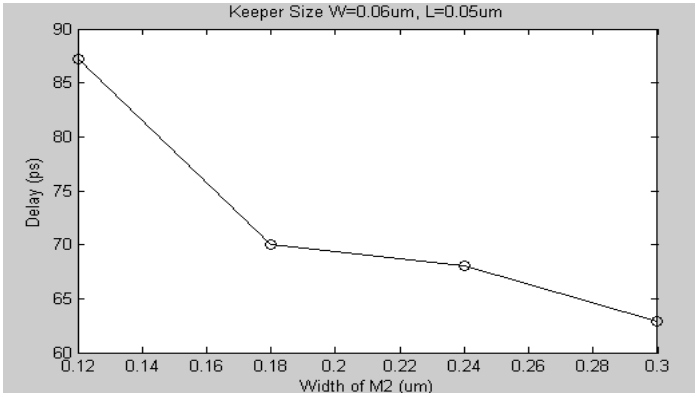
Width of Keeper transistor	UNG (normalized to Vdd=1V)	Power (uW)	Delay (ps)
0.06 um	736	7.49	68
0.07 um	791	7.72	115



(a)



(b)



(c)

Figure 6. (a) UNG (normalized to Vdd=1V) ,(b) power and (c) delay for various values of M2 width.

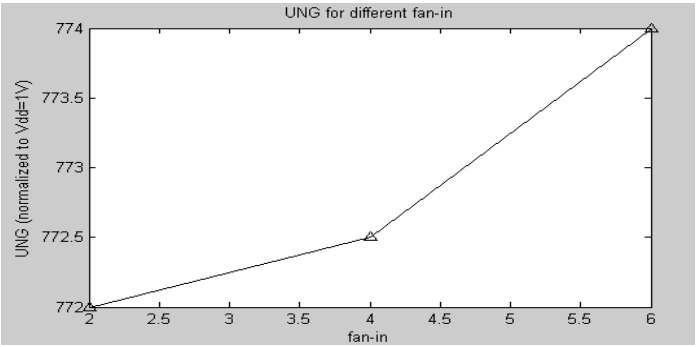
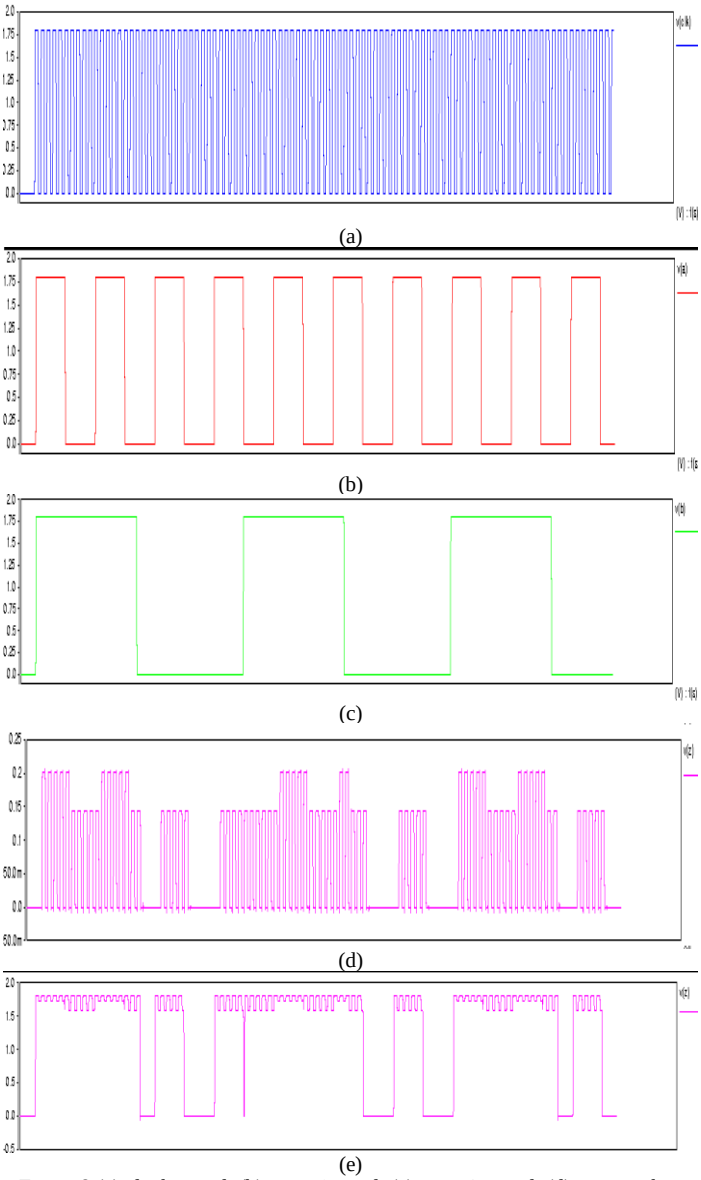


Figure 7. UNG values normalized to Vdd=1V for different fan-in



(a)

(b)

(c)

(d)

(e)

Figure 8.(a) clock signal, (b) input 1signal, (c) input 2 signal, (d) output when width of M2=0.06um and length=0.05um and (e) output when width of M2=0.12um and length=0.05um in proposed scheme.

5. CONCLUSION

A novel circuit scheme for the domino logic is proposed. The proposed circuit style is simulated using HSPICE simulator using 45 nm PTM for bulk CMOS model card. Proposed scheme when compared with the recent proposals shows high power savings as well as less power-delay product with almost same noise immunity. Furthermore, UNG increases as fan-in increases. The proposed circuit can be used in design of high-speed embedded processors where low power consumption is an essential requirement.

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