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Low power, High speed & Large Gainbandwidth three stage Operational Amplifier

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***Abstract*—The paper describe the two stage operational amplifier basic topology to get fast slew rate and large gain bandwidth product design. This has the large output current and the fast settling time for output. The circuit is design using .18 micron technology.**

***Keywords*—Opamp, GBWP, Slew rate.**

I. Introduction

Analog CMOS design becomes more difficult especially in the present age of nanometer technology. This, in itself, poses major problems in design and with the emergence of the nanometer technology, more problems arise. These problems make design process and implementation more difficult than it is in previous CMOS technologies. Fundamentals like power management, circuit integrity, rule-based physical verification, and parasitic extraction may not just be enough. A designer's strategy must shift from basic and fundamental design techniques to new and optimal design methods which may require changing the design itself.

The presented design using .18 micron technology describe the two stage operational amplifier design. It has advantageous parameter like low power dissipation, large gain bandwidth product, fast switching and settling characteristics of the operational amplification. It also has the large unity gain frequency. But as discussed in previous paragraph we also got difficulties to maintain the PSRR. The one more advantage in that design is the input and output current difference. It gives a large current so it can be used in high current application also.

II. CIRCUIT DESCRIPTION

The CMOS low power operational amplifier shown below was designed to study the behavior and connections between the different parameters and achieve the specifications and, in general, is a low power, moderate gain, high slew rate and fast settling time operational amplifier consisting of three stages.

The first stage provides of the biasing circuitry for the amplifier. Transistors MNMOS_8 and MNMOS_9 provide the gate bias voltage of transistor M9 and, in doing so, sets its "on" resistance. Transistors MNMOS_5, MNMOS_6 and MNMOS_7 are simply used to decrease the voltage drop across this stage and sets the current. This current sets the gate voltage of transistor MNMOS_4, and this gate voltage is used as a gate bias voltage for the transistor current sources, MPMOS_1 and MPMOS_5, which bias the second and third stages of the amplifier..

The second stage of the amplifier is the first gain stage and provides the differential input for the op-amp. Transistors MPMOS_1 and MPMOS_2 are the drivers for this stage, with MNMOS_1 and MNMOS_2 acting as the active current mirror load for this first stage. The high output resistances of these transistors provide a high gain for this stage, and its single ended output feeds the second gain stage.

The last stage is the second gain stage and consists of transistors MNMOS_3 and MPMOS_5. The NMOS transistor MNMOS_3 is the driver with MPMOS_5 acting as the load. Again, the high output resistances of these two transistors equate to a relatively large gain for this stage and an overall moderate gain for the complete amplifier.

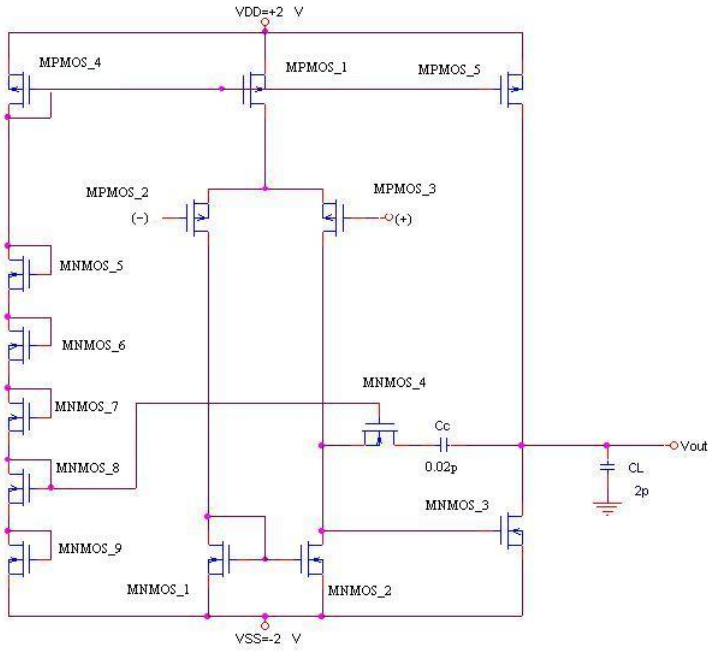

Figure 1 The complete CMOS operational amplifier circuit

The large gain of the last stage is further utilized in the compensation of the amplifier via the capacitance Cc.

Without compensation, the op-amp will oscillate in feedback circuits with a high loop gain. By taking advantage of the Miller Effect and the high resistance at the drain of MPMOS_2, a smaller value for the capacitance Cc is used than would be needed otherwise. However, due to the low transconductance of MOSFETS, the transistor MNMOS_4 is needed to provide a nulling resistance to reduce the effects of that right hand plane zero in the transfer function, and, in fact, can be used to improve the frequency response of the amplifier.

The three stages of the amplifier and its compensation circuitry provide a stable, moderate gain, low power and fast settling time monolithic CMOS operational amplifier. The following sections discuss the design of this amplifier, the constraints for the design, the simulation and performance results, and a discussion of the overall amplifier.

III. Design constraints

A. DC Gain:

The open loop gain of an op amp determines the precision of the feedback system employing the opamp. As mentioned before, the required gain may vary by four orders of magnitude according to the application. Trading with such parameters as speed and output voltage swings, the minimum required gain must therefore be known.

$$\frac{vo}{vi}=\frac{g_{m2}\times g_{m6}}{(g_{ds2}+g_{ds4})\times(g_{ds6}+g_{ds7})}=\frac{\sqrt{k_p\times 2k_n}}{(\lambda 2+\lambda 4)\times(\lambda 6+\lambda 7)}\times\frac{\sqrt{(\frac{W}{L})_2\times(\frac{W}{L})6}}{\sqrt{I_{D5}\times I_{D7}}}$$

B. Common-Mode Input Range:

For large differential output swings the differential input swings are usually much smaller (by a factor equal to the open loop gain), the input common mode level may need to vary over a wide range in some applications.

$$CMR^{-}=V_{GS3}+\left|V_{DSAT1}\right|-\left|V_{GS1}\right|=\leq 01.43V$$

$$CMR^{+}=\left|V_{DSAT5}\right|+\left|V_{GS2}\right|\leq 0.68,$$

C. Output Swing**:**

Most system employing op amps require large voltage swings to accommodate a wide range of signal amplitudes. The need for large output swings has made fully differential op amps quite popular, such opamps generate "complementary outputs, roughly doubling the available swings.

$$Vout^{+}=\left|V_{DSAT7}\right|=\sqrt{\frac{2I_{D7}}{k_p(\frac{W}{L})_7}}\leq 0.149\ ,$$

$$Vout^{-}=\left|V_{DSAT6}\right|=\sqrt{\frac{2I_{D7}}{k_n(\frac{W}{L})6}}\leq 0.549$$

D. Power Dissipation:

Power is the important constraint for designing any opamp. It should be as low as possible. It depends on the supply voltage and the total currents.

$$(I_{D8}+I_{D5}+I_{D7})*(V_{DD}-V_{SS})\leq 1.4mW,$$

$$(I_{D8}+I_{D5}+I_{D7})\leq 400uA$$

E. Unity Gain Frequency:

$$fu=\frac{g_{m2}}{2\pi C_C}=\frac{\sqrt{I_{D5}k_p(\frac{W}{L})_2}}{2\pi C_C},$$

F. Settling Time:

For the operational amplifier we need fast settling time to get stability in output. It somehow connected to the slewing effect.

$$SR=\frac{C_C}{I_{D5}}+\frac{C_L}{I_{D7}}\ =\ 145\ \text{V/µs}$$

$$p_1=-\frac{1}{g_{m6}R_{o1}R_{o2}C_C}=-\frac{\omega_u}{a_{vo}}=-\frac{(\lambda_2+\lambda_4)(\lambda_6+\lambda_7)I_{D5}\sqrt{I_{D7}}}{2C_C\sqrt{2k_n(\frac{W}{L})_6}}$$

$$p2\cong-\frac{g_{m6}}{C_C}=-\frac{\sqrt{2I_{D7}k_n(\frac{W}{L})_6}}{C_C}$$

$$\omega_n=\sqrt{p_1p_2a_{vo}}$$

$$\zeta=\frac{p_1+p_2}{2\sqrt{p_1p_2a_{vo}}}$$

$$V_{OVERSHOOT}=Vo\exp\left[\frac{\pi\zeta}{\sqrt{1-\zeta^2}}\right]$$

$$T_S=\frac{\pi}{\omega_n\sqrt{1-\zeta^2}}-\frac{1}{\zeta\omega_n}\ln\left[\frac{0.001\times Vo}{V_{OVERSHOOT}}\right]$$

IV. Simulation result

The proposed operational amplifier design with the TSMC 0.18 micron CMOS Process. The tables1 shows the Aspect ratio of all the mosfet used in the circuit design. Tables 2 show the result taken in different configuration.

Table 1: Different Transistors Aspect Ratio and Current

TRANSISTOR TYPE & NAME	W/L RATIO	W (µm)	L(µm)	I_D (µA)
MPMOS_1(M5)	20.89	3.76 µ	.18 µ	41.017
MPMOS_2 (M1)	23.89	4.30 µ	.18 µ	20.508
MPMOS_3 (M2)	23.89	4.30 µ	.18 µ	20.508
MPMOS_4 (M8)	0.337	.18 µ	.534 µ	0.589
MPMOS_5 (M9)	225.67	40.62µ	.18 µ	368.43
MNMOS_1(M3)	0.0731	.27 µ	3.69 µ	20.508
MNMOS_2(M4)	0.0731	.27 µ	3.69 µ	20.508
MNMOS_3 (M6)	2.133	.576 µ	.27 µ	368.43
MNMOS_4 (M9)	50	9 µ	.18 µ	0
MNMOS_5(M12)	0.0189	.27 µ	14.295 µ	0.589
MNMOS_6(M13)	0.0189	.27 µ	14.295 µ	0.589
MNMOS_7(M14)	0.042	.27 µ	6.39 µ	0.589
MNMOS_8(M10)	12.83	2.31 µ	.18 µ	0.589
MNMOS_9(M11)	12.83	2.31 µ	.18 µ	0.589

Table 2: Simulation Design Result

PARAMETER NAME	VALUES
V_{DD} & V_{SS}	2 V & -2V
DC GAIN	33.49 dB
UNITY GAIN FREQUENCY	158.49 MHz
LOAD CAPACITANCE	2 pF
SETTLING TIME	5.90 ns
POWER DISSIPATION	1.4 mW
SLEW RATE	145 V/µs
COMMON MODE RANGE	1.43 V +ve & .68 -ve
Output Swing	1.85V +ve & 1.5V –ve
PSRR	11 dB for +ve PSRR 2 dB for -ve PSRR
GAIN BW PRODUCT	5.33 * 10^9

A. DC GAIN

Throughout the design, the dc gain was not a factor and was reduced in trading off other performance characteristics of the design. The gain was measure using the configuration shown in figure 6.1, below, because it allows the direct measurement of v_o/v_{in} at dc.

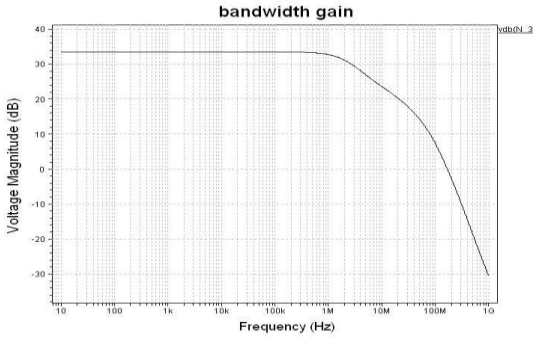

Figure 2. DC Gain and –3dB frequency of the amplifier.

The graph in Figure 3, above, shows the result of the simulation. The DC gain is just slightly over 33 dB, 33.494 dB to be exact, and the gain starts to roll off around the –3dB frequency of 2.39 MHz. and the unity gain frequency is 158.49MHz.

B. POWER DISSIPATION

The circuit was initially designed for a maximum open loop quiescent power or 1.4 mW.

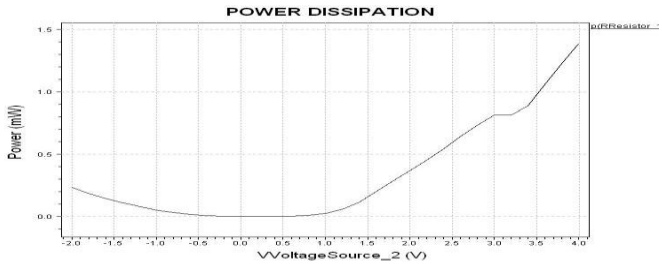

Figure 3. Power dissipation of the amplifier

C. SETTLING TIME

The settling time was the most demanding constraint in the design of the amplifier. The initial design contained large (W/L) ratios and a small current in the differential pair in order to meet the CMR specification.

The results of this simulation are shown in figures 4. The settling time to 0.1% for the amplifier was 5.9 ns for a 0 to +1 V output step and 5.9 ns for a 0 to –1 V output step.

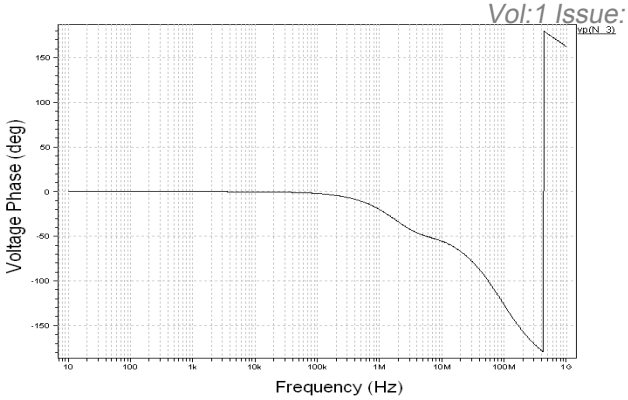

Figure 4 The phase response of the open-loop amplifier, displaying a phase margin of 143.3°at unit gain.

V. Conclusion

The design process that was followed resulted in a complete CMOS operational amplifier that at least met and, in a few cases, exceeded the design objectives by a large margin. The notable performance areas were the settling time of 5.9 ns, High slew rate 145 V per micro second, very large gain bandwidth product and the power consumption of 1.4 mW with high current capability as compared to input. The design also have the some drawback due to the making some parameters good. When we making op amp fast it decreases the the power supply rejection ratio and the gain.

A great deal was learned in the design process, including how to approach a design project, the tradeoffs involved in a CMOS op-amp design, patience, and how to stay up late.

References

1. B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2002.
2. Danica Stefanovic and Mahar Kayal, " Structured Analog CMOS Design", Springer 2008.
3. D. John and K. Martin, "Analog Integrated Circuit design" John Wiley , 1997
4. Philip E. Allen and Douglas R. Holberg, "CMOS Analog circuit Design" Oxford University Press, 2002, second edition.
5. M.Figueiredo, E.Santin, J.Goes and R.Santos-Tavares, "Two stage Fully Differential Inverter based Self biased CMOS Amplifier with high efficiency" in IEEE- 2010 journal ISBN no. 978-1-4244-5309-2/10
6. Hyunchol Shin and Youngcho Kim," A CMOS Active-*RC* Low-Pass Filter With Simultaneously Tunable High- and Low-Cutoff Frequencies for IEEE 802.22 Applications" in IEEE transactions on Circuits And Systems—II: Express Briefs, Vol. 57, No. 2, February 2010
7. Ehsan kargaran, Hojat Khosrowjerdi and Karim Ghaffarzadegan, "A 1.5 V High Swing ultra-low power two stage CMOS Opamp in .18 micron techonology" in 2nd International conference on mechanical and Electronics Engineering (ICMEE2010) 978-1-244-7481-2 @IEEE
8. F.A. Amoroso, A. Pugliese, and G. Cappuccino, "Design considerations for Fast-settling two stage miller compensated Operational Amplifiers" in IEEE 2009 conference with 978-1-4244-5091-6/09