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Design of low power and high speed components of SAR ADC

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Abstract: **Main building blocks of a SAR-ADC are: sample & hold circuit, comparator, timing and logic control which is mainly SAR logic, DAC (Digital to Analog Converter) in the feedback loop of ADC. For low-power applications designer needs to come up with a compromise among speed and resolution. In this paper the components for SAR ADC are designed in 0.18µm CMOS technology in such a way that the total power is minimized.**

CMOS has been the dominant technology for VLSI implementation. As VLSI circuits continue to grow and Technologies evolve, the level of integration is increased and higher clock speeds are achieved. Higher clock speeds, increased level of integration and technology scaling are causing unabated increase in power consumption as a result; low power consumption is becoming a critical issue for modern VLSI circuits.

For battery operated systems, low power consumption requirements are well understood and followed. Whereas for high performance ICs, reducing the delay has been the main objective, and power containment was secondary. However recent research shows that power containment for high power applications is becoming critical for reliability, transistor performance, and cooling considerations. In this paper we are presenting low power and high speed components of ADC.

Key words -Analog-to-digital converter (ADC), CMOS analog integrated circuits, DAC, comparator, low power, low supply voltage, successive approximation.

I. Introduction

Today's trend in mixed-signal ASICs leads to integration of Analog-Digital-Converters (ADCs) with complex digital circuitry on a single chip. ADCs are a key element in mixed-signal ICs. The power consumption is critically important in modern VLSI circuits especially for low-power applications. The power optimization techniques are applied at different levels of digital design. However, optimization at the logic level is one of the most important tasks to minimize the power. Among logic components, latches and flip-flops are critical to the performance of digital systems.

In a recent survey article on data conversion, it was pointed out that the most popular type of analog-to-digital (A/D) converter in use today is the one employing the successive-approximation (SA) logic. The main reason for its popularity lies in its inherently fast conversion time which is a constant n clock periods for an n-bit converter. When compared to other A/D schemes such as the dual-slope integrating method and the servo-type method, the successive-approximation scheme offers much higher conversion rates. Considering these factors, SAR becomes an ideal component for some portable or battery-powered instruments.

Basically, the successive-approximation A/D converter consists of three main components an analog comparator, a DAC, and a successive-approximation register (SAR) all of which are connected in a feedback arrangement shown in Fig.

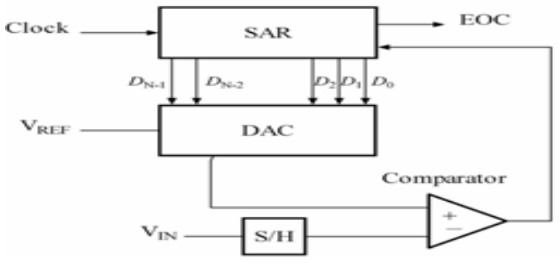

Fig.1. Block Diagram of SAR ADC

In the proposed SAR design, register is made up of double edge triggered D Flip-flops connected in series fashion. A single row of DETDFF is used in each bit cell which functions both as sequencer and code register. This

type of design is often referred to as the sequencer/code register design.

In a conventional single edge-triggered (SET) flip-flop, data moves from input to output in synchrony with one edge of the clock. The use of double edge-triggered flip-flops has been already proposed for low-power circuit design. In a DET flip-flop, both rising and falling edges of the clock signal are used to transfer data from input to output. In this way, for a given throughput, the clock frequency can be halved with respect to a system using SET flip- flops, with a reduction of power consumption. Unfortunately, DET flip-flops require a more complex implementation with respect to SET flip flops. This results not only in larger silicon area but also requires higher number of internal nodes and transistors

Also, since this design is fully synchronous with the clock and data input signals, a reduction in propagation delay through the register is achieved when compared to asynchronous SAR designs.

II. Shift Register Using DETDFF

Conventional single-edge-triggered flip-flops (SET-FF's) changes states at the time when the clock signal goes from 0 to 1 or at the time when the clock goes from 1 to 0. The former are called positive-edge-triggered flip-flops (PET-FF's) or rising edge-triggered flip-flops (RET-FF) and the latter are called negative-edge-triggered flip-flops (NET-FF's) or trailing-edge triggered flip-flops (TET-FF's).

The advantage of edge triggering is that the setup time for data input is independent of the clock pulse width. This makes system design simpler. It is also less sensitive to noises. However, these flip-flops respond only once per clock pulse cycle. Energy and time are wasted.

These double-edge-triggered flip-flops (DET-FFs) have two major advantages. First, power dissipation is reduced. With the conventional SET-FF's, one of the two clock transitions accomplishes nothing. However, this transition may cause changes in the output of some logic elements internal to the FF's. In addition, extra energy is wasted to charge or discharge the capacitive load of the global clock line in a system using SET-FF's. This is particularly true in CMOS where static power dissipation is small and the dynamic power dissipation is the main contributor of energy dissipation. Second, the speed of the system is accelerated. With both edges able to cause state transition, some redundant logic can be eliminated. Moreover, the clock period will be shortened because there is no need to wait for the clock signal to toggle up and down. The main disadvantage of DET-FF's has been the substantial increase in the number of components required to build such FF's. In most cases, more than double the logic counts is expected. This paper proposes a novel design in CMOS which will implement static DET-FF's with relatively little increase in components.

If we investigate the basic process that the clock signal controls a flip-flop, we will find that the efficiency of the clock is only 50%. Low and high levels of the clock signal put a latch in either a storage state or an input state. In the storage state, the clock level switches off the input path, and the input data is thus rejected, while in the input state, the clock level allows the input signal to reach the output terminal of the latch. However, if input date can be received and sampled at both levels of the clock, the flip-flop will receive and process two data values in one clock period. In other words, the clock frequency can be reduced by half while keeping the data rate the same. This means that under the requirement of preserving the original circuit function and data rate, the dynamic power dissipation due to clock transitions can be reduced by half. It is expected that the half frequency reduced clock system is useful in low power systems (including wireless, battery operated systems).

How to sample and store the input data at both clock levels? We consider two related problems. The first problem is to restructure the flip-flop so as to sample and store the input data at both of its edges. This is precisely a double edge- triggered (DET) flip-flop, which samples the input data by both the clock's rising edge and falling edge. The second problem is to use the traditional single-edge-triggered (SET) flip-flop (for example, sensitive to clock's falling edge) to compose a new storage system, which can sample the input data on the clock's rising edge as well as its falling edge. **As** to the first challenge, this paper investigates the principles of the DET flip-flop design and presents a logic structure based on multiplexors (MUX), which is used to realize this type of flip-flop. Furthermore, a new circuit design of a CMOS DET flip-flop is described. By using computer simulation, the proposed design is compared with the traditional SET flip-flop. Results show that the DET flip-flop exhibits a **2x** power saving factor. Besides, comparison of this DET flip-flop with ones reported by other researches show that our design has a simpler structure, lower delay and higher maximum data rate. As to the second challenge, this paper proposes a new double-edge-triggered storage device, which is composed of traditional SET flip-flop, but receives data at both edges of the clock. This design can also be used for reducing power dissipation while preserving the data throughput or doubles the data throughput while preserving the power dissipation.

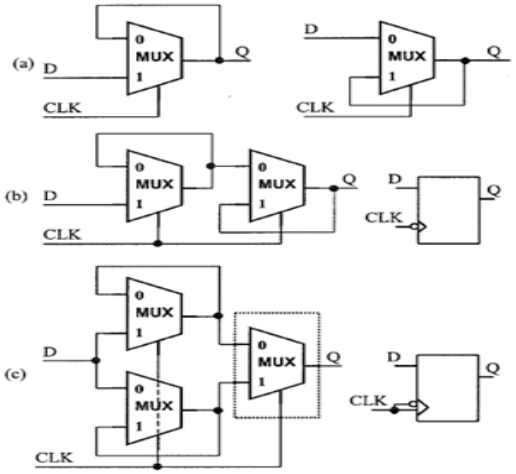

Fig. 2 – (a) Positive and negative level sensitive latch
(b) SET Flip-flop (c) DET Flip-flop

A. Logic Structure of DETDFF Flip-Flop

The following figure 3(a) indicates the CMOS implementation of DETDFF using MUX. The proposed model is designed by using 0.18um TSMC model technology. We have used the supply voltage =of 1 V. This is a simpler design for DETDFF. Power consumption is approximately equals 900pw-1uw. , Due to the diverse design-styles and the number of transistors used, the power consumption and delay varies from one flip flop to another. The power consumption what we mentioned here is the average internal power consumption, which is the intrinsic power consumed by the Flip Flop on switching their internal nodes. The delay we had taken into account is the time measured between the clock edge and output edge. The simulation results are given in Table. If supply voltage is increases at 1.2v speed and power will increases, satisfactory and sufficient for 1 GHz no need to increases power supply voltage.

Fig 3 (a)

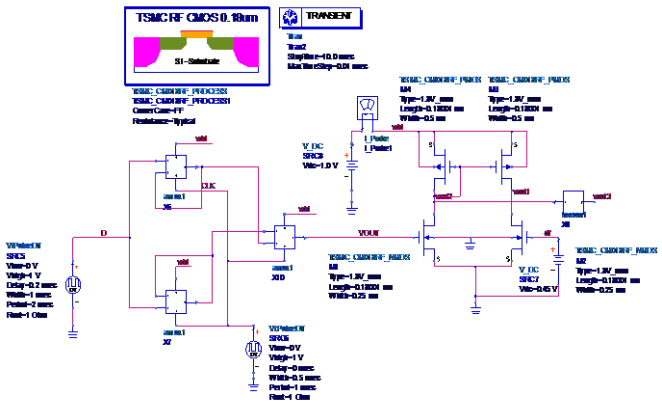

Fig.3 (b)

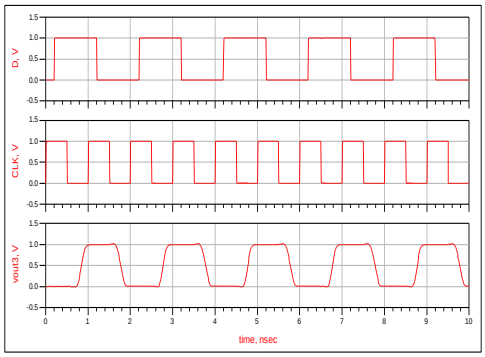

Fig.3. (a) CMOS Structure of DETDFF

(b) Transient Response of DETDFF

B. Design of Shift Register Using DETDFF Based On Traditional SET Flip-Flop

Dynamic DET flip-flops have also been investigated based on the fact that the DET flip-flops can be connected in series to form a shift register. Figure 2(a) shows two DET flip-flops connected in series, which form a 4-bit shift register. This example hints that the traditional SET flip-flop can also be used to form a 4-bit register which is double-edge-triggered. Figure 6(b) shows the waveforms of 4 bit shift register.

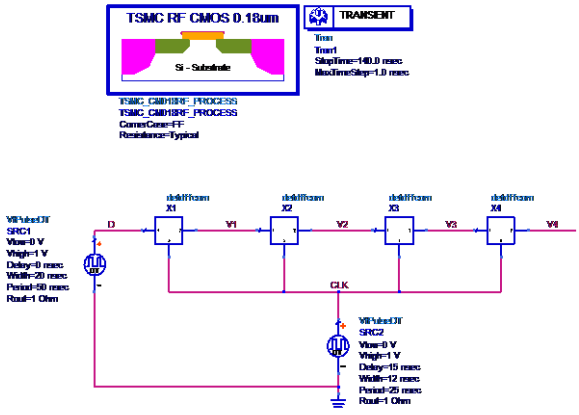

Fig.4. (a) 4 bit shift register using DETDFF

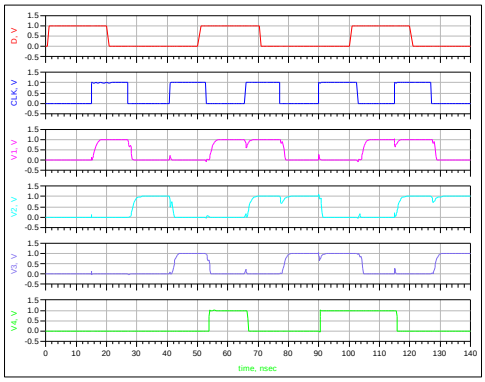

Fig.4. (b) Transient analysis of 4 bit shift register

III. Differential Circuits

In order to precisely slice the input data, a reference voltage may be transmitted, on a different signal path, along with the data. Alternatively, the data may be transmitted differentially (an input and its compliment). In either case a differential amplifier is needed as shown in below fig.5. Differential amplifier input buffer amplifies the difference between the two inputs. In the simple case one input to the input buffer is DC voltage, say 0.5 V (Vinm in fig). When the other input (Vinp) goes above 0.5 V, the output of the buffer changes states (goes from low to high or vice versa).

Vinp > Vinm → out = '1'

Vinp < Vinm → out = '0'

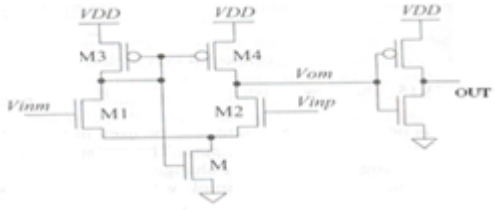

Fig.5.An (n-flavor) input buffer for high-speed digital design

This circuit is self biased because no external references are used to set the current in the circuit (the gate of M6 is tied up with M3). When Vinp is greater than Vinm, the current in M2 is larger than current in M1 (VGS2 > VGS1). The current in M1 flows through M3 and is mirrored by M4 (and so M4's current is less than M2's current). This causes the diff-amp's output, Vom, to go towards ground (until the current in M2 equals the current in M4) and the output of the inverter, Out, to go high.

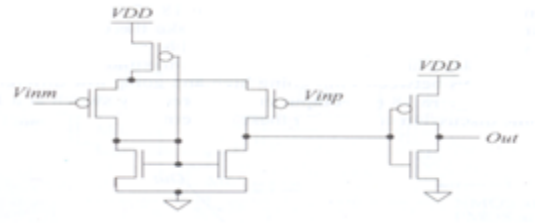

Fig.6.A PMOS input buffer for high-speed digital design

Transient Response

A very small increase in Vinp above Vinm is required to make the output of the buffer switch states. Looking at fig, we can see the input falls below VTHN (= 250mV here), then the circuit won't work very quickly (the MOSFETs moves into the sub threshold region). So we would expect the propagation delays to increase.

Ideally the delay of the buffer is independent of power supply voltage, temperature, or input signal amplitudes (or pulse shape). To get better performance for lower input level signals, we might use the PMOS version of the buffer as shown in Fig 6.

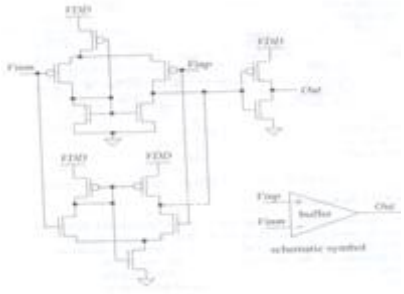

Fig.7. Rail to Rail input buffer

The delays are considerably better, however, there is an offset that appears rather large (because the output changes at the same time as Vinp going past Vinm, indicating that an offset is present).To avoid this offset, we might use the NMOS buffer in fig. 5 with the PMOS buffer in fig.6 to form a buffer that operates well with input signals approaching ground or VDD. The result seen in fig.7. By using the buffers in parallel, the complementary nature results in buffer that is robust and works over a wide range of operating voltage.Fig. 8 (a,b,c) shows the CMOS circuit ,test circuit and transient analysis of comparator .

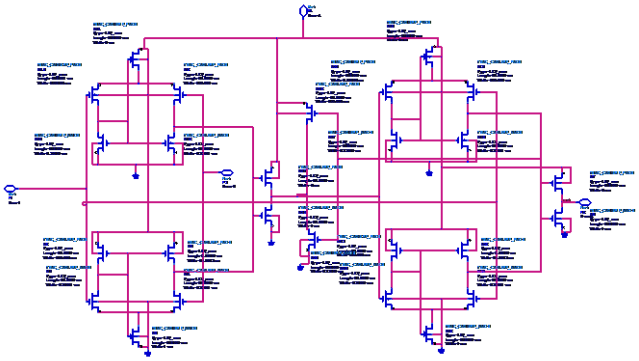

Fig.8. CMOS Structure of Comparator

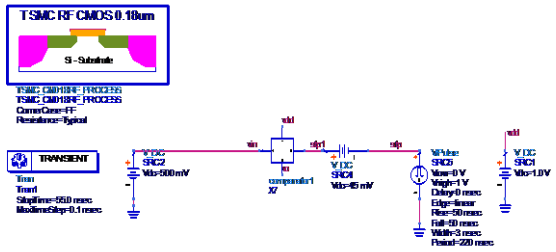

Fig.8.(b) Test circuit of Comparator

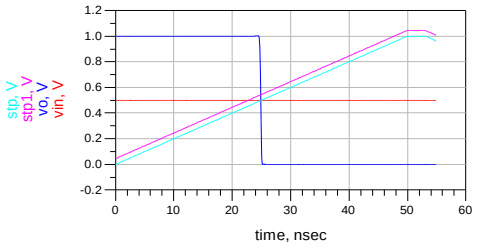

Fig.8.(c) Transient Analysis of Comparator

IV. Digital to Analog Converter (DAC)

A R-2R ladder D/A converter is shown in a fig.9(a) below. It uses resistors of only two values R and 2R. The inputs to the resistor network are connected through digitally controlled switches. A switch is in position 1 or 0 corresponding to the digital input for that bit position being 1 or 0, respectively.

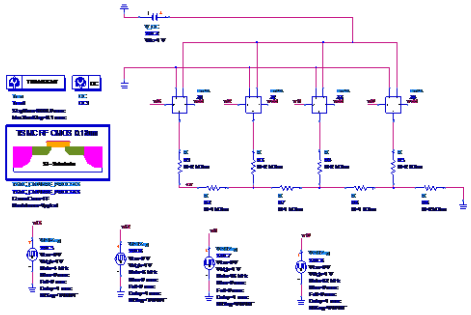

Fig.9. (a) Design of DAC Using R-2R Ladder Network

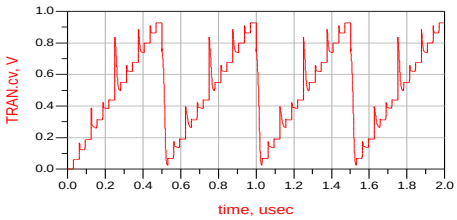

Fig.9.(b) Transient analysis of DAC

V. Conclusion

In this paper, low power and high speed components of SAR ADC are proposed and designed in .18µm CMOS technology. We presented high speed and low power design of DETDFF and by using the same we designed shift register whose speed of operation is doubled than that of shift register made up of SETDFF with low power consumption. Also we presented CMOS comparator circuit which is a combination of n-flavored and p-flavored buffers and remove the disadvantages of both. An area efficient DAC architecture strictly based on the R-2R ladder topology is designed. Currently we are working on developing SAR logic.

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