A CMOS Mixer For Multiband Receiver Front-End

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Abstract

In this letter, a fully integrated down-conversion mixer is presented for multiband applications. The receiver front-end consists of a multiband low-noise amplifier (LNA) and a down-conversion mixer. The down-conversion mixer is major responsible for the limited dynamic range in the RF front-end. Using a standard 0.18 µm CMOS technology, a 0.7–2.5 GHz mixer for multiband receiver frontend is implemented suitable for many applications such as GSM/DCS/CDMA2000 cellular standards[1][2]. It exhibit below 10dB DSB NF. The main advantages of the proposed mixer are using a identical mixer for each frequency band which reduces the chip area.

I. INTRODUCTION

The wireless market is growing rapidly. Being pushed by market demands, various wireless communication systems are emerging. In order to increase flexibility on the market and functionality of RF transceivers, multi-band and/or multistandard transceiver architecture solutions are pursued.

With the proliferation of wireless standards and frequency bands of operation, there is an urgent need to design a single transceiver that is compatible with multiple standards. This paper presents the design of a multiband CMOS quadrature down-conversion mixer.

The main challenge lies in maintaining moderate gain, noise figure, and linearity at minimum current consumption across a wide frequency spectrum with the abating supply voltage. The circuit operates at a wide range of frequencies from 700MHz to 2.5GHz suitable for many applications such as GSM/DCS/CDMA2000 cellular standards. It takes advantage of the different requirements set by the different standards. The minimum required performance of a certain wireless system is determined by the standard. However, including multiple standards in the same device puts a higher demand on the circuit performance.

The paper is organized as follows. In Section II, the receiver frontend architecture. In section III, the Circuit Design, the design of the Mixer is described. Section IV gives the simulated results. Finally, a conclusion is drawn in Section V.

II. RECEIVER FRONTEND ARCHITECTURE OVERVIEW

A block diagram of the receiver front-end is shown in Fig. 1, which consists of a wideband low-noise amplifier (LNA) and two double-balanced mixers for down-conversion of the RF signal to IF in quadrature outputs. In this version of the design, the LO is provided externally by a separate frequency synthesizer chip with quadrature outputs. It will eventually be implemented with the receiver front-end together as a single chip to increase the integration level and to reduce the power consumption consumed by the LO drivers[2].

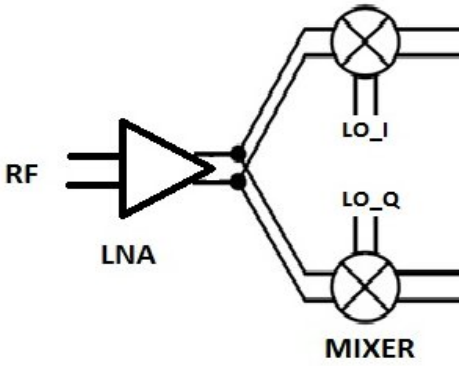

Figure 1. Block diagram of the receiver frontend

Figure above shows the block diagram of the circuit; the key building blocks include a low-noise amplifier, a quadrature demodulator. It consists of two separate mixers and a quadrature local oscillator (LO). To enable a double-balanced topology, a modified Gilbert mixer with RF input stage acting as an active balun to perform single-ended to differential conversion is designed.

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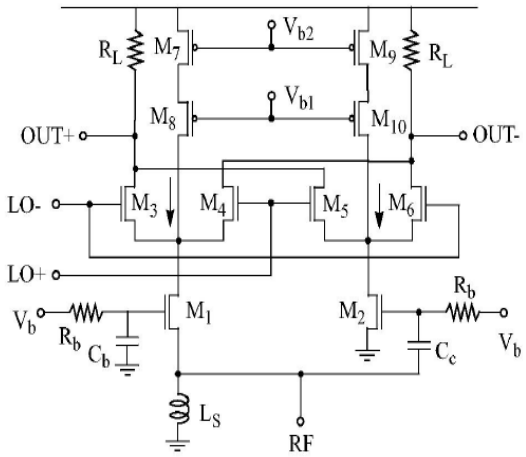
III. DOWNCONVERSION MIXER DESIGN

The schematic of the down-conversion mixers is drawn in Fig 2.The mixer is based on a double-balanced Gilbert mixer topology. MOS transistors M1 and M2 are used to perform voltage-to-current conversion of the RF signal, while M3-M6 are used as LO-switches.

The RF input stage, with combined common-gate stage M1 and common-source stage M2, also

function as an active balun in converting the single-ended RF voltage input to differential current output.



Additional dc currents are injected at the common source nodes of the MOS switching pairs through cascode current sources composed by PMOS transistors M7-M10. Without them the linearity and noise performance of this type of
mixers always trade off each other[3].

IV. EXPERIMENTAL RESULTS

The proposed downconversion mixer is implemented in a 0.18 um CMOS technology. Operated at a 1.5 V supply voltage, the fabricated frontend consumes a dc current of 15 mA. Table I summarizes the performance of the fabricated frontend at various operating frequency bands. External baluns are used to convert the differential output to a single-ended form. At the time when this paper is prepared, measurements are still on-going. Most of the results presented below are obtained from post-layout simulations. Over the entire 0.7-2.5GHz frequency band the mixer achieves a power gain of greater than 15 dB and a noise figure of less than 10 dB, respectively [4].

V.CONCLUSION

A novel multiband mixer suitable for multiband wireless applications is demonstrated in this work. The mixer circuit is implemented in a 0.18 m CMOS process. The design of a 0.7-2.5 GHz CMOS mixer for multiband wireless applications has been presented. This architecture consists of a quadrature down-conversion mixers with embedded active balun, which provides the single-ended-to-differential conversion and enables the use of single-ended LNA and double-balanced mixers.

Specification	Value
Operating Frequency	0.7 GHz - 2.56 GHz
Process Technology	0.18 μm CMOS
Supply Voltage	1.5V
Voltage conversion gain	>10 dB
DSB NF	<10 dB

REFERENCES

1. A 3–5 GHz Frequency-Tunable Receiver Frontend for Multiband Applications by Chong-Ru Wu, Hsieh-Hung Hsieh
2. A 1.5V 0.7-2.5GHz CMOS Quadrature Demodulator for Multi-Band Direct-Conversion Receivers Nuntachai Poobuapheun, Wei-Hung Chen, Zdravko Boos, and Ali M. Niknejad
3. Noise in RF-CMOS Mixers: A Simple Physical Model Hooman Darabi and Asad A. Abidi
4. A CMOS Receiver Front-End for 3.1-10.6 GHz Ultra-Wideband Radio by Bo Shi and Michael Yan Wah Chia
5. Multi-Band Combined LNA and Mixer by Miguel A. Martins, Jorge R. Fernandes, and Manuel M. Silva