International journal of Advances in Electronics Engineering
Vol:1 Issue:1 ISSN 2278 - 215X

Static Write Margin and Power for 6T & 7T SRAM Cell: A Comparison

Manoj Kumar, Rohit Kumar
Department of Electronics & Communication Engineering
Guru Jambheshwar University of Science & Technology, Hisar, India (125001)
manojtaleja@yahoo.com, rohit_pahwa001@yahoo.com

***Abstract*— SRAM cell read stability and write-ability are major concerns in CMOS technologies, due to the progressive increase in V_{DD} and transistor scaling. In this paper, we studied and comparedthe performance of 7TN (with NMOS access transistor), 7TP (with PMOS access transistor) andconventional 6T structure.SRAM cells have been simulated in SPICE with 0.35 µm technology. The techniques that provide the highest data stability, the lowest power consumption, and the smalllayout area are identified. Both 7TN and 7TP cell provides higher write stability as compare to 6T SRAM cell (around 24% increase in SWM). Voltage swing of 7T is large than 6T. 7TN SRAM shows 51% power reduction and 7TP cell shows 62% (write and read '1') power saving as compare to conventional 6T.**

Keywords– CMOS, static random access memory (SRAM), static write margin (SWM), bit line (BL), write-read (WR).

I. INTRODUCTION

Modern SRAM designsstrive to increase bit count while maintaining low power consumption and high performance. Scaling the supply voltage and minimum transistor dimension that are used in SRAM cells challenges the process and design engineers to achieve reliable data storage in SRAM arrays. This task is particularly difficult in large SRAM array that contains millions of bits. Due to device scaling there are several design challenges for VLSI (very large scale integration) SRAM design. Now designers are working with very low threshold voltage and ultra thin gate oxide due to which leakage power consumption is increasing. Besides this data stability during read and write operation is also getting affected [1].

This paper presentsa comparative analysis of low power CMOS SRAM cell. 7TP SRAM cell showswith 62% reduced power consumption and large write stability as compared to 6T and 7TN(with NMOS access transistor).The seven transistor (7T) SRAM cells have advantage of reducing the active and standby mode power consumption while enhancing the datastability &circuit speed.With 7T SRAM cell, thedata storage nodes are isolated from the bit lines during a read operation. The data stability is thereby significantly enhanced byup to 87% as compared to a standard 6T SRAM cell [5].

Rest of paper organized as follows: SRAM cells are described in Section II. Results and comparison of SRAM cells have been presented in Section III. The conclusions have been drawn in Section IV.

II. SRAM CELLS

A. Conventional 6T SRAM:

The conventional 6T SRAM cell is shown in Figure1. It composed of two cross-coupled CMOS inverters (N1, P1 and N2, P2) with two NMOS pass transistor (N3 and N4) connected to complementary bit-lines. The two access transistors are also connected to word-line (WL) to perform theaccess write and read operation through bit line (BL) and bit line bar (BLB). Bit-lines act as input/output nodes carrying the data from SRAM to a sense amplifier during read operation, or from write circuitry to the memory cells during write operation [2].

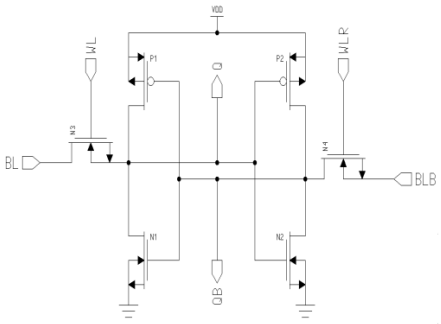
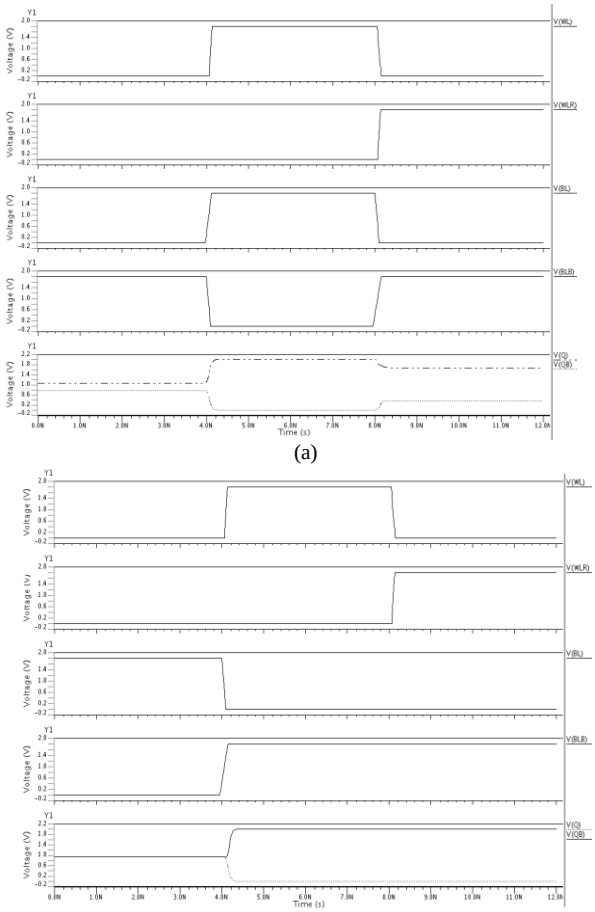


Figure 1. 6T-SRAM

Careful transistors sizing is also required to ensure a stable read and write operations [2]. Writing is done by lowering one of the bit lines to ground while asserting the word line. To write a '0' BL is lowered, while writing a '1' requires BLR to be lowered. To prevent accidental writing transistor N1 has to be stronger than transistor N3. To read datum 6T use a differential read operation. This means that both the stored value and its inverse are used in evaluation to determine the stored

value. Prior to read operation bit lines are precharged to high. The gates of transistorsN3 and N4 are held low, these access transistors are off and the cross-coupled latch is isolated from the bit lines. If a '0' is stored on the left storage node, the gates of the latch to the right are low. That means that transistor N2 is initially turned off and P1will also be off initially since its gate is held high. The next phase of the read operation is to pull the word line high and at the same time release the bit lines. This turns on the access transistors and connects the storage nodes to the bit lines. It is evident that the right storage node has the same potential as BLB and therefore no charge transfer will be take place on this side.The left storage node, onthe other hand, is charged to '0' (low) while BLB is precharged to $V_{DD.}$ Thus the data written during write operation is read successfully. Simulation result to write-read '1' and '0' is shown in figure 2(a), (b) respectively.



(a)

(b)

Figure 2.(a) 6T WR '1' (b) 6T WR '0'

B. 7TN SRAM:

The circuit schematic of the 7TN SRAM cell is shown in Figure 3 .The cross-coupled transistor (N1, P1, N2 and P2) foam a latch and keeps the datum, here two separate control signals W and R are used to control write and read operation respectively. 7TN SRAM overcome the stability problem of 6T SRAM cell to a great extant [5].

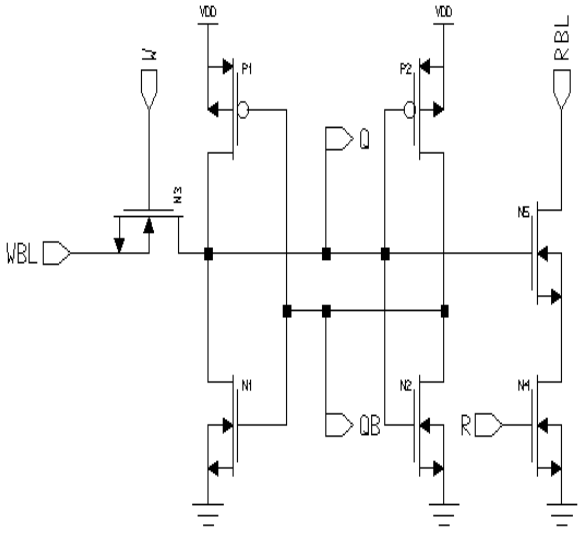
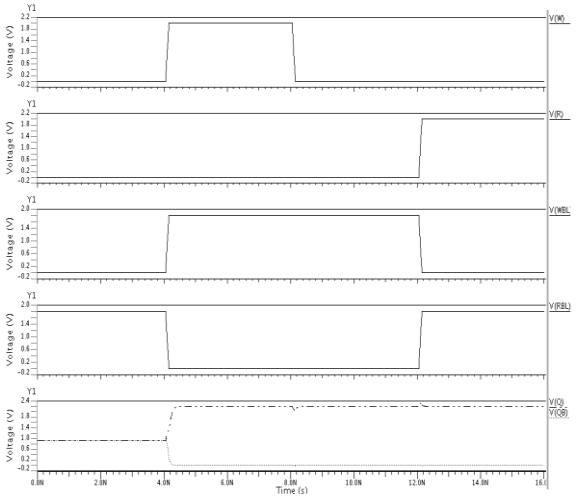


Figure 3. 7TN SRAM

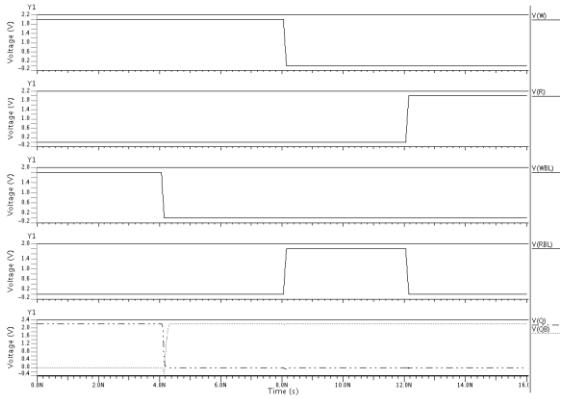
To start a write operation, the write signal W is kept at VDD and read signal R is kept as ground. On the other hand WRL is maintained at V_{DD} or ground to force a "1" or "0" at node Q. For write operation access transistor N3 must be stronger than pull down transistor N1 [3]. Write-read operation at node Q for datum "1" and "0" is shown in figure 4(a) and 4(b) respectively.



(a)

During read operation R is maintained at "1" while W at "0". WBL and RBL are pre-charged to V_{DD} [6]. The write stability of 7TN cell is improved by 71% as compares to

conventional6T cell. Read stability is also enhanced due to isolation of bit-lines during read operation [4].



(b)

Figure 3.(a) 7TN WR '1' (b) 7T WR '0'

C. 7TP-SRAM:

The 7TP SRAM cell introduced in [4] is shown in figure (5). 7TP is based on 4T cell, because 4T SRAM cell's power consumption is lower than 6T cell. 7TP SRAM cell reduces the activity factor of discharging the bit line pair to perform a write operation [4]**.**The circuit employs 2 PMOS transistor for write operation and one NMOS transistor for read operation.

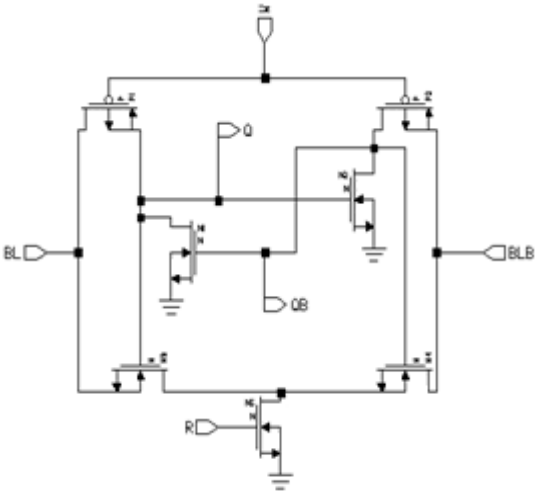
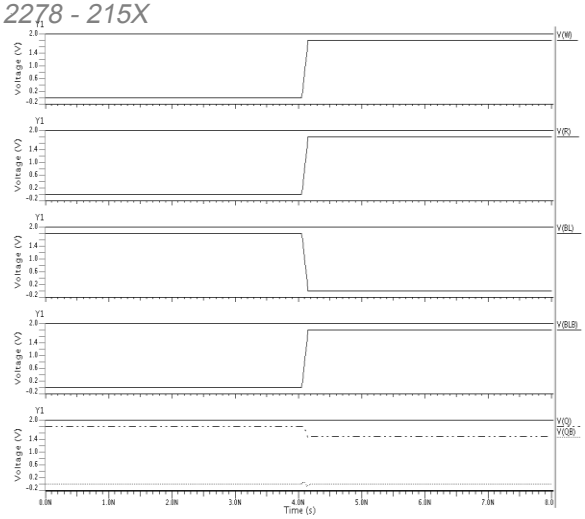
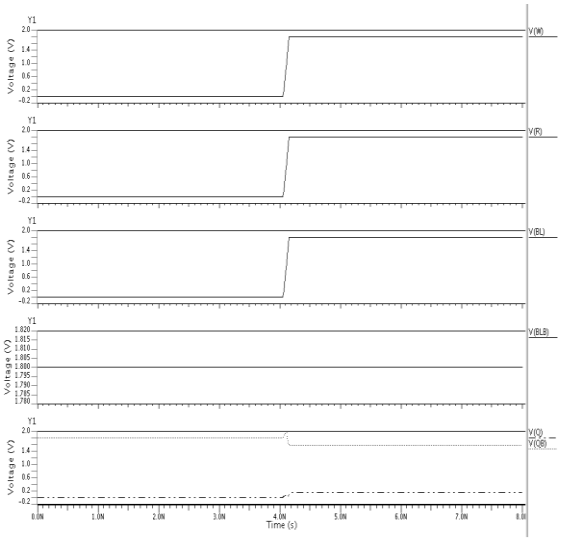


Figure5. 7TP-SRAM

As there is no direct path from bit-lines to the storage nodes, which offer high stabilityread operation. Also writing path of this cell are independent and never interfere therefore data destruction never occurs [4]. Figure 6(a) and 6(b) shows simulation result for write-read operation.



(a)



(b)

Figure 3.(a) 7TP WR '1' (b) 7TP WR '0'

III. RESULTS AND COMPARISION

A. Write Margin:

SRAM write ability is the major concern in VLSI CMOS technology. Write ability of SRAM is depends upon the static write margin (SWM) and dynamic write margin. In this section we compare SWMof different cells by different approaches. The most common static approach uses WL to measure SWM. In this method SWM is defined as the difference between V_{DD} and WL [7]. Figure (7) shows SWM for 7TP, during write '1' operation when Q and QB flip.

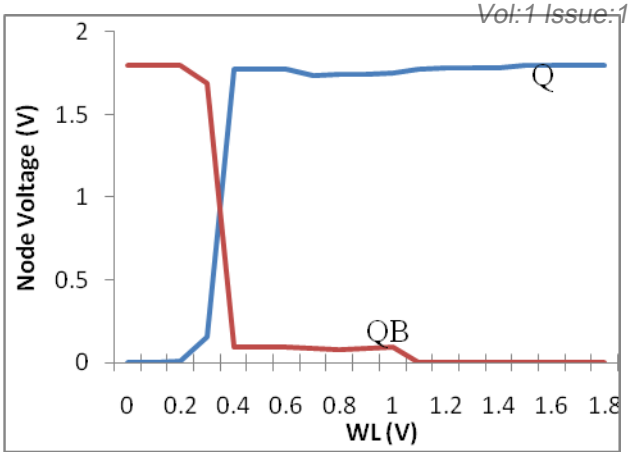


Figure 7. SWM of 7TP SRAM

BLB voltage can also be used to measure write margin [7]. SWM using BLR is defined as the value of BLB at the point when Q and QB flip and term as VBL. For faithful write operation value of VLB must be high. Table 1 shows the value of VWL and VBL for 6T, 7T and 7TP.

TABLE 1.STATIC WRITE MARGIN FOR SRAM CELL

Cell	Static Write Margin	
	VWL (V)	*VBLB/VRL(V)*
6T	0.272	0.342
7TN	0.390	0.366
7TP	0.380	0.380

Figure 8. shows the effect of control voltage (WL, BL/WBL, and BLR/RBL) over SWM. Values of SWM keep on decreasing as we reduced the control voltage.

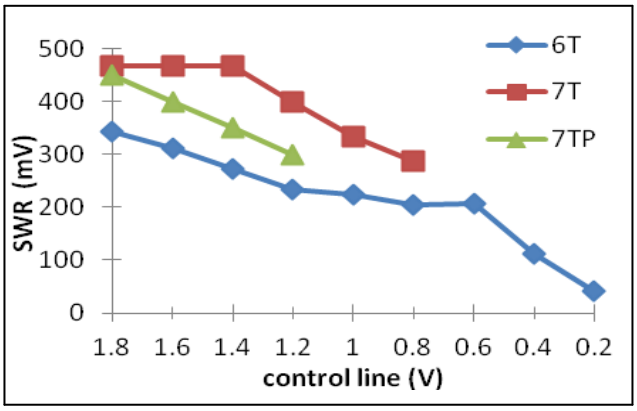


Figure 8. Effect of control voltage on SWM

B. Power Consumption:

Power consumption of memory part is increased due to increased in area of on chip memory. According to ITRS data memory cells will occupy 90% chip area by 2012 [8]. This paper present a very low power 7TP SRAM cell based on PMOS access transistor, without employing VDD[4]. Table(2) shows a power consumption comparison between 6T, 7TN and 7TP. Power consumption of 6T is more due to precharging of bit lines while in 7TP there is no direct path for bit lines[3] [4]. 7T design improves power consumption by 51%.

TABLE 2. POWER CONSUMPTION

Cell	*Vdd (V)*	*Operation*	*Power*
6T	2.2	WR '1'	271.2µW
		WR '0'	158 µW
7TN	2.2	WR '1'	134 µW
		WR '0'	1.4 nW
7TP	0	WR '1'	100.7µW
		WR '0'	437 pW

IV. CONCLUSION

In present work a comparison of static write margin (SWM), power consumption for 6T, 7TN (with NMOS access transistor) and 7TP (with PMOS access transistors) have been presented. SRAM cells with 6T, 7TN and 7TP shows SWM of 0.272V, 0.390V and 0.380V (VWL) respectively. Power consumption of 271.2µW,134µWand100.7µWhave been obtained for 6T, 7TN and 7TP respectively for WR '1' and power consumption of 158µW, 1.4 nW, 437pWhave been obtained for 6T, 7TN and 7TP respectively for WR '1'. 7TP SRAM cell shows improve performance as with 62% power saving compared to 6T SRAM cell.

REFERENCES

[1] Benton Calhoun and A. Chandrakasan,"Static noise margin Variation for sub-threshold SRAM in 65nm CMOS," in IEEE Journal of Solid-State Circuits, Vol.41, No.7, July 2006.

[2] Vasudha Gupta and MohabAnis," Statistical Design of the 6T SRAM Bit Cell," IEEE Transaction on circuits and system, VOL. 57, NO. 1, pp. 93-103 Jan. 2010.

[3] Ramy E. Aly and Magdy A. Bayoumi,"Low Power Cache Design Using 7T SRAM Cell" IEEE Journal, pp.318-322, Oct. 2007.

[4] Yen Hsiang Tseng, Yimeng Zhang, Leona Okamura and Tsutomu Yoshihara, "A new 7-transistor SRAM cell design with high stability," IEEE International Conference on Electronic Device, System and Application, 2010.

[5] Sherif A. Tawfik and VolkanKurusu, "Stability enhancement techniques for nanoscale SRAM circuits: A comparison," IEEE International SoC Conference, 2008.

[6] Ramy E. Aly and Magdy A. Bayoumi, "Prechargedsram cell for ultra low power on chip cache" IEEE, pp.95-98, July 2005.

[7] Jiajing Wang, SatyanandNalam,"Analyzing static and dynamic write margin for nanometer SRAM," ISLPED'08, Bangalore, India, Aug. 11-13,2008.

[8] International Technology Roadmap for Semiconductor 2005. http://www.itrs.net/links/2005itrs/home2005.htm.

[9] Anantha P. Chandrakasan, Samuel Sheng, "Low-Power CMOS Digital Design", IEEE Journal of Solid State Circuits, vol. 27, no. 4, p. 473-484, Apr. 1992.