International Journal of Advances in Electronics Engineering
Vol:1 Issue:1 ISSN 2278 - 215X

A Study and Comparison of Low Power CMOS Voltage Reference

SandeepK.Arya, Manoj Kumar, Ashok Kumar
Department of Electronics & Communication Engineering
Guru Jambheshwar University of Science & Technology, Hisar, India(125001)
ashokkdhania@gmail.com

***Abstract*-This paper presents a study and comparison between CMOS low power voltage reference in terms of voltage independent over the temperature .The reference voltage circuits are designed &simulated in SPICE with0.35-µm technology with supply voltage (VDD) of 2.5V & 1.8V respectively. The simulated results show that the circuits generate an average reference voltage of 246.66 mV & 817.0mV respectively and there is only small variation of ±2mV &±0.2mV from the temperature range of -40°C to 120°C. The circuits consume approximately 10.49µW&69.8 µW of power dissipation from a supply voltage of 2.5V & 1.8-V respectively.**

I. INTRODUCTION

Low voltage and low power are two important design criteria in both the analog and digital systems. It is expected that the whole system will be able to operate down to a single 1 V supply in the near future [1], [2]. A voltage reference, as one of the core functional blocks in both analog and digital systems should be able to operate from a single 1 V supply for both systems.The voltage reference circuit is an essential element in the design of biasing schemes for analog or mixed-signal circuits, such as high precise analog to digital converters, digital to analog converters in DRAM's, flash memories, and analog devices etc.The main purpose of the voltage reference is to provide a voltage or current that is insensitive to supply voltage, temperature and process variations. Most of common voltage reference is the band gap reference (BGR) voltage based on bipolar devices [3].DC values can produce undesirable effects such as bit errors in analog-to digital converters, non-linearity in RF mixers and low-noise amplifiers (LNA) [4]. Circuit design techniques have been developed to provide nearly zero or small DC variations with respect to each of threeerror generating parameters: temperature, process and supply. By using MOS devices in weak inversion, the constant bias current can be reduced to a few hundred nano-amperes, thus achieving very low quiescent power dissipation[5].

A study is given by the Allam and Filanovsky regarding about the MOSFET temperature behavior, the gate–source voltage of a MOSFET after biasing with a fixed drain current decreases with temperature [6]. Due to this condition a gate–source voltage can be used to design a voltage reference independent of temperature.

Here, in this paper the work reported by the G.Giustolisi, G. Palumbo et al. [7] &Shihabudheen T, V. Suresh Babu et al. [8] isextended.

II. CIRCUIT DESCRIPTION

A. The Voltage Reference with current bias:

Fig. 1 shows the voltage reference[7] circuit-I topology. It consists of two main sub-circuits. The first such circuit is composed of four MOSFET transistors M_{N1}, M_{N2}, $M_{P3,}$ M_{P4}, bias current (I_B), capacitor C_1 and the resistor R_1. The second such circuit is composed of transistors $M_{P5}$to M_{P8}&$M_{N9}$to M_{N11}, capacitor C_2 and three resistors R_2, R_3, R_4 respectively.

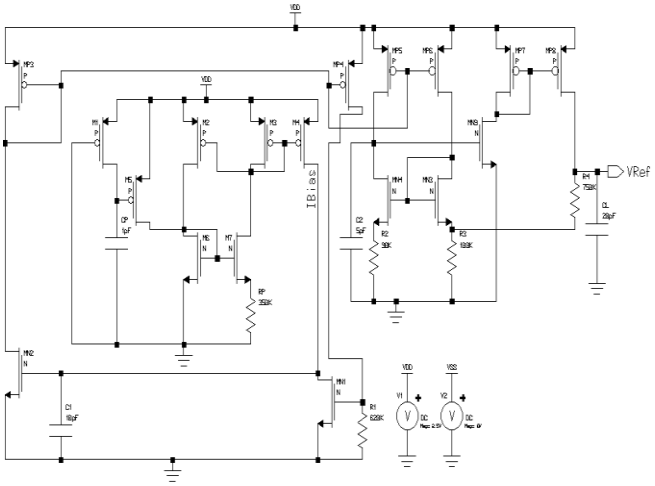

Fig. 1 Schematic of a Voltage Reference with Current Bias

Vol:1 Issue:1 ISSN 2278 – 215X

The current I_{R1}that flows in the resistor R_1 of the voltage reference circuit gives the V_{Ref} as the sum of proportional to absolute temperature (PTAT) component and gate to source voltage (V_{GS}) component. The voltage reference circuit shown in the fig. 1 is consists of two capacitors C_1 & C_2 which are used for stability of the circuit and for the proper compensation. In the circuit, capacitor C_L is used for the any capacitive load. When the gate to source voltage of a MOS transistor is reduced below the threshold voltage due to the strong inversion characteristics, so channel current decreases exponentially.

The current-voltage characteristics of a MOSFET in a subthreshold region under the condition $V_{DS}>4U_T$ is given by the equation

$$I_D = SI_{D0} \exp\left(\frac{V_G}{nU_T}\right) \exp\left(-\frac{V_S}{U_T}\right) (1)$$

WhereI_{D0} is a process-dependent characteristic current which can be considered as known for a given technology and V_G and V_S are the gate and the source voltage with respect to the bulk.

The current I_{R1} flowing in the resistor R_1 of the voltage reference circuit is given as

$$I_{R1} = \frac{V_{GS1}}{R_1} \quad (2)$$

Current I_{R1} is mirrored through transistors M_{P5} and M_{P6}, due to the transistors dimension ratios.

$$I_{DP5[P6]} = \left(\frac{S_{p5[P6]}}{S_{p4}}\right) I_{R1} (3)$$

The voltage V_{R3} is produced by resistor R_3 due to feedback across transistors $M_{N10}$and M_{N11} provided by $M_{N8}$and M_{P8}.

$$V_{R3} = \frac{S_{p5} R_2}{S_{p4} R_1} V_{GS1} + U_T \ln\left(\frac{S_{N11} S_{p5}}{S_{p7} S_{p6}}\right) \quad (4)$$

The reference voltage $V_{Ref}$is given as the sum of voltage drop through resistor R_3 and R_4.

$$V_{Ref} = R_4 I_{R4} + V_{R3} = R_4 \left(\frac{V_{R3}}{R_3} - \frac{S_{P6}}{S_{P4}} I_{R1}\right) + V_{R3} (5)$$

After putting the given values the reference voltage V_{Ref}becomes

$$V_{Ref} = \alpha V_{GS1} + \beta U_T (6)$$

Here, the values of α and β is given by

$$\alpha = \left(\frac{R_4}{R_3} + 1\right) \frac{R_2}{R_1} \frac{S_{p5}}{S_{p4}} - \frac{R_4}{R_1} \frac{S_{p5}}{S_{p6}} (7)$$

$$\beta = \left(\frac{R_4}{R_3} + 1\right) ln\left(\frac{S_{N11}}{S_{N10}} \frac{S_{P5}}{S_{P6}}\right) \quad (8)$$

Where I_D is drain current, U_T = kT/q is thermal voltage & S_N,S_P are the transistor aspect ratio of P & N-type MOSFET's.

B. The Bias Current Circuit:

The Bias current generator shown in fig. 2 is generating a bias current I_B for the voltage reference which is independent of temperature. The bias current I_B is generated by the transistor M_4.

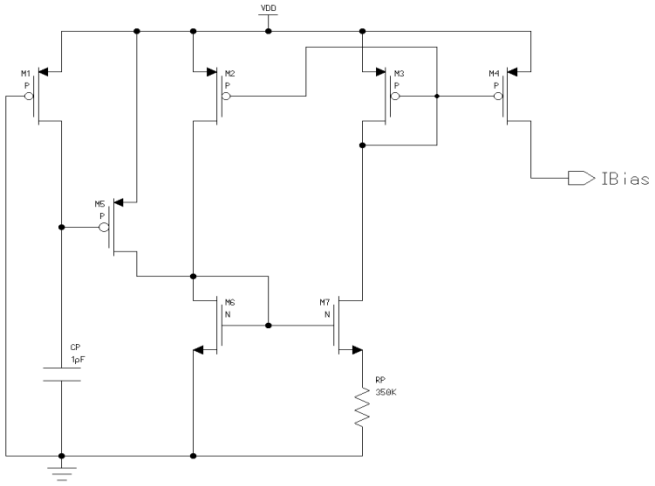

Fig. 2 Schematic of Bias Current

C. The Voltage Reference with error amplifier:

Fig.3 shows the voltage reference [8] circuit-II with error amplifier composed of op-amp, MOSFET's and the resistors.

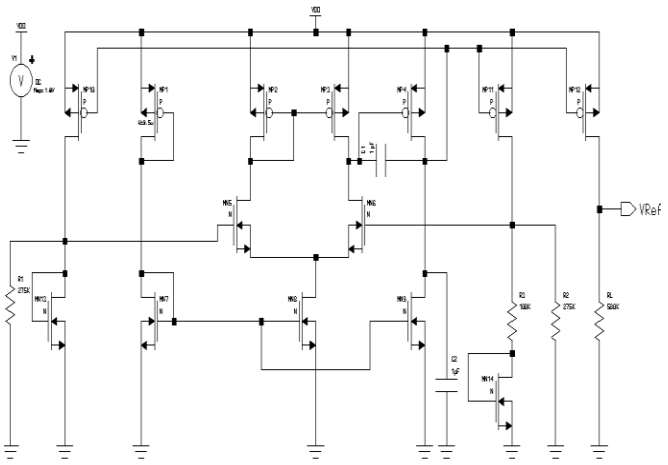

Fig. 3 Schematic of Voltage Reference with Error Amplifier

The PMOS transistors M_{P10},M_{P11} and$M_{P12}$are operating in the strong inversion saturation mode. The transistors aspect ratio of M_{P10},$M_{P11}$and $M_{P12}$are same and both the resistors R_1 and R_2 are equal. Gate of transistors M_{P10},$M_{P11}$and $M_{P12}$are connected to a common node forming a current mirror which produce the current I_1, I_2 and I_3 of equal value. Also the aspect ratio of transistors M_{P1},M_{P2}, M_{P3},$M_{P4}$are same. The output reference voltage is generating through the load resistance R_L.

Due to the operation of the MOSFETs M_{N13} and M_{N14} in the sub threshold region, currents through the resistors $R_1$and R_2 decrease as the temperature increases. Transistors M_{P1} toM_{P4} andM_{N5} to M_{N6} make the op-amp. The op-amp acts as an error amplifier producing a proportional to absolute temperature (PTAT)current through the resistor R_3.The current flowing through transistors M_{P10}, M_{P11} is sum of two currents i.e. one is proportional to $V_{GS}$and other is proportional to thermal voltage V_T. So, such current generated is temperature independent current, which will flow through the transistorM_{P12} due to current mirroring. Hence output reference voltage across the load resistor R_L is independent of supply voltage (V_{DD})and temperature variation.

The reference voltage thus produced is given by the equation

$$V_{Ref} = \frac{R_L}{R_2}\left(V_{GS1} + \frac{R_2}{R_3}\Delta V_{GS}\right) \qquad (9)$$

III. RESULTS AND DISCUSSION

The low power CMOS voltage reference with bias current circuit and voltage reference with error amplifier have been simulated in SPICE with 0.35-µm technology with supply voltage (VDD) of 2.5V and 1.8Vrespectively. Table 1.shows the comparison of result of process, minimum power supply voltage, reference voltage and power dissipation of these voltage reference circuits. Table1. shows that power dissipation of low voltage CMOS voltage reference is less as compared to other circuit. Fig. 4 to fig. 9 shows the reference voltage vs. temperature, supply voltage &time relationship for voltage reference with current bias and voltage reference with error amplifier. Fig. 4 and fig. 7 show that there is small variation of reference voltage over the temperature range of-40 °C to 120 °C. Here fig. 6 shows that reference voltage is constant with time for the voltage reference with current bias and fig. 9 shows that reference voltage is approximately constant with time for the voltage reference with error amplifier.

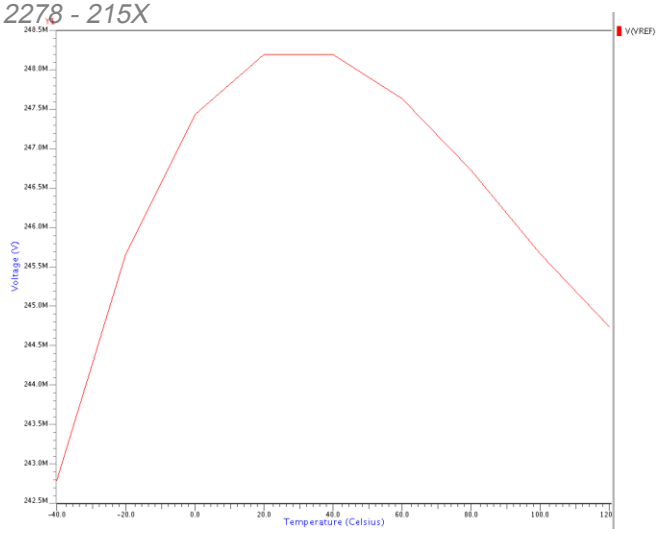

Fig. 4 Reference Voltage vs. Temperature of Voltage Reference with Current Bias

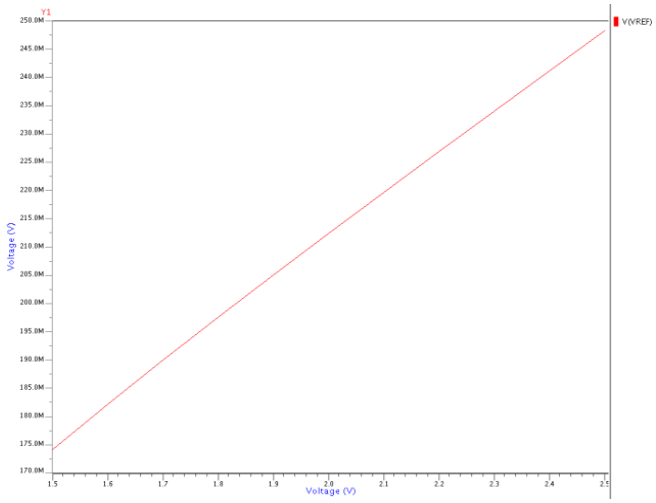

Fig. 5 Reference Voltage vs. Supply Voltage of Voltage Reference with Current Bias

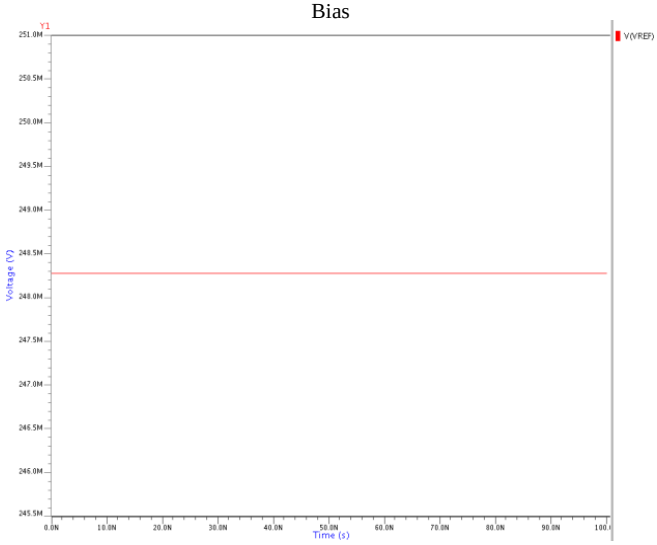

Fig. 6 Reference Voltage vs. Time of Voltage Reference with Current Bias

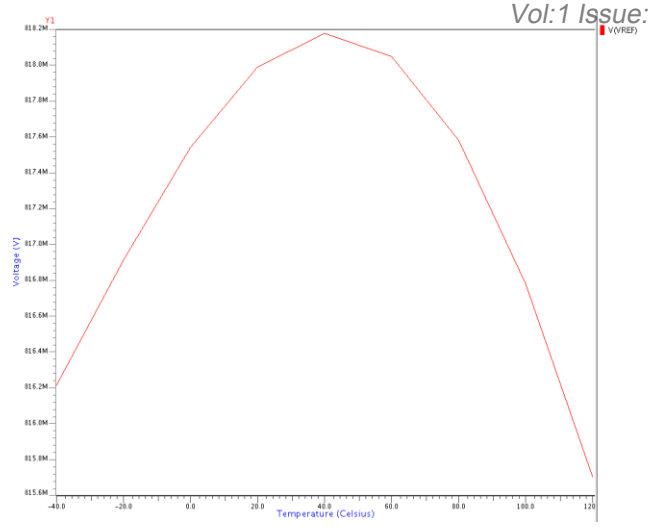

Fig. 7 Reference Voltage vs. Temperature of Voltage Reference with Error Amplifier

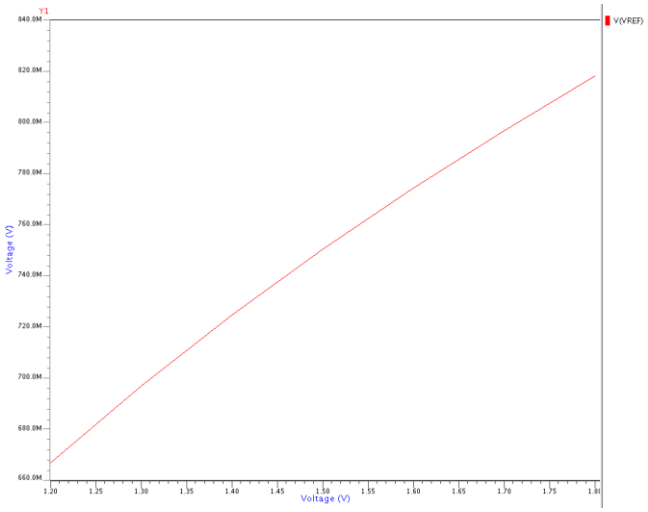

Fig. 8 Reference Voltage vs. Supply Voltage of Voltage Reference with Error Amplifier

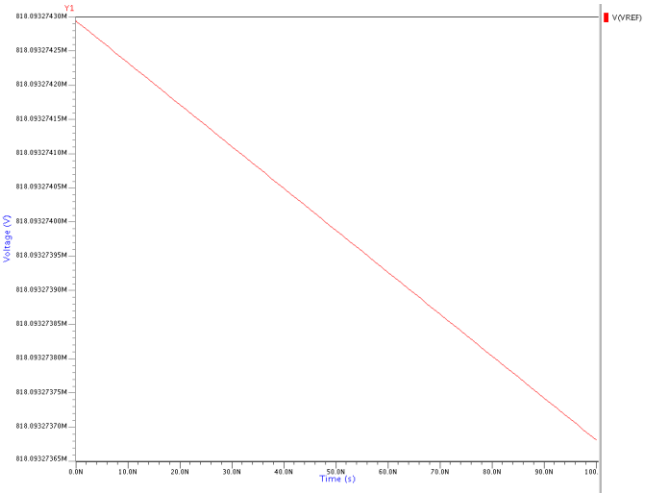

Fig. 9 Reference Voltage vs. Time of Voltage Reference with Error Amplifier

TABLE I. COMPARISION BETWEEN VOLTAGE REFERENCES

	Minimum Supply Voltage (V)	Reference Voltage (mV)	Power Dissipation (µW)	Process Technology (µm)
[7]	1.5	246.66	10.49	0.35
[8]	1.2	817.37	69.8	0.35

IV. CONCLUSION

The low power CMOS voltage reference with bias current circuit and voltage reference with error amplifier have been simulated in SPICE with 0.35-µm technology with supply voltage (VDD) of 2.5 V and 1.8 V respectively. The simulated results show that the circuits generate a reference voltage of 246.66 mV & 816.20mV respectively and there is only small variation of ±0.1mV &±0.2mV from the temperature range of -40°C to 120°C. The circuits consume approximately 10.49µW&69.8µW of power dissipation from a supply voltage of 2.5V & 1.8V respectively. The total variation in the reference voltage is 2.27% over the temperature range of -40 to 100˚C for the voltage reference with current bias and 0.25% over the temperature range of -40 to 100˚C for the voltage reference with error amplifier.

REFERENCES

[1] Pierazzi, Andrea, et al., "Band-gap reference for near 1-V operation in standard CMOS technology", IEEE 2001 custom integrated circuits conference, pp. 463-466, 2001.

[2] K.N. Leung and P.K.T. Mok, "A sub 1V 15ppm/˚CCMOS bandgap voltage reference without requiring low threshold voltage device," IEEE journal of solid-statecircuits, vo1.37, pp.526-530, April 2002.

[3] R. J. Widlar, "New developments in IC voltage regulators," IEEE J.Solid-State Circuits, vol. SC-6, pp. 2–7, Feb. 1971.

[4] Baker, Jacob R., Li, Harry W.et al., CMOS circuitdesign, layout, and simulation, New York, IEEE Press, 1998.

[5] K. Manetakis, "CMOS micro-power output stage for integrated voltage references," Electronics Letters, 22nd July,2004, Vol.40,No.15.

[6] M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," IEEE Trans. Circuits Syst. I, vol. 48, pp. 876–884, July 2001.

[7] G. Giustolisi, G. Palumbo et al., "A low-voltage low-power voltage reference based on subthreshold MOSFETs," IEEE Journal of Solid-State Circuits, Vol. 38, No. 1, January2003.

[8] Shihabudheen T, V.SureshBabu et al.,"A low power sub 1V 3.5ppm/°C voltage referencefeaturingsubthresholdMOSFET's," IEEE ICECS 2008, pp. 438-441, Nov. 2008.