International journal of Advances in Electronics Engineering
Vol:1 Issue:1 ISSN 2278 - 215X

A Comparative Study of Dynamic Latch Comparator

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***Abstract*- This paper presents the comparison between CMOS dynamic latch comparators. The circuit has been simulated using SPICE tool with 0.35µm technology, supply voltage of 3 V and 3.3V respectively. The circuits studied and simulated in this paper are Preamplifier dynamic latch circuit that consists of a preamplifier followed by a doubleregenerative dynamic latch and the Buffered dynamic latch circuit that consists of a basic dynamic latch comparator followed by an inverter buffer stage. The power dissipation of preamplifier latch and buffered latch comparator operating at frequency 160 MHz and 100 MHz are 960.129 µW and 1.132 mW respectively.**

Keywords: Analog to digital converter(ADC), Buffer, preamplifier.

I. INTRODUCTION

High speed low power dynamic latch comparators are the main building blocks for high speed flash analog to digital convertors (ADC) [3]. Such ADC's are widely used in many applications such as data storage systems, fast serial links and high speed measurement instruments. There are several most popular structures of high speed comparators like multistage open loop comparator, the regenerative latch comparator and the preamplifier latch comparator [5]. Among all these comparators, the multistage open loop comparator can obtain high speed and good resolution easily. In these days dynamic latched comparators are widely used to satisfy the need for high speed and low power consumption. In preamplifier latched topology an amplifier is added before a latched comparator which significantly decreases the effects of the offset voltage errors caused by device mismatch. Transmission gates are used between preamplifier and latch to control the signal path and to provide high gain to the output signal of the amplifier using charge injection phenomenon [1]. The major disadvantages of dynamic latch are the kickback noise produced by high transmission currents which induces spikes at the differential input voltage signal and the offset error caused due to the device mismatch [1]. In buffered latch comparator inverter buffers are added to the output of the dynamic latch comparator to isolate the comparator output from large capacitive loads [2].

The circuits presented in this paper are taken from [1] and [2]. The power consumption of preamplifier latched comparator presented in paper [1] operating at frequency 40MHz based on 0.6µm technology is 750µW. The power consumption of buffered latched comparator presented in paper [2] operating at frequency 100MHz based on 0.5µm technology is 70nW.

The paper is organized in four sections. Section II describes the detailed circuits of dynamic latch comparators. Section III describes the simulation results and comparisons. Finally, conclusion has been explainedin section IV.

II. CIRCUIT DESCRIPTION

A. Preamplifier dynamic latch comparator:

The preamplifier latch circuit has been studied in this paper. The basic principle of preamplifier latch circuit is that the preamplifiers amplify the input signal and later the amplified signal is fed to the input of dynamic latch comparator using transmission gates [7]. The preamplifier latch comparator has low propagation delay as compared to the latched comparator.

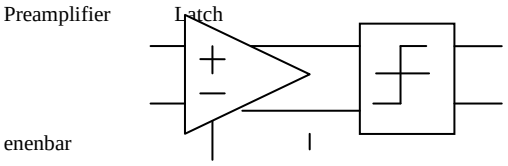

Figure 1. Block diagram of comparator

Preamplifier: The preamplifier uses fully differential circuit structure as shown in figure 2. The preamplifier should have wide bandwidth and small gain to achieve high speed. The preamplifier decreases the effects of the offset voltage error due to device mismatch. Thepreamplifier prevents any disturbances due to the kickback noise [1].

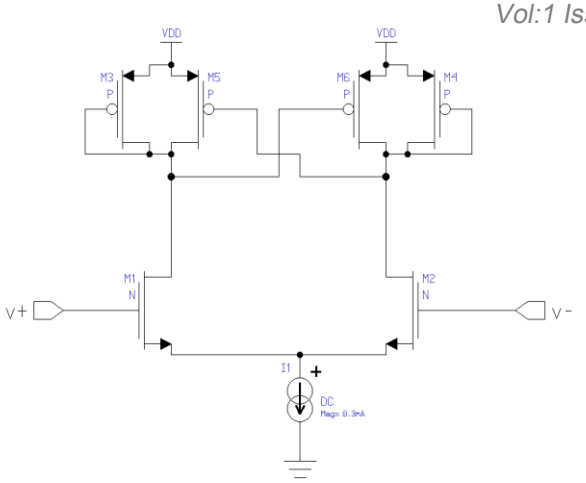

Figure 2. Preamplifier circuit [1]

2) Dynamic Latch: The latch type comparator consists of a preamplifier stage followed by a latch stage. The latch employed can be divided in to two groups: static latch comparators, dynamic latch comparators [4]. In dynamic latch comparators two cross coupled CMOS inverters are used for regeneration. A clock is used to set the comparator in active or standby mode [2].

The dynamic latch comparator can achieve a high speed without limitation of quiescent point. However, if the output nodes of preamplifier are directly connected to the regeneration nodes, kickback noise is produced. Kickback noise is produced due to high transmission currents resulting in voltage spikes at the voltage differential input signal. Hence, transmission gates are used to control the signal path between preamplifier and latch.

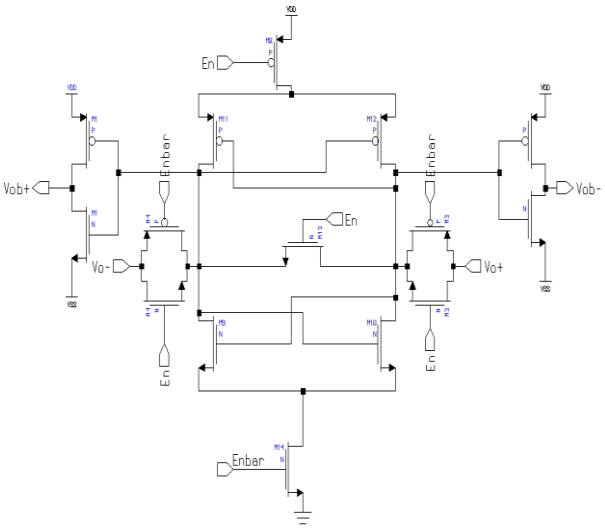

Figure 3. Dynamic latch comparator [1]

The dynamic latch studied in this paper consists of two cross coupled pair of NMOS and PMOS transistors which are connected to groundthrough a clock enabled transistor. The pair of PMOS and NMOS transistor combination reduces the time constant up to 25% as compared to single regeneration counterpart [1]. The transistor sizes should be as small as possible to meet high speed and low parasitic capacitance requirements.

Offset in Dynamic Latch: The offset voltage of the dynamic latch can be expressed as [1]

$$V_{offset} = \Delta V_{th} + \frac{1}{2}\left(\frac{\Delta W}{W} - \frac{\Delta L}{L}\right)(V_{GS} - V_{th}) + \frac{\Delta Q}{C_D} \quad (1)$$

Where, ΔV_{th} is the standard deviation of the threshold voltage, $\Delta w/w$ is the width dimension mismatch, $\Delta L/L$ length dimension mismatch, V_{gs}-$V_{th}$is the overdrive voltage at the beginning of dynamic latch regeneration phase ΔQ is the charge due to switches controlling nodes V_{out+} and V_{out-} and C_D denotes the total equivalent capacitance in the output nodes of the dynamic latch. ΔV_{th}can be expressed as [1]

$$\sigma(V_{TH}) = \frac{A_{VTH}}{\sqrt{WL}} \quad (2)$$

Where, A_{VTH} is the technology dependant factor measured inV.µm.

3) Preamplifier Dynamic Latch Comparator:

Figure 4 shows the dynamic latch comparator with preamplifier when the clock signal e_n goes high the comparator enters the reset phase. The comparator is resetting through the shorted transistor M13 between the two cross coupled inverters.When e_n goes low the circuit enters the comparison phase. Transistor M8 is connected to the voltage supply and M4 is connected to ground. The transmission close and the comparator enter the regenerative phase.

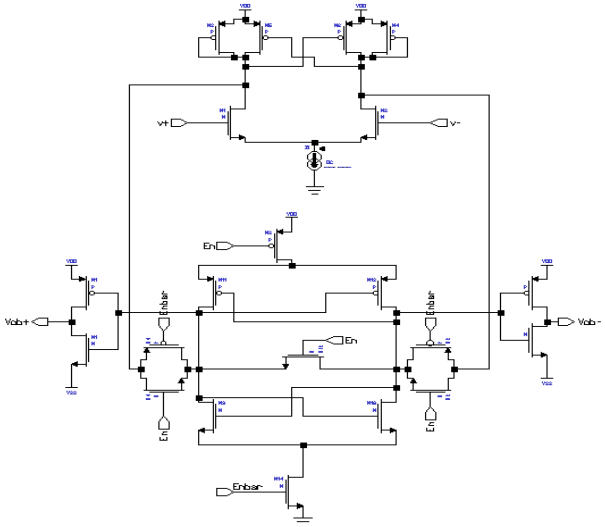

Figure 4. Dynamic latch comparator using preamplifier

A. Dynamic latch comparator using inverter buffer:

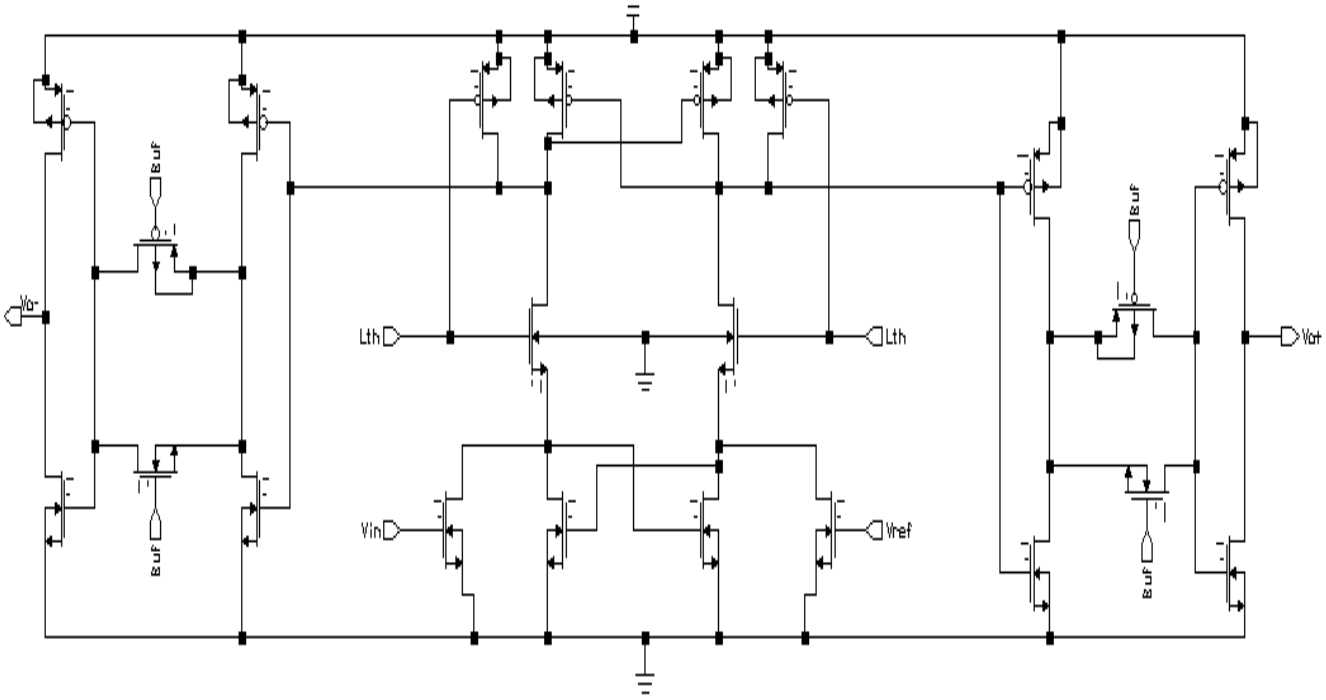

Figure 5. Dynamic latch comparator with inverter buffer [2]

The schematic of the dynamic latch comparator is shown in figure 5 [2]. Transistors M1, M9 and M2, M7 form the pair of inverters and their outputs are connected to the inputs of the other. When the latch signal $L_{th}$is low and thetransistors M5 and M8 are off M1, M2 are separated from M9 and M7 and the output node is pre charged to digital '1' by the transistors M3 and M4 when the latch signal $L_{th}$is high. The transistors M5 and M8 are on and the drain voltages of M1 and M2 start dropping from the positive rail. If the input is larger than the reference, the voltage at drain of M1 will drop faster than the output node. When the input reaches V_{DD}-V_{th}, M2 starts turning ON and triggers the regenerative feedback.

The major drawback of the dynamic latch comparator is the offset error caused by transistor mismatch and unbalanced charge residues [8]. The basic principle of a dynamic latch comparator comes from its positive feedback that triggers the regenerative action. This operation becomes quite slow when the voltage is in the small signal range and a large capacitive load at the output will greatly degrade the speed [9].

In figure 5 inverter buffers are added to isolate the comparator output and the large load capacitance. The function of the switches used between the pair of inverters of buffers is to connect and disconnect the buffer output. The inverter buffers are used to minimize the offset errors.The timing signals latch (L_{th}) and the buff (clk) signals must be designed carefully to correctly represent the relationship between input and the reference.

III. SIMULATION RESULTS

Based on ELDO SPICE model of TSMC 0.35µm CMOS process, the dynamic latch comparatorwith preamplifier and buffered dynamic latch comparator were simulated under supply voltage of 3V and 3.3V respectively. Figure6, 7 and 8 respectivelyshows the simulation results corresponding to dynamic latch comparator using preamplifier operating at frequency 160 MHz. and buffered dynamic latch comparator operating at frequency 100 MHz.

TABLE 1.COMPARISON OF DIFFERENT COMPARATOR

Author	Dynamic latch comparator with preamplifier		
	Technology	***Frequency***	***Power***
Carlos J Solis,2010 [1]	0.5µm	40MHz	750µW
This paper	0.35µm	160MHz	960.13µW

Author	Buffered Dynamic Latch Comparator		
	Technology	***Frequency***	***Power***
Zhaohui Huang,2005 [2]	0.5µm	100MHz	70nW
This paper	0.35µm	100MHz	1.13mW

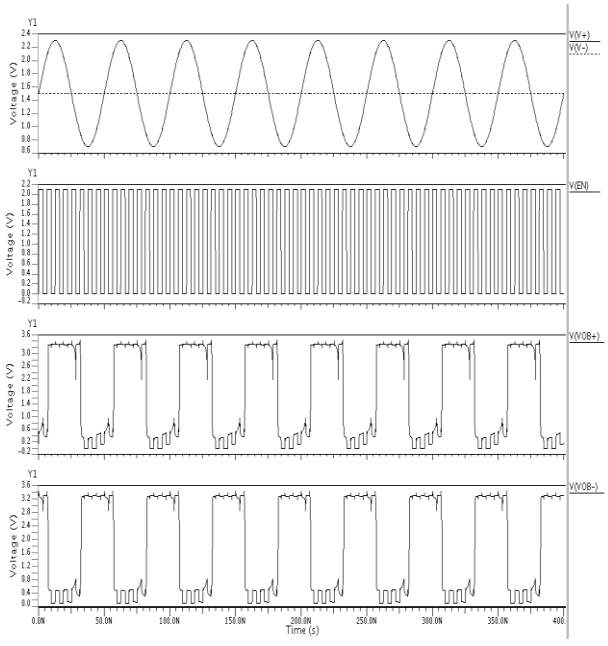

Figure 6. Dynamic latch comparator with preamplifier

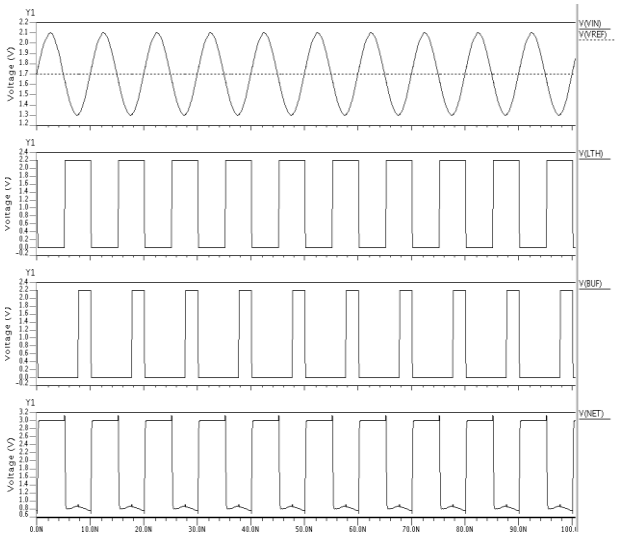

Figure 7. Dynamic latch comparator without buffer

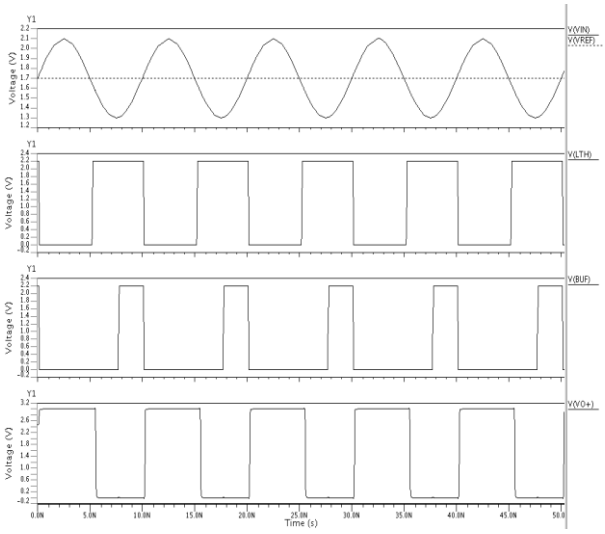

Figure 8. Buffered dynamic latch comparator

IV. CONCLUSION

The circuits presented in papers [1] and [2] were studied and simulated using SPICE tool with 0.35µm technology. The power consumption of the preamplifier based comparator operating at frequency 160MHz is 960.13µW and that of the buffered comparator operating at frequency 100MHz is 1.13mW. The output waveforms after simulation were studied successfully.

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