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Implementation of LFSR Counter Using CMOS VLSI Technology

M.Mahaboob Basha[1]
Associate Professor, Department of ECE
AVR&SVRCET
Nandyal, India
mmehboobbasha@gmail.com

K.Vasudeva Reddy[2]
Assistant Professor, Department of ECE
AVR&SVRCET
Nandyal, India
Vasureddy60@gmail.com

H.Devanna[3]
Associate Professor, Department of ECE
SJCET
Yemiganur, India
Devanna_03@yahoo.co.in

B.Pradeep[4]
UG Student, Department of ECE
AVR&SVRCET
Nandyal, India
deepusummi@hotmail.com

***Abstract*— As chip manufacturing technology is suddenly on the threshold of major evaluation, which shrinks chip in size and performance, LFSR (Linear Feedback Shift Register) is implemented in layout level which develops the low power consumption chip, using recent CMOS, sub-micrometer layout tools. Thus LFSR counter can be a new trend setter in cryptography and is also beneficial as compared to GRAY & BINARY counter and variety of other applications. This paper compares 3 architectures in terms of the hardware implementation, CMOS layout and power consumption, using Microwind CMOS layout tool. Thus it provides solution to a low power architecture implementation of LFSR in CMOS VLSI.**

Keywords-Chip technology, Layout level, LFSR, Pass transistor.

I. Introduction

With advancements in large scale integration, millions of transistors can be placed on a single chip for implementation of complex circuitry. As a result of placing so many transistors in such a small space, major problems of heat dissipation and power consumption have come into the picture. Research has been conducted to solve these problems. Solutions have been proposed to decrease the power supply voltage, switching frequency and capacitance of transistor [1] LFSR is used in a variety of applications such as Built-in-self test (BIST) [2], cryptography, error correction code and in field of communication for generating pseudo-noise sequences. In cryptography it is used to generate public and private keys. Hence one of the low power architecture is proposed in this paper.

Today LFSR's are present in nearly every coding scheme as they produce sequences with good statistical properties, and they can be easily analyzed. Moreover they have a low-cost realization in hardware.

Counters such as Binary, Gray suffer problem of power consumption, glitches, speed, and delay because they are implemented with techniques which have above drawbacks. They produce not only glitches, which increase power consumption but also complexity of design. The propagation delay of results of existing techniques is more which reduces speed & performance of system. Thus we are going to implement these counters with techniques using different technologies of CMOS. By studying different implementation techniques, we conclude to implement LFSR counters with pass transistor in cryptography.

Unlike most everyday devices whose inputs and operations are effectively predefined, VLSI chips must be able to react to a constantly changing environment.

For layout and simulation at deep submicron CMOS design tool Micro wind is used. Software implementations will be considered for further hardware implementation.

II. LFSR

LFSR is a *shift register* whose input bit is a *linear* function unlike most everyday devices whose inputs and operations are effectively predefined, It is a shift register that, when clocked moves the signal through the register from one flip flop to next. Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism. A LFSR can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip flops as shown in Figure.1.

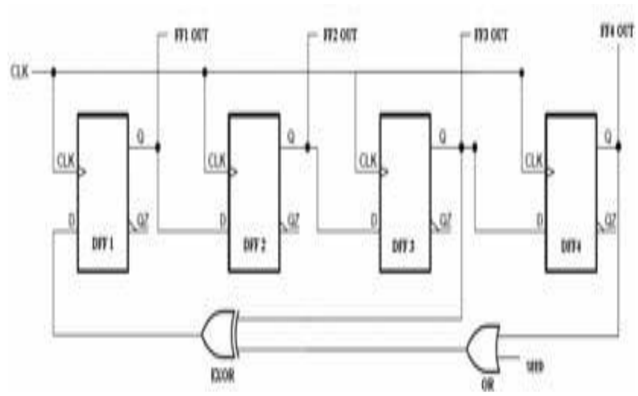

Figure.1 Block diagram of LFSR

The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the sequence of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, a LFSR with a well-chosen feedback function can produce a sequence of bits which appears random in nature & which has a very long cycle.

A. *Working*

The list of bits position that affects the next state is called the tap sequence. In block diagram, the sequence is [4, 3].The outputs that influence the input are called taps. A maximal LFSR produces an *n-sequence* (i.e. cycles through all possible 2n-1 states within the shift register except the state where all bits are zero), unless it contains all zeros, in which case it will never change. The sequence of numbers generated by a LFSR can be considered a *binary numeral system* just as valid as *Gray code* or the *natural binary code*.

TABLE I
PATTERN GENERATED BY LFSR

Clock pulse	*FF1 OUT*	*FF2 OUT*	*FF3 OUT*	*FF4OUT*
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	1	0	0	1
8	1	1	0	0
9	0	1	1	0
10	1	0	1	1
11	0	1	0	1
12	1	0	1	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	1	1	1

FF1 OUT-output of flip flop 1, FF2 OUT-output of flip flop 2, FF3 OUT output of flip flop 3, FF4 OUT-output of flip flop 4.

The tap sequence of an LFSR can be represented as a polynomial mod 2. This means that the coefficients of the polynomial must be 1's or 0's. This is called the feedback polynomial or characteristic polynomial. For example: if the taps are at the 3rd, 4th, bits the resulting LFSR polynomial is X4+ x3 +1.The '1' in the polynomial does not correspond to a tap. The powers of the terms represent the tapped bits, counting from the left.

If (and only if) this polynomial is a primitive, then the LFSR is maximal. The LFSR will only be maximal if the number of taps is even. The tap values in a maximal LFSR will be relatively prime There can be more than one maximal tap sequence for a given LFSR length. Its output for the various condition of input is expressed in Table I.

III. Design Aspects

We have designed CMOS layout of LFSR Counter .The logic hardware contains D Flip Flop, 2-input OR gate, 2 input XOR gate and inverters. The most important component of our LFSR Counter Design is D Flip Flop. We have designed D-flip flop by using following different components: NAND Gates, Transmission gates and inverter and Pass transistors.

A. *Design of D Flip Flop*

The latches and flip flops are the basic building blocks of sequential circuits. In ASIC design environments, latches and flip flops are typically predefined cells specified by the ASIC vendor. The D Flip Flop is negative edge triggered. The D Flip Flop combines a pair of D latches (Master and slave). The edge triggered D Flip Flop has a setup and hold-up time window during which the D inputs must not change. The negative edge triggered D Flip Flop simply inverts the clock input, so that all the action takes place on falling edge of CLK. By designing D Flip Flop, we compare the Power Consumption; from this we decide the most efficient D Flip Flop implementation.

B. *Design of D Flip Flop using NAND Gate*

The basic construction of the Master Slave D Flip Flop is shown in Figure.2

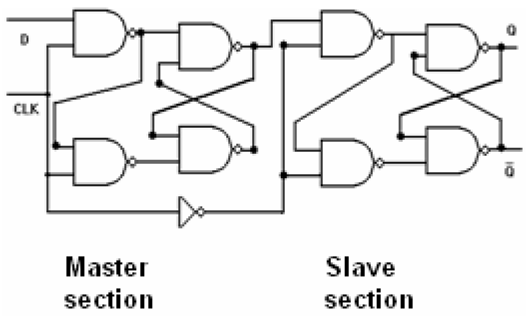

Figure 2 D Flip Flop using NAND gates

C. *Design of D Flip Flop using TRANSMISSION GATE*

From Figure.3, at the negative edge of the CLK (clock), transistors T1 and T4 are ON and transistors T2 and T3 are OFF. During this time the slave maintains a loop through two inverters I3, I4 and T4. Thus the previous triggered value from Din is stored in slave. At the same time master latches next state but as T3 is OFF it is not passed to slave. At the positive clock edge T2 and T3 are turned ON and new latched value passes to slave through the loop of two inverters I1, I2 and T2. When we want to reset the circuit, both the master and slave loops are pulled down to ground.

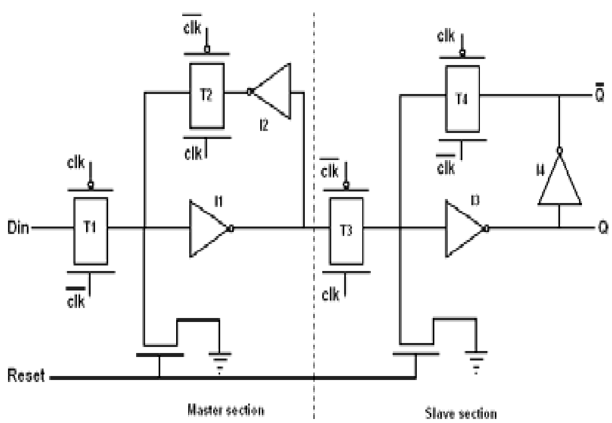

Figure.3 D Flip Flop using transmission gate

D. *Design of D Flip Flop using PASS TRANSISTOR*

The most compact implementation of edge trigger latch is based on inverters and passes transistors as shown in Figure.4. The two chained inverters are in memory state when the PMOS loop transistor is on, that is when clock = 0. Other two chain inverters on the right hand acts in opposite way, and the reset function is obtained by direct ground connection of the master and slave memories, using NMOS devices.

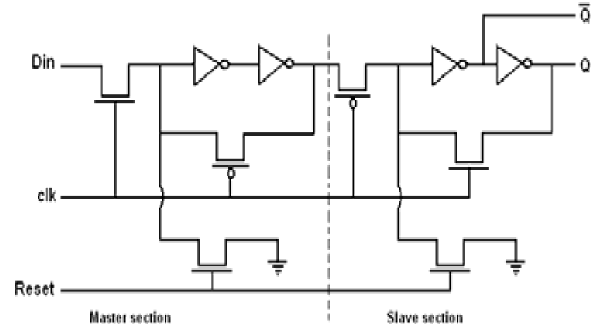

Figure.4 D Flip Flop using pass transistors

IV. LAYOUT ASPECTS

Layout-level environments exist primarily for the generation of final manufacturing specifications.

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A. *Layout of D FLIP FLOP*

Before implementing the whole circuit, a gate-level schematic in DSCH3 is generated. DSCH3 program is a logic editor and simulator used to validate the architecture of logical circuit, before microelectronics started. It provides user friendly environment for hierarchical logic design and fast simulation with delay analysis, which allows design and validation of complex logic structures.

After successful simulation we implemented the above designs of D Flip Flop with different components using Microwind 3.1 CMOS layout tool for its ease of use and availability. The result of the implementation is detailed below.

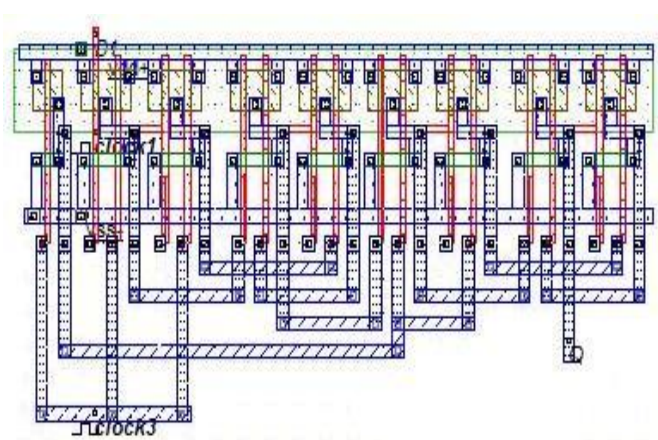

Figure.5 Layout of D Flip Flop using NAND gate

1) **D Flip Flop layout using NAND GATE**

Layout of LFSR counter in which D Flip flop is implemented using NAND gates is as shown in Figure.5.

2) D Flip Flop layout using TRANSMISSION GATE

Layout of LFSR counter in which D Flip flop is implemented using transmission gates is as shown Figure.6

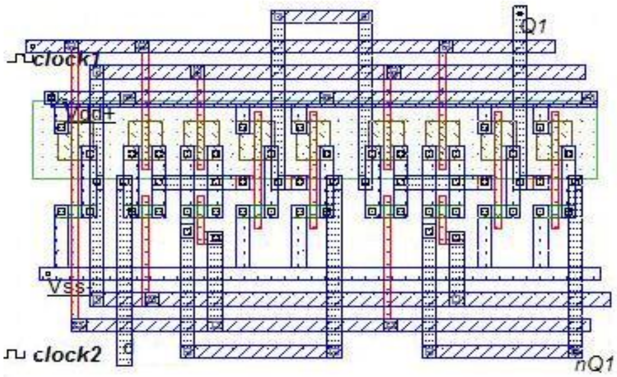

Figure.6 Layout of D Flip Flop using Transmission gate.

B. *D Flip Flop layout using PASS TRANSISTOR*

Layouts of LFSR counter in which D Flip Flop is implemented using transmission gates is as shown Figure.7.

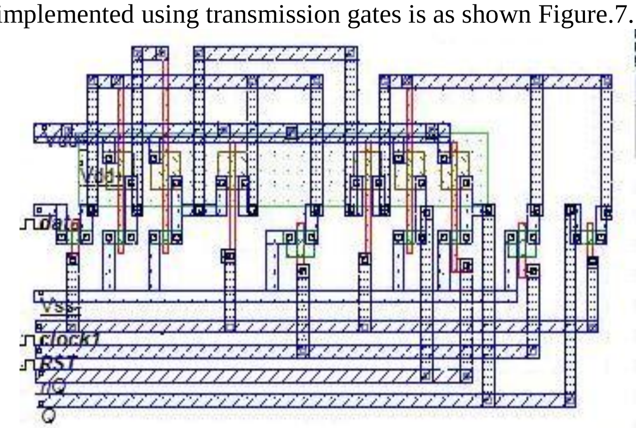

Figure.7 Layout of D Flip Flop using Pass transistor

C. *Result of LFSR Layout Implementation*

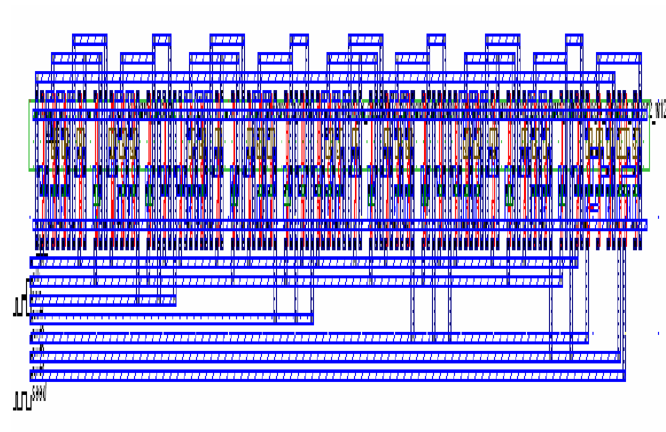

Figure.8 Layout of LFSR in Microwind

In Table II and III we have compared the LFSR layouts. The layouts are implemented in 120 nm and 90 nm technology respectively. The various parameters because of different technologies and D Flip Flop design is tabulated for further conclusion and CMOS layout using pass transistors is as shown in Figure.8.

TABLE II
LFSR IN 90 nm TECHNOLOGY

Components	No. of Transistors	Power consumption (Microwatt)	Max frequency (GHz)	Layout area (micro sq. meter)
NAND	148	106.0	1.96	295
Transmission Gate	86	99.6	1.7	270
Pass Transistor	68	28.188	1.4	321

TABLE III
LFSR IN 120 nm TECHNOLOGY

Components	No. of Transistors	power consumption (Microwatt)	Max frequency (GHz)	Layout area (micro sq. meter)
NAND	148	169	1.78	224.8
Transmission Gate	86	155	1.8	390.1
Pass Transistor	68	50.471	1.814	460

V. COMPARISON OF LFSR AND GRAY COUNTER LAYOUT

From Table II and III it is clear that LFSR is optimally implemented layout when compared with layout of gray counter. A layout of both counters is implemented using 120 nm and 90 nm technology. From the layouts various critical parameters are tabulated in Table IV.

TABLE IV
COMPARISION OF COUNTERS IN 90 nm TECHNOLOGY

Components	No. of Transistors	power consumption (Microwatt)	Max frequency (GHz)	Layout area (micro sq. meter)
GRAY	188	40.25	0.756	949.6
LFSR	68	28.188	1.4	321

VI. Conclusion

This paper concludes that LFSR counter is best implemented using the pass transistors. In this the number of transistors required is minimum i.e. 19, power consumption is 28.188 micro watt , Max operating frequency is 1.4 GHz, layout size area is 321 micro sq. meter. Thus it is preferable over Gray counters in maintaining the logic density in fabrication process, power optimization, reducing the propagation delay & glitches. Thus LFSR implemented in CMOS chip technology, is the best illustration of VLSI.

References

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