Simulation of Low Power Architecture of Finite State Machine

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Abstract — With the predominance of mobile devices, rising energy costs, and an awareness of green practices,power consumption has become a major concern for design engineers. When power consumption is analyzed, it breaks down into two main components: static or leakage power, which occurs naturally when components are idle and powered on; and dynamic power, which is the power consumed when components are switching. While both static and dynamic power remain important targets for power reduction, this paper will focus on architectural level techniques for reducing power. To further improve efficiency, designers must use innovative techniques at the architectural level. Further, analysis shows that datapath circuits often consume large amounts of dynamic power due to their large circuit size and high switching activities. They are especially impactful because they are often a major portion of the circuits that must be powered on for an extended time.
In this paper, we address the issue of low power realization of FSMs using decomposition and a gated clock architecture [9]. We decompose an state machine into two interacting machines and develop it at architectural level .To lower the power consumption of these circuits,designer propose a architecture level method to compute power in finite state machine .

Keywords : FSM Decomposition[1] ,Architectural level [2] ,Sub finite state machines , Decoder circuitry , Power consumption

1. INTRODUCTION

In CMOS circuits, power is dissipated in a gate when the gate output changes from 0 to 1 or from 1 to 0. Minimization of power dissipation can be considered at algorithmic, architectural, logic, and circuit levels. In sequential circuit design, an effective approach to reduce power dissipation is to "turn off" portions of the circuit, and hence reduce the switching activities in the circuit. In general, low power and high performance are usually two conflicting goals at all levels of the design hierarchy. For example, one common technique for reducing power consumption is to lower the supply voltage. This reduction in supply voltage, however, results in slower circuits. Higher frequencies are desirable for high performance, but they increase power consumption. Higher activity (and thus utilization) could result in a larger throughput, but also in higher power. The excessive power consumption of today's processors is, in part, the outcome of very high utilization of their components .
Power optimization at the architectural and software levels has attracted the interest of a number of researchers.In this article we propose a architectural level technique of computing power at original and decomposed FSM.

Objective of this paper is :
(1) Take a Mealy FSM , decompose it into parts .[1]
(2) To develop an architecture of Low Power FSM [2]
(3) To develop code in verilog
(4) To simulate it in MODELSIM .

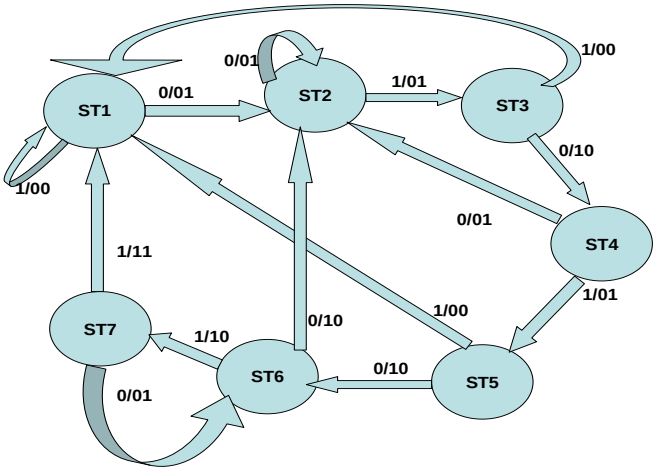
II. METHODS AND APPROACHES

The key steps in our approach are:
(1) Decomposition of a finite state machine into submachine so that there is a high probability that state transitions will be confined to the smaller of the sub machines most of the time.
(2) It is based on the concept in which the redundant computation can be dynamically disabled
to reduce the overall power dissipation
(3). When the input signal arrives, the active submachine remains active. In that case, the other
Submachine will not be turned on and remain inactive. On the other hand when next input signal arrives, the

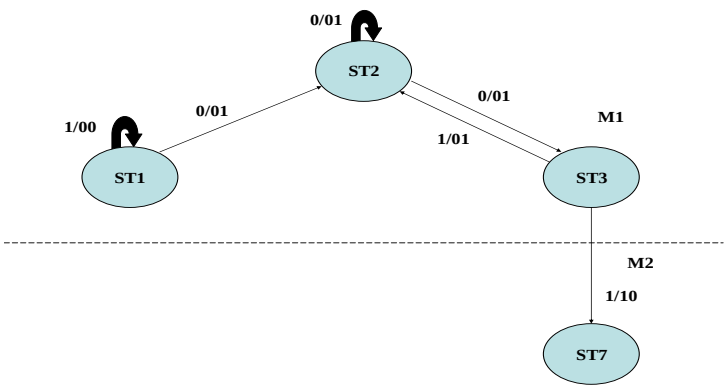
active submachine might turn on another submachine and turn itself off, becoming inactive
(4). At any moment, only one submachine is active (with its corresponding combinational circuit turned on) while all other sub machines are inactive (with their corresponding combinational circuits turned off).
(5) Compute power dissipation of original FSM and decomposed FSM at architectural level.[2]
(6) Compare the results for power consumption at architectural level
(7) Get simulated WAVEFORMS.

II. DECOMPOSITION APPROACH

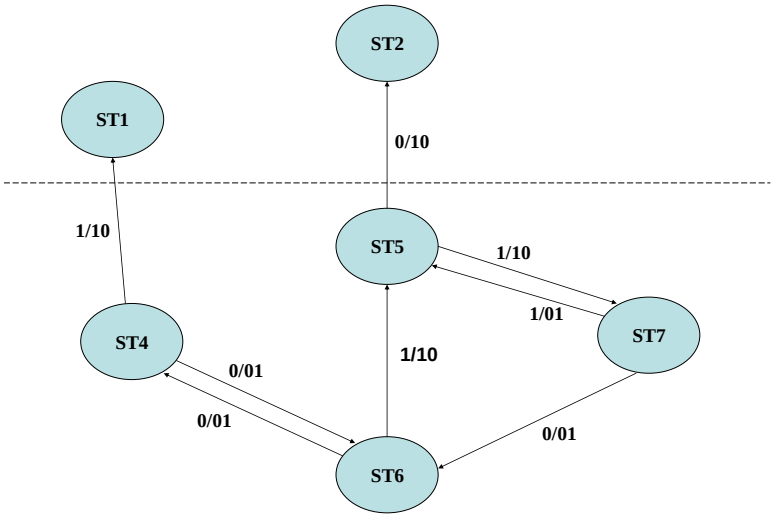
(1) Keep minimum crossing Transition to reduce power consumption.[2]
(2) First bit of state code is Control bit distinguish between Sub machines.
(3) Inner two bits are to distinguish between states within each submachine.



original FSM

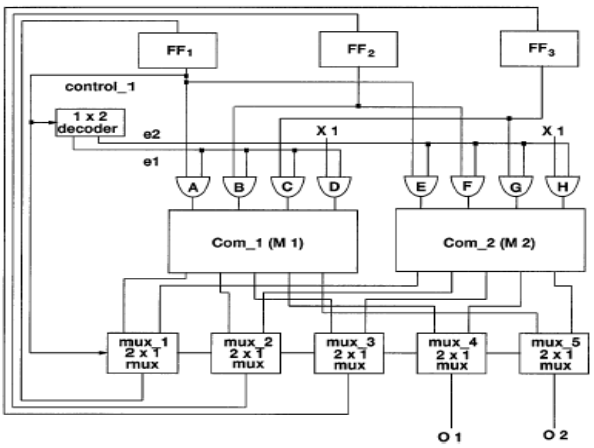


Upper half FSM



Lower half FSM

III. ARCHITECTURE OF LOW POWER FSM



Block diagram of low power architecture

There is one control signal, control_1 , which is the output of the first flip-flop; one 1x2 decoder which will generate the enable signals e1 and e2 for submachine M1 and M2 ; four AND gates A, B, C, D in front of M1 and four AND gates E,F,G,H in front of M2 which will block the state and primary input signals from propagating through M1 and M2 , respectively;three multiplexers mux1 , mux2 , mux3 which will determine whether the next state registers will be loaded from M1 or M2 ; and two multiplexers mux4 , mux5 which will determine the correct output signals[3]. Suppose submachine M1 is active and is in state s6 . Since the first bit of the state code (the control signal control_1)of s6 , which is the input to the 1x2 decoder, is 0, the output signal from the decoder to Com1 , e1 , is 1 which will turn on all the AND gates A, B, C, D in front of submachine M1 . Thus, all signals fed to the circuit corresponding to submachine M1 will propagate through. However, the output signal from the decoder to Com2 , e2 ,is 0 which will turn off all the AND gates D, E, F, G in front of submachine M2 . Thus, all signals fed to the circuit corresponding to submachine M2 will be blocked. Similarly, with the control signal control_1 being 0, signals for the next state flip-flops and output will come from Com1 through the, F, G, H in front of M2 which will block the state and 2x1 multiplexers. Now, if the input is 0, submachine M1 will transit to state START. Since the first bit of the state code of START is also 0, submachine M1 will stay active in the next clock cycle. On the other hand, if the input is 1, submachine M1 will transit to state s2 . Since the first bit of the state code (the control signal control_1)ofs2 is 1, the output signal of the decoder e2 will be 1 which will allow inputs to propagate through the AND gates E, F, G, H and Com2 , and thus turn on the submachine M2 .In the meantime, the value of e1 is 0 which will inhibit the propagation of inputs through the AND gates A, B, C, D, and thus set all the inputs to submachine M1 to 0s in the next clock cycle, rendering submachine M1 inactive. If in subsequent clock cycles state transitions are confined to within submachine M2 , the value of e1 will remain 0 and submachine M1 will remain inactive.

IV.COMPUTING POWER CONSUMPTION AT ARCHITECTURAL LEVEL

Results

Power consumption in Decoder circuitry	4.15Mw
Power consumption in Multiplexer circuit	3.45mW
Power consumption in AND gate	4.40mW
Power consumption in D Flip Flop	2.3mW
Power consumption in Original FSM	5.39mW

Table 1.1 Power consumption at architecture level for original FSM

Total Power consumption in the circuitry considering Original FSM is 20.06mW as calculated from Table 1.1.[2]

Power consumption in Decoder circuitry	4.15mW
Power consumption in Multiplexer circuit	3.45mW
Power consumption in AND gate	4.40mW
Power consumption in D Flip Flop	2.3mW
Power consumption in Decomposed FSM	3.55mW

Table 1.2 Power consumption at architecture level for decomposed FSM

Total Power consumption in the circuitry when Decomposed FSM is considered is 17.75mW as calculated from Table 1.2.

Considering the original FSM the power consumption is calculated as 20.06mW and when architecture of decomposed FSM is considered, power consumption was minimized to 17.75mW.

V. CALCULATION

At the Architecture Level

$P_{originalFSM}$ = 20.06mW

P_{subFSM} = 17.75mW

Percentage in power saving = $(P_{originalFSM} - P_{subFSM}) / (P_{originalFSM})$ = 12.10%

So total power saving of 12% is achieved at an architecture level.

VI. SIMULATION

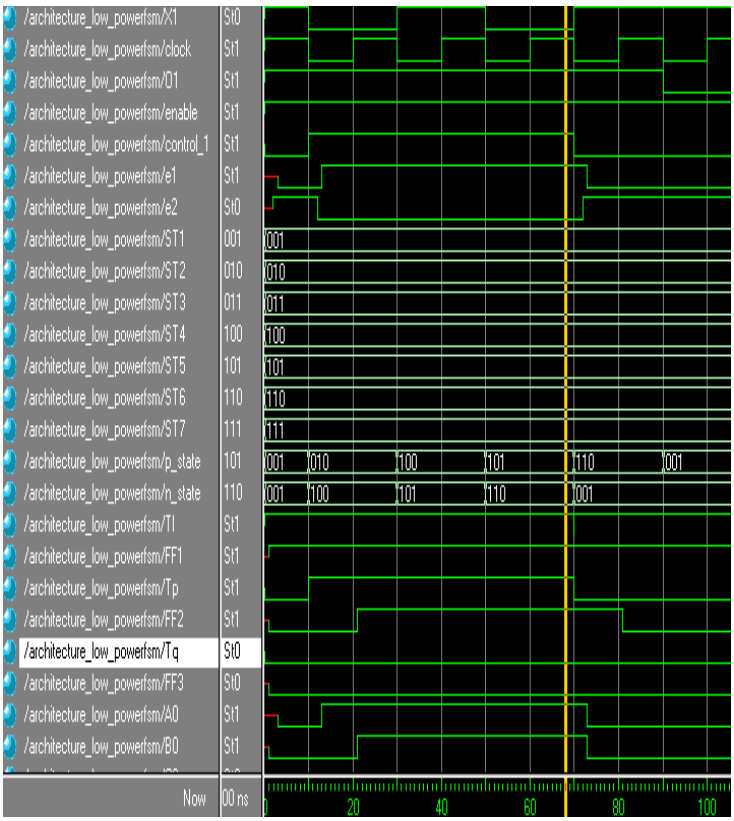


Figure (a)

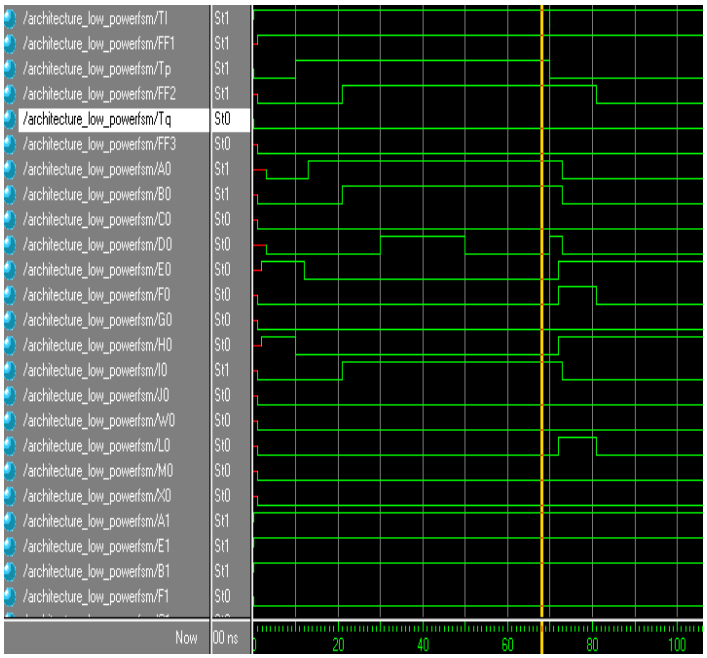


Figure (b)

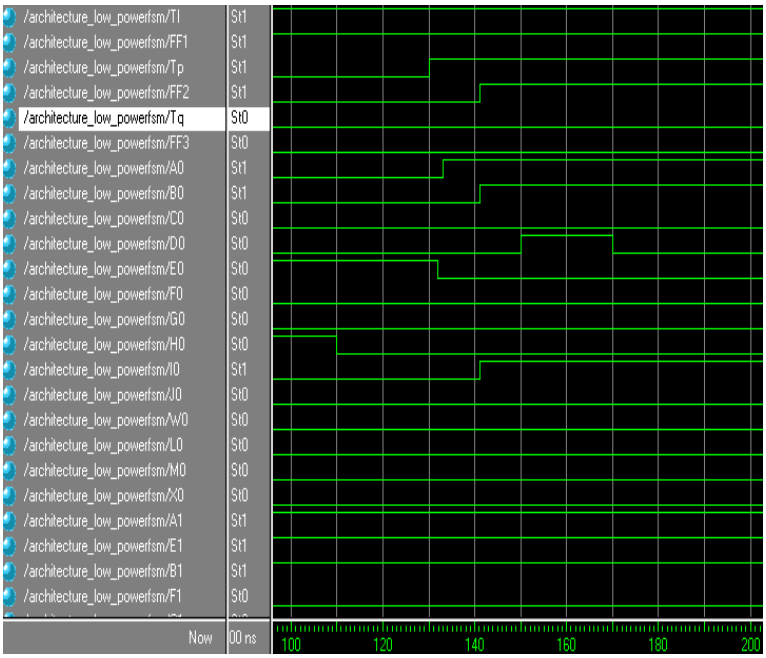
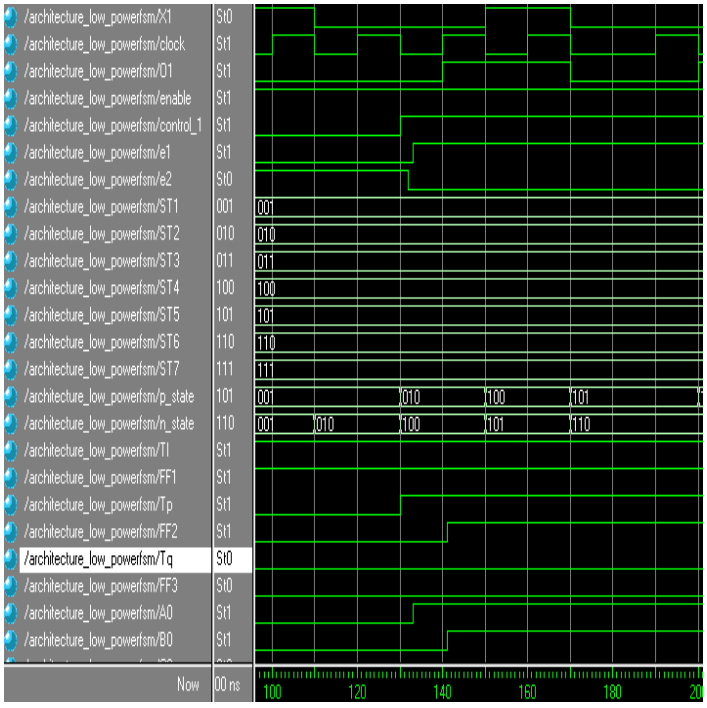


Figure (d)



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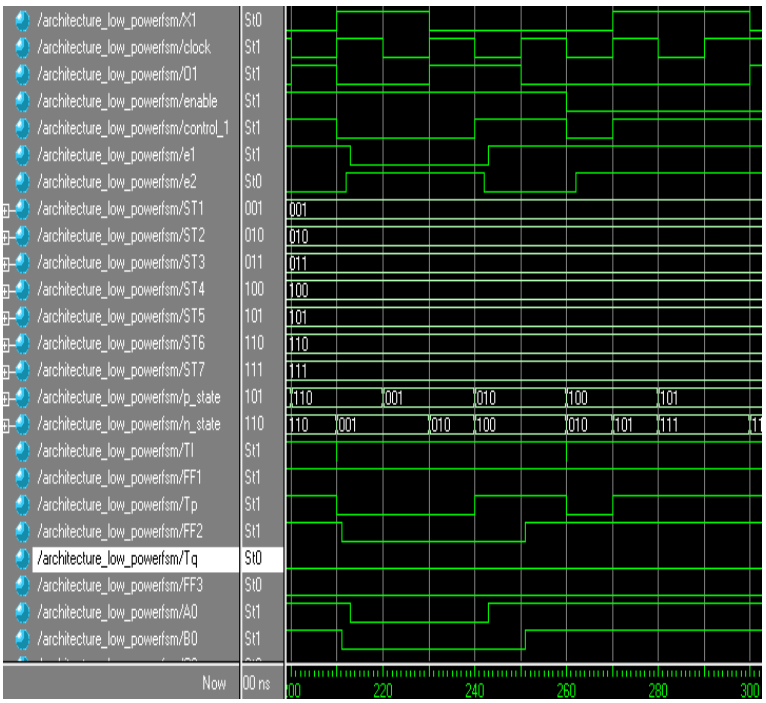

Figure (e)

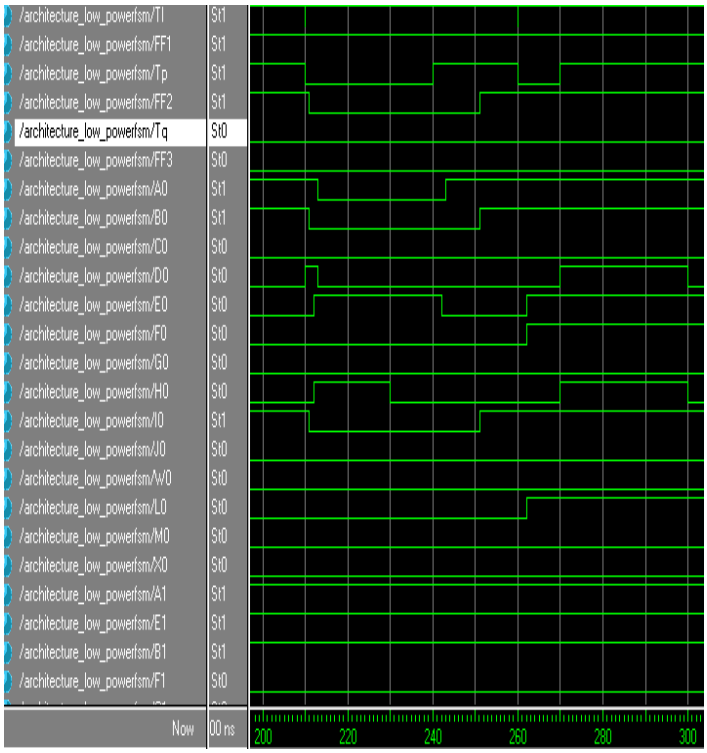

Figure (f)

Figure (a), (b) , (c) ,(d) ,(e) ,(f) shows output waveform representing State transition at an architecture level .

VII. CONCLUSION

The Architectural level technique leads in a 12% average reduction of the total switching activity of the implemented circuit. Although the solution is heuristic, and does not guarantee the minimum power consumption, these results leads to a reduction in the power consumption in the complete circuit, not just used in the part used for the computation and the storage of the state information.

VII. REFERENCES

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