Parameter Extraction and Analysis of Pentacene Thin Film Transistor with Different Insulators

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Abstract— **This paper presents both analytical modeling and simulations based on finite element method of Pentacene Thin Film Transistors or Organic Thin Film transistors (PTFTs/OTFTs). Analytical modeling approach is introduced by using conventional transistor equations and finite element method using ATLAS two dimensional numerical device simulators. Both the methods shows a good agreement of output characteristic and parameters with experimental results. Further simulation is performed for top contact OTFT devices with different insulator materials while pentacene is used as organic semiconductor (OSC) material. A large variation has been observed for different insulators which insight the importance for right selection of the material during fabrication. It has been observed that the best results can be obtained for Hafnium oxide (HfO_2) due to highest dielectric constant. Parameters such as current on-off ratio drain current and transconductance shows a variation of 85% or more for different insulators. However, a minor change is achieved for mobility analysis. This analysis clarifies a number of issues that can help in design and fabrication of devices on flexible substrates. The simulated results are demonstrated in terms of performance parameters such as output and transfer characteristics, drain current, mobility, threshold voltage, I_{ON}/ I_{OFF} and transconductance.**

Index Terms— **Insulator, Mobility, Pentacene, Organic Thin Film transistors (OTFTs), Top contact OTFTs.**

I. INTRODUCTION

OTFT is likely to have suitable applications requiring large area coverage, structural flexibility and low cost which was not possible with crystalline silicon [1]. Fabrication of OTFTs at lower temperature allows wide range of substrate possibilities and build organic transistors as future candidate for many low-cost electronics applications that require flexible polymeric substrates such as RFID tags, smart cards, electronic paper, touch screen mobile phones and active matrix flat panel displays [2]. However, the innovative human mind soon searched a novel class of TFTs based on organic or polymeric semiconductor as active layer material that shows amazing possibility for integration on flexible plastic substrates, thus giving the world an idea of futuristic technology of low cost, thin, printable electronics, strong, flexible and lightweight displays [3]. Organic transistor based circuits are potentially useful in number of applications where high speeds are not essential. Organic semiconductors are actually a new class of materials comprising small molecules and polymers with semiconducting properties [4].

Many organic semiconductor materials have been analyzed including pentacene, poly (3-octylthiophene) (P3OT), poly (3-alkylthiophene) (P3AT) and poly (3-hexylthiophene) (P3HT) are the organic materials for semiconducting layer, but pentacene is the most extensively used organic material because of extensive reports on its performance [5]. Although, most of the works are focused on optimizing the organic semiconductor material in terms of higher carrier mobility, but it is desirable to use plastic substrates to achieve flexible display devices. To meet the goal, gate insulator material should be organic to reduce thermal stress induced by the difference in thermal expansion coefficient between TFT organic semiconductor layer and substrate. Organic polymers have good process ability and dielectric properties such as poly methyl methacrylate (PMMA), fluoropolymer and CYTOP. This paper reports the simulation of pentacene based TFT with various combinations of insulator material and illustrates the performance dependency on right selection of insulator material [6].

II. DEVICE DESIGN AND SIMULATION SETUP

A. *Finite Element Type Simulation*

An OTFT is a transistor composed of thin film of current carrying semiconductor, an insulator layer and three electrodes. The primary difference between the geometry of conventional MOSFETs and OTFTs is that organic material based device does not have a fourth terminal that is body, thus making these transistors free of the body effect. Secondly, in inorganic based devices have the conduction channel formed by an inversion layer while in OTFT, it is because of accumulation layer. Classification of organic thin film transistor is shown in Fig. 1 [7]. In the top contact device structure, source/drain electrodes are deposited on the semiconductor film, while in bottom contact devices, this deposition sequence is reversed [2, 4].

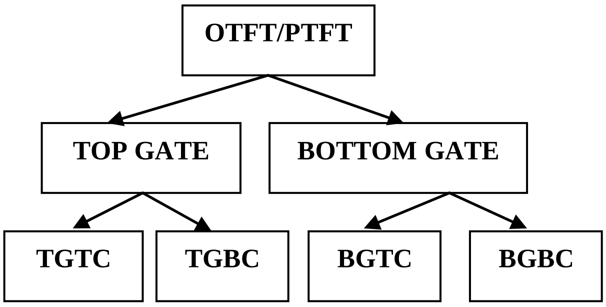
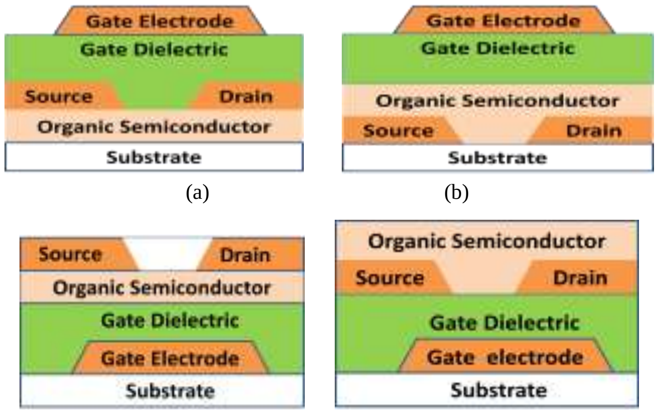


Figure 1. (a) Classification of Organic or Pentacene Thin Film Transistors (OTFT/PTFTs) structures.

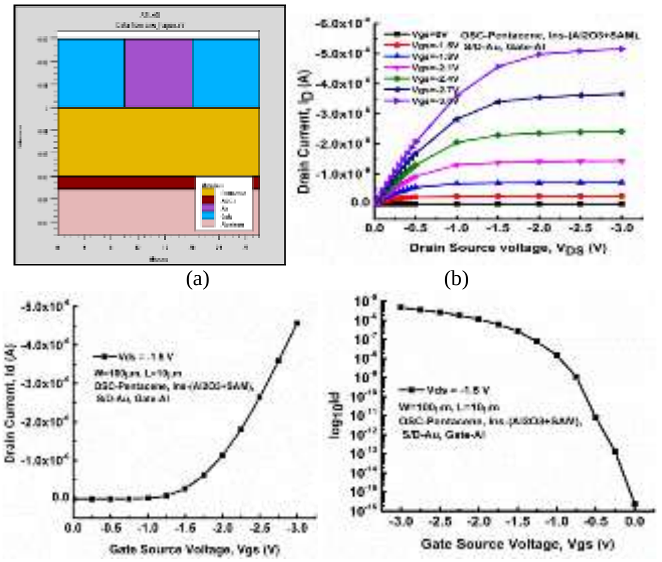


(a) (b) (c) (d)

Figure 2. Schematics of cross sectional view for (a) Top gate top contact (TGTC) (b) Top gate bottom contact (TGBC) (c) Bottom gate top contact (BGTC) and, (d) Bottom gate bottom contact (BGBC) structures.

For simulation of OTFTs certain architectures have been proposed as shown in Fig. 2(a) through Fig. 2(d), out of which bottom-gate-top-contact (BGTC) and bottom-gate-bottom-contact (BGBC) architecture are enormously modeled devices [4]. The deposition of organic semiconductor on the insulator is much easier than the reverse due to fragile nature of organic semiconductors; hence bottom gate architecture is built in majority for current OTFTs. In terms of field effect mobility, BGTC structure shows better performance in comparison with BGBC structure. The better field effect mobility for top contact OTFT is due to less contact resistance than that of a bottom contact one [8].

The simulations are performed for BGTC device with finite element based ATLAS two dimensional numerical device simulator. Fig. 3(a) through Fig. 3(d) depicts simulation results which include device structure, output and transfer characteristics and $\log_{10}I_D$ curve. In spite of Al_2O_3 insulator, self assembled monolayer (SAM) is considered as per given in experimental setup [4, 9].



(a) (b) (c) (d)

Figure 3. BGTC (a) Device structure, (b) O/P (I_D-V_{DS}) Characteristics, (c) Transfer (I_D-V_{GS}) Characteristics and (D) $\log_{10}I_D$-V_{GS} curve.

In this paper major parameters used in 2-D device simulation for channel length (*L*), Channel width (*W*), Al_2O_3+SAM insulator thickness (t_{ox}), and pentacene active layer thickness (t_P) are 10µm, 100µm, 5.7nm, and 30nm respectively. The thickness of gold (*Au*) S/D contacts is 30 nm and aluminum (*Al*) gate electrode is 20 nm [9].

The properties of pentacene organic semiconductor material used in simulation include energy gap of 2.2 eV, permittivity is 4.0, electron density of state of 2.88 x 10^{21} per cm^3 in valance band and conduction band and [10]. Mobility of electron and hole is taken as 5 x 10^{-5} and 0.70 respectively. Poole-Frenkel like electric-field dependence, which is the inverse variation in activation energy against the square root of electric –field strength expression, has been employed for pentacene active channel. To carry out finite element based simulation, Poole-Frenkel mobility model is expressed as,

$$\mu(E)=\mu_0 \exp\left[-\frac{\Delta}{kT}+\left(\frac{\beta}{kT}-\gamma\right)\sqrt{E}\right] \qquad (1)$$

where E is electric field and $\mu(E)$ is field dependent mobility, μ_0 is zero field mobility, β is poole frankel factor, Δ is zero field activation energy, *K* is boltzmann constant and *T* is temperature. According to this model thermal excitation of trapped charge carriers is enhanced due to electric field.

B. *Analytical modeling*

To verify the parameters obtained through 2-D device simulation, we have also done MATLAB simulation It is employed using the standard equation of transistor (2) for linear and (3) for saturation regions

$$I_{D,lin}=\frac{W\mu C_i}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{{V_{DS}}^2}{2}\right] \qquad (2)$$

For $V_{GS}-V_{th}>V_{DS}$ (linear regime)

$$I_{D,sat}=\frac{W\mu C_i}{2L}(V_{GS}-V_T)^2 \qquad (3)$$

For $V_{DS}>V_{GS}-V_{th}>0$ (saturation regime)

where C_i is the capacitance per unit area of gate insulator material, μ_{lin} and μ_{sat} are field effect mobility for linear and saturation regions; V_{GS}, V_{DS} and V_T are gate, drain and threshold voltage respectively. Whereas *L* and *W* are channel length and channel width of OTFT respectively. Table I. shows comparison of extracted parameters with MATLAB simulation and experiment results. Simulations have been carried out for these models to modified and adjusted to account for the characteristics parameters.

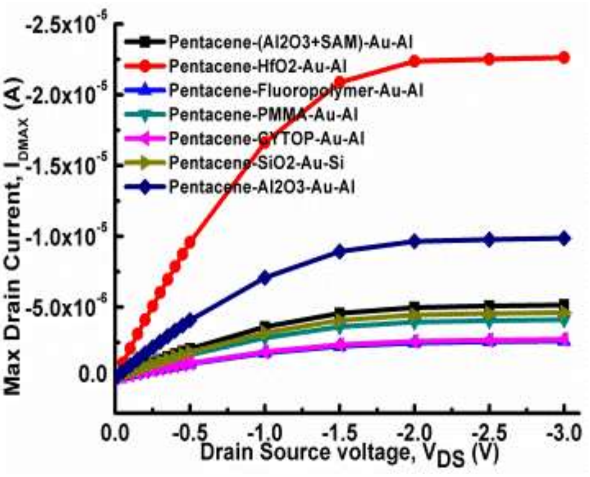
TABLE I. CHARACTERISTICS PARAMETERS THROUGH EXTRACTION, SIMULATION, ANALYTICA AND EXPERIMENT FOR BGTC DEVICE.

Characteristics Parameters	**Simulation**	**Analytical**	**Exp. [9]**
Threshold, V_T (V)	-1.18	-1.0	-1.1 V
Sub-threshold slope, *SS* (mV/dec)	91	96	100
Transconductance, *gm* (µS)	3.9	4.0	4.0
Mobility, μ_{sat} (cm^2/V.s)	0.364	0.37	0.4
Current on-off ratio, I_{ON}/I_{OFF}	3.9×10^7	5.5×10^7	10^7

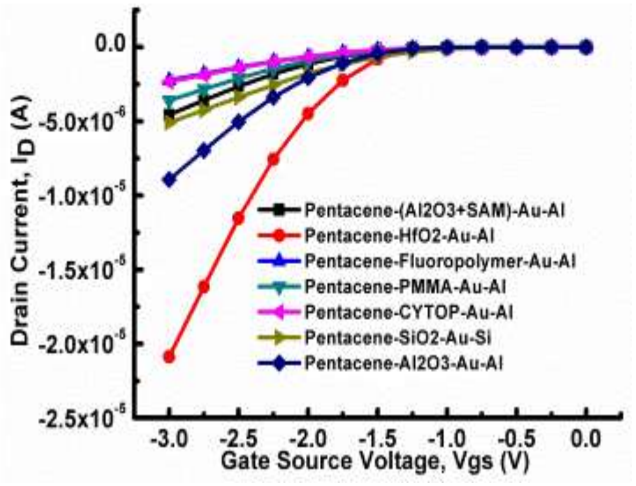
Drain current (μA) at V_{GS} = -3V	5.1	5.5	5.0
Drain current (pA) at V_{GS} = 0V	0.13	0.10	5.0

III. PARAMETERS EXTRACTION FOR DIFFERENT INSULATOR MATERIALS

We have done the simulation for various BGTC devices with pentacene as OSC, gold S/D contacts and different insulator materials to highlight the impact of insulator material on performance of OTFT. All the structures are simulated in the above organic module known as ATLAS environment with identical dimensions. The output and transfer characteristics of OTFT have been analyzed by use of proper boundary condition and physics of OTFTs [7]. Table-II includes the dielectric constant (D.C), calculated insulator capacitance (C_i), obtained maximum and minimum drain currents (I_{Dmax} and I_{Dmin}) for various insulator materials with pentacene organic semiconductor.



(a)



(b)

Figure 4. (a) I_D-V_{DS} curves at constant V_{GS}=-3V (I_{Dmax}), (b) I_D-V_{GS} curves at constant V_{DS}=-1.5V for structures containing pentacene, Au contacts, Al gate and various insulator materials.

From the table-II and Fig. 4 (a) and 4 (b) it is clear that at V_{GS}=-3V, the highest current (22 μA) is obtained for HfO_2 insulator with pentacene as semiconductor. The leakage current is also minimum (0.005 pA) for this combination due to maximum dielectric constant hence maximum gate capacitance. The characteristic performance of devices is evaluated in terms of various extracted parameters like mobility, threshold voltage, transconductance, on-off current ratio and subthreshold slope.

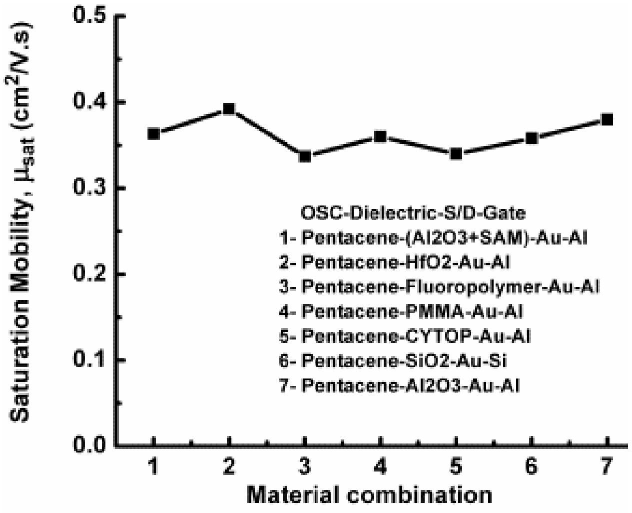
TABLE II. DIELECTRIC CONSTANT (D.C.), CAPACITANCE, MAXIMUM (I_{DMAX}) AND MINIMUM (I_{DMIN}) DRAIN CURRENTS FOR DIFFERENT INSULATOR MATERIALS WITH PENTACENE.

Material combinations (OSC, Ins, S/D, Gate)	**D. C.**	**C_i (μF/cm^2)**	**I_{Dmax} (μA)**	**I_{Dmin} (pA)**
Pentacene, Al_2O_3+ SAM, Au, Al	4.5	0.7	-5.1	-0.13
Pentacene, HfO2, Au, Al	22	3.4	-22	-0.005
Pentacene, Fluoropolymer, Au, Al	2.1	0.33	-2.6	-1.8
Pentacene, PMMA, Au, Al	3.5	0.54	-4.1	-0.29
Pentacene, CYTOP, Au, Al	2.2	0.34	-2.7	-1.5
Pentacene, SiO2, Au, Si	3.9	0.61	-6.2	-42
Pentacene, Al2O3, Au, Al	9.1	1.41	-9.8	-0.02

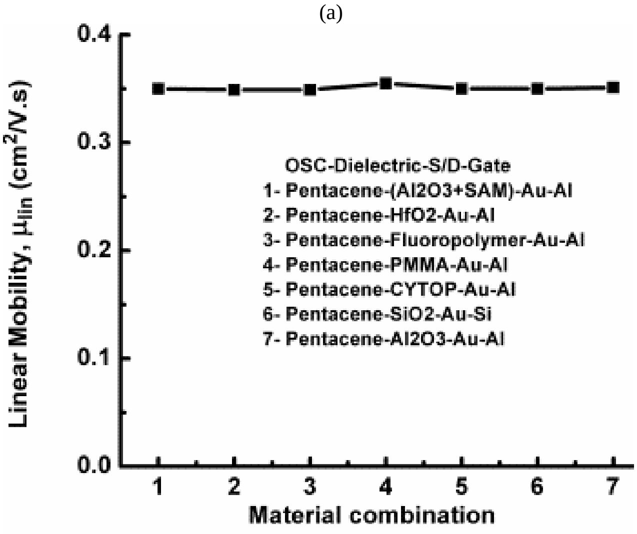
A. *Mobility, Threshold voltage and Transconductance*

The transistor requires larger mobility for reliable operation [11]. The bias dependent mobility, expressed as power law for organic thin film transistor is given by:

$$\mu\,(V_{GS}) = \mu_0\,(V_{GS} - V_T)^{\gamma} \qquad (4)$$



(a)



(b)

Figure 5. (a) Mobility in saturation region (μ_{sat}), (b) Mobility in linear region (μ_{lin}), for structures containing pentacene, Au contacts, Al gate and various insulator materials.

where μ_0 is reference mobility of material at low overdrive voltage (V_{GS}-V_T) about 0.5V and γ is mobility enhancement factor. The parameter γ is usually estimated in the range of ~ 0.2 – 0.5 for different OTFTs. γ is a result of an exponential trap distribution with characteristic temperature (T_c) at absolute temperature (T) with relation $\gamma = (T_c - T) / T$ [11].

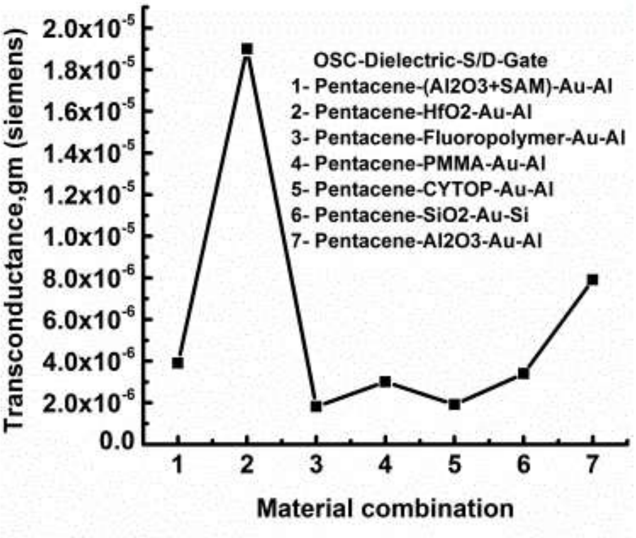
We have evaluated the saturation and linear region mobility from transfer characteristics of OTFT as shown in Fig. 5 (a) and (b), respectively using standard equation of field effect mobility (μ) and transconductance (g_m).

$$g_m = \frac{\partial I_{D,lin}}{\partial V_{GS}} \tag{5}$$

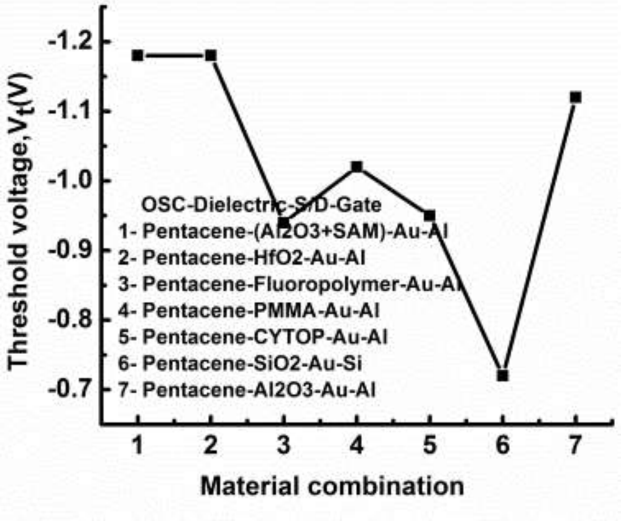
$$\mu_{lin} = \frac{L g_m}{W C_i V_D} \tag{6}$$

$$\mu_{sat} = \frac{2L}{W C_i}\left(\frac{\partial\sqrt{I_{Dsat}}}{\partial V_{GS}}\right)^2 \tag{7}$$

where g_m is transconductance and $\frac{\partial\sqrt{I_{Dsat}}}{\partial V_G}$ is slope of the curve [7].



(a)



(b)

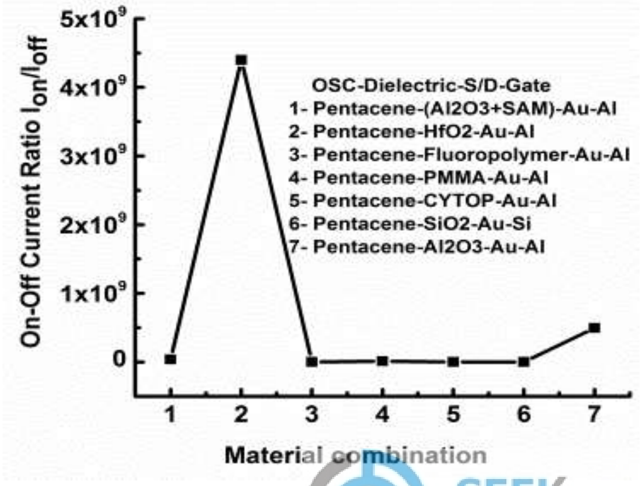
Figure 6. (a) Transconductance (gm) and (b) Threshold voltage (V_T)

From Fig. 5 (a) and Fig. 5 (b) it can be analyzed that linear region mobility is almost constant for all combinations where as saturation region mobility shows slight variation about 16%. Mobility should increase for insulators containing lower dielectric constant and hence lower capacitance as per relation given in (5) and (6). But we have observed decreasing slope values with respect to decreasing dielectric constant. Due to which the effect is nullifying and extracted mobility is constant.

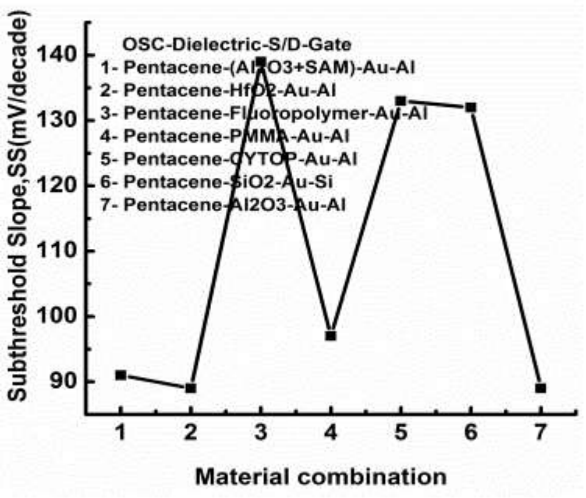
The transconductance should be high as it shows drain current modulation in variation with gate voltage. It is extracted from relation shown in (5) shows positive variations as moved to the insulator material of higher dielectric constant (D.C.) as shown in Fig. 6 (a). The minimum gate voltage at which the OTFT begins to conduct is called threshold voltage (V_T). As shown in Fig. 6 (b), V_T is lowest (-0.94V) for SiO_2 insulator material structure with silicon as gate. For further Structures, V_T is higher due to difference in work function of gate metal i.e. aluminum and other insulators. It can be further improved by optimize the gate material, doping concentration and thickness of insulator material [11].

B. On/off (I_{on}/I_{off}) Current Ratio and Subthreshold slope

I_{on}/I_{off} is ratio of current in the accumulation mode over current in the depletion mode [11].



(a)



(b)

Figure 7. (a) Current On/off (I_{on}/I_{off}) ratio and (b) Sub-threshold slope

I_{ON} is drain current above threshold voltage V_T at which saturation takes place and I_{OFF} is the drain current below threshold Voltage [11]. The extracted current on/off ratio is highest (4.4×10^9) for HfO_2 insulator due to maximum on current (22 µA) and minimum off current (0.005 pA) values as depicted in Fig. 7 (a). Sub-threshold slope is the ratio of change in gate voltage to the change in drain current on log scale at constant drain voltage. It is an important parameter which explains how best we can use transistor as a switch. As per results plotted in Fig. 7 (b) switching behavior of OTFT is better for HfO_2, PMMA and Al_2O_3 insulators as sub-threshold slope is lower (approx 90mV/dec.) for these material combinations with pentacene.

TABLE III. PERCENTAGE VARIATION IN EXTRACTED PARAMETERS FOR VARIOUS OTFTS STRUCTURES WITH DIFFERENT INSULATORS.

Performance parameters	**Variation range**	**% variation**
Max. drain current, I_{Dmax} (A) at V_{GS}=-3V	-2.61e-6 to -2.26e-5	88.4 ↓
Min. drain current, I_{Dmin} (A) at V_{GS}=0V	-5.14e-15 to -4.22e-11	97 ↓
Mobility, μ_{sat} (cm^2/V.s)	0.337 to 0.392	16.3 ↑
Mobility, μ_{lin} (cm^2/V.s)	0.349 to 0.355	1.7 ↑
Capacitance C_i (µF/cm^2)	0.33 to 3.4	90.2 ↓
Threshold, V_T (V)	-0.94 to -1.18	25.5 ↑
Current on-off ratio, I_{ON}/I_{OFF}	1.4e5 to 4.4e9	97 ↓
Sub-threshold slope, *SS* (mV/dec)	89 to 139	56 ↑
Transconductance, *gm* (µS)	1.82e-6 to 1.9e-5	89 ↓

IV. CONCLUSION

Simulation results analyze different performance parameters of pentacene TFTs with different insulator materials. From Table III, it has been observed that parameters shows large percentage variation for different insulators which insights the importance for right selection of the material during fabrication. The performance parameters such as I_{ON}/I_{OFF}, I_D and g_m shows more than even 85% variation as moved from one insulator to another. Basically for a particular organic semiconductor, variations in mobility can be observed with respect to doping concentration, mobility enhancement factor (ϒ) and overdrive voltage. Maximum ON and minimum OFF current are obtained as 22 µA and 0.005pA respectively for HfO_2 insulator material due to highest dielectric constant and thus maximum capacitance value is achieved. An organic device with fluoropolymer and CYTOP insulator shows minimum V_T which is desirable for low voltage operation of OTFTs. Best switching scenario has been seen for SiO_2 insulator with silicon as gate electrode. Most of the results are in favor of HfO_2 insulator and observed as optimized material for insulator layer with pentacene as organic semiconductor.

V. REFERENCES

[1] M. Jamal Deen, “Plastic microelectronics with organic and polymeric thin film transistors,” *Proc. 26th international conference on microelectronics* (MIEL 2008).

[2] Y. Sun, Y. Liu and D. Zhu, “Advances in organic field-effect transistors, ” J. mater. chem., vol. 15, pp. 53-65, 2005.

[3] H. Klauk, “Organic thin film transistor,” *Chem.Soc.Rev*., 39, pp. 2643-2666, 2010.

[4] M. J. Deen and M. Kazemeini, “Photosensitive polymer thin-film FETs based on poly (3-octylthiophene)P3OT,” *Proc. IEEE*, vol. 93, no. 7, pp. 1312–1320, Jul. 2005.

[5] C. Shekar, T. Lee and S. W. Rhee, “Organic thin film transistors, material, processes and devices,” *Korean J. Chem. Engg*., vol. 21, no. 1, pp. 267-287, 2004.

[6] P. Mittal, B. Kumar, B. K. Kaushik, Y.S.Negi and R .K. Singh, “Analysis of pentacene based organic thin film transistors through two dimensional finite element dependent numerical device simulation”. *IJCA Special Issue on Optimization and On-chip Communication* (OOC-1): pp. 11-17, 2012.

[7] G. Horowitz, E. Hajlaoui and R. Hajlaoui, “Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistor *J. Appl. Phys*, vol. 87, no. 9, 2000.

[8] H. Klauk, U. Zschieschang, and M. Halik, “Low-voltage organic thin-film transistors with large transconductance,” *J. Appl. Phys*., vol. 102, no. 7, pp. 074514-1–074514-7, Oct. 2007.

[9] Dipti Gupta, M. Katiyar and Deepak Gupta, “An analysis of the difference in behavior of top and bottom contact organic thin film transistors using device simulation,” *Organic Electronics*, vol. 10, pp. 775 - 784, 2009.

[10] M. Hamilton, S. Martin, and J. Kanicki, “Field-effect mobility of organic polymer thin-film transistors,” *Chem. Mater*., vol. 16, no. 23, pp. 4699–4704, 2004.

[11] P. Mittal, B. Kumar, Y. S. Negi, B. K. Kaushik and R. K. Singh , "Organic Thin Film Transistor Architecture, Parameters and their Applications," *International Conference on Communication Systems and Network Technologies (CSNT2011)*, pp.436-440, 2011.

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